Digital Front End (DFE) Training

DFE Overview

Agenda

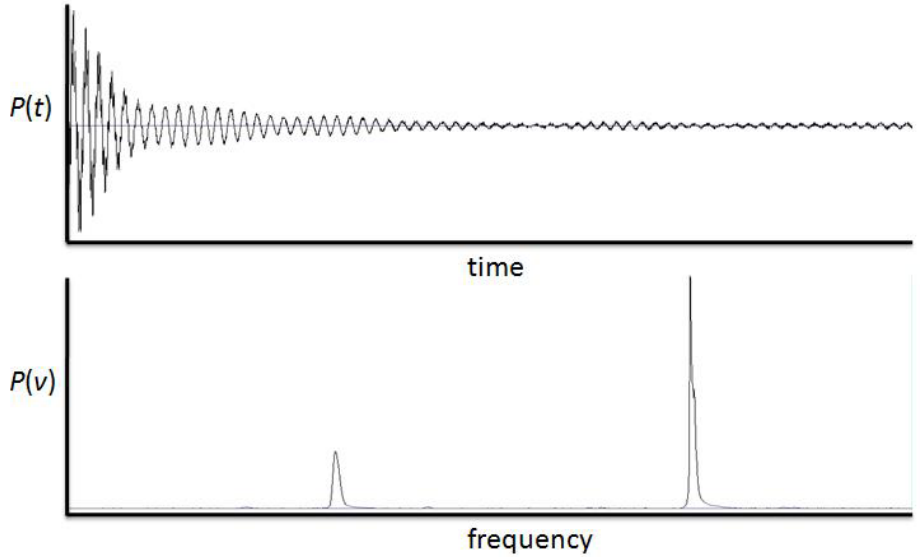
- High-speed Data Converter Systems Overview
- DFE High-level Overview
- DFE Functional Block Diagrams
- DFE Features
- DFE System Use Cases
- DFE Configuration

High-speed Data Converter System Overview (1)

- Signals can be represented in the time domain or frequency domain.
- In order to describe the signal processing in a high-speed data converter system on the following slides, it will be helpful to look at the signal in the frequency domain at several key places.

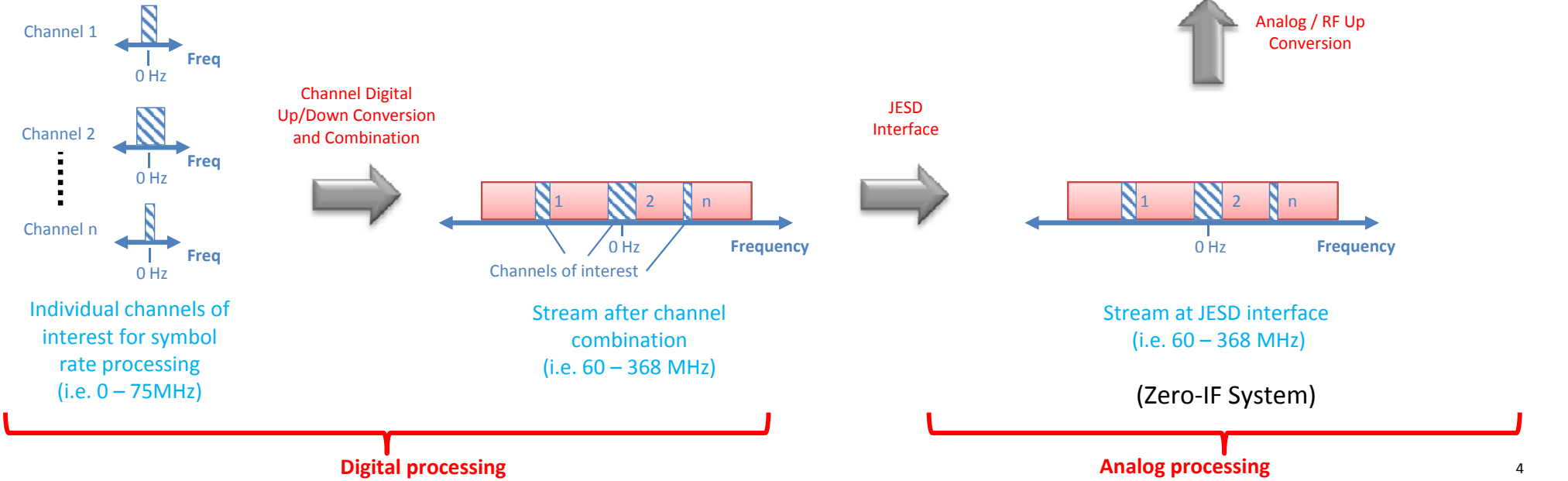
Time Domain:

Frequency Domain:



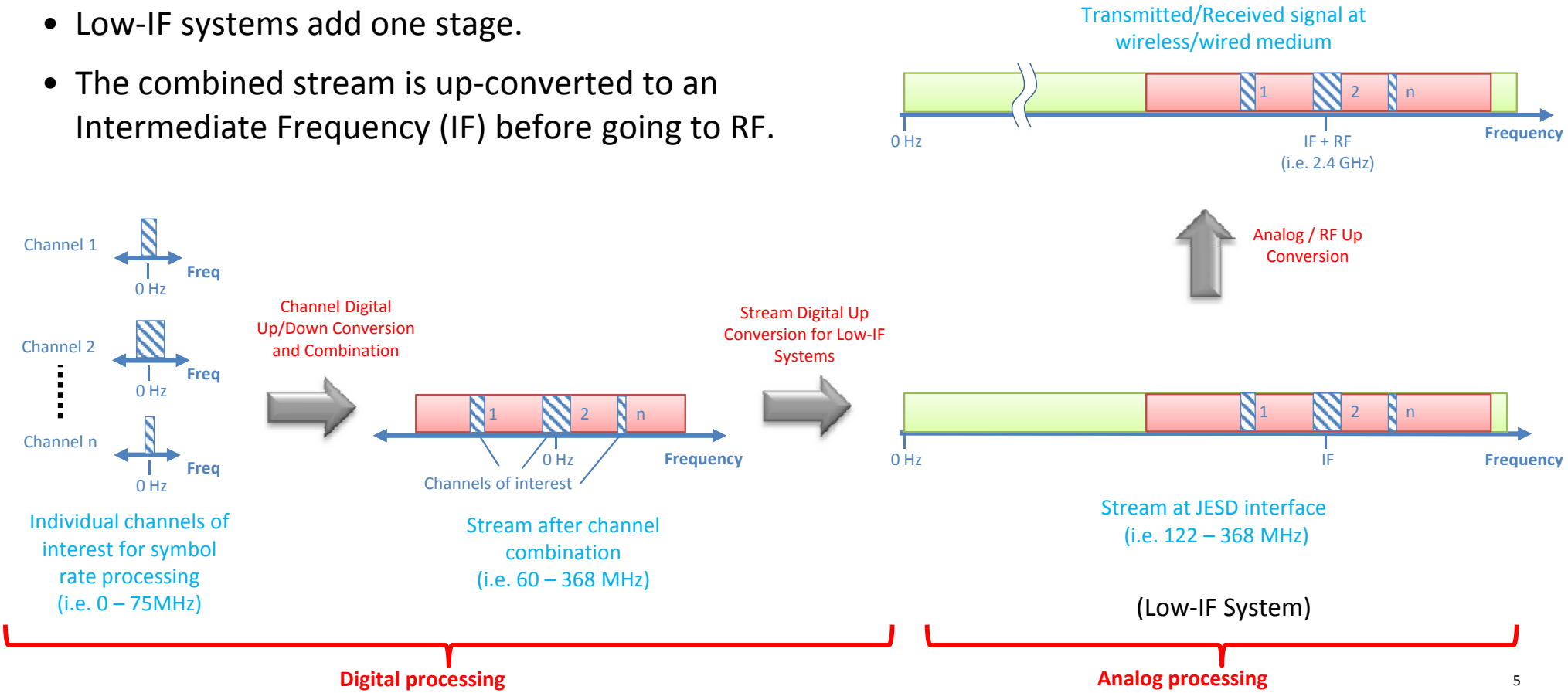
High-speed Data Converter System Overview (2)

- Processors handle data channels of interest at symbol rate.
- Digital up/down conversion and combination up-samples and moves the individual channels up or down in frequency and combines them into a higher bandwidth stream.
- The combined stream is sent across the JESD interface.
- Analog/RF processing moves the combined signal to RF so each channel ends up at the desired carrier frequency.

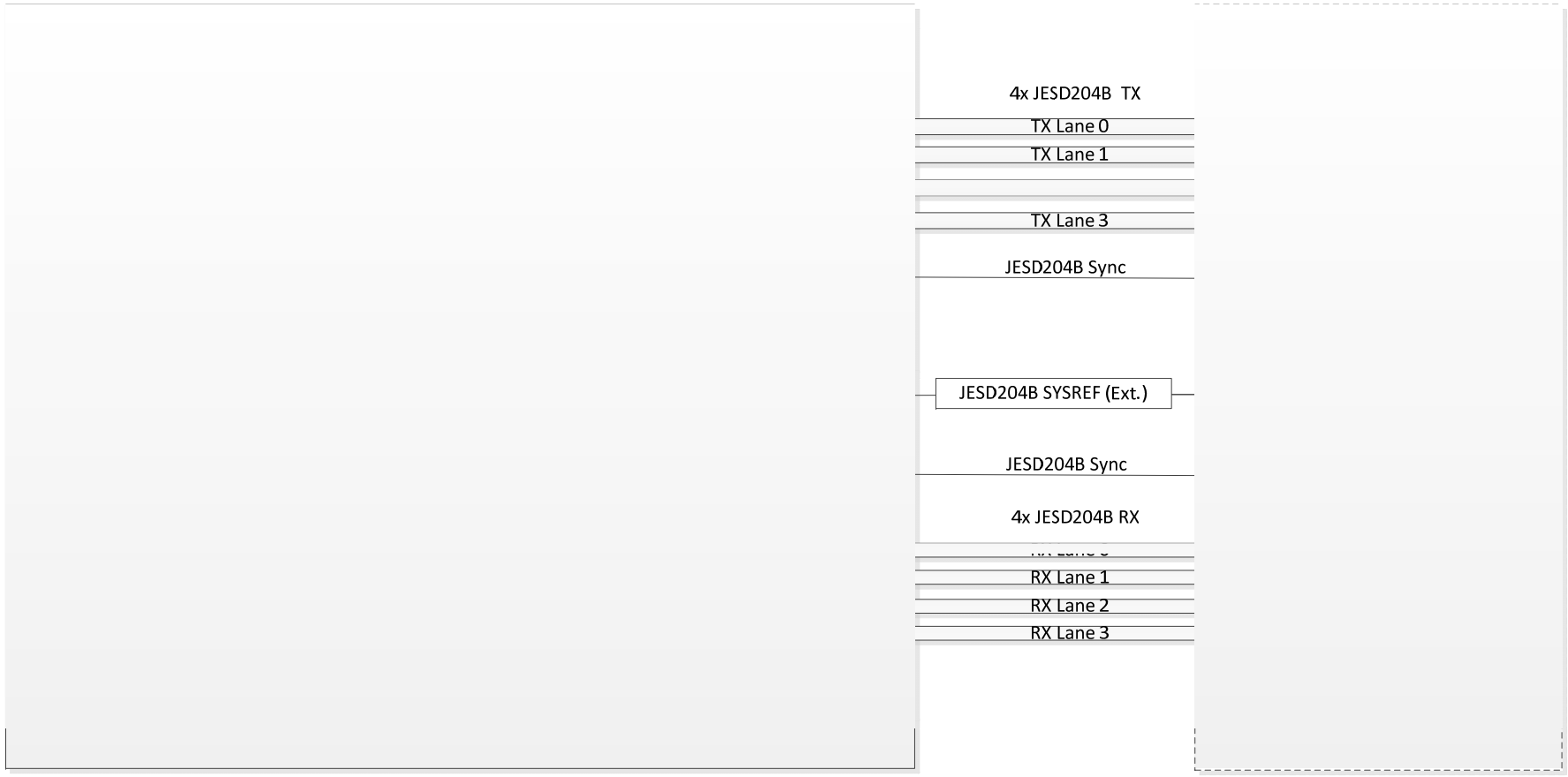


High-speed Data Converter System Overview (3)

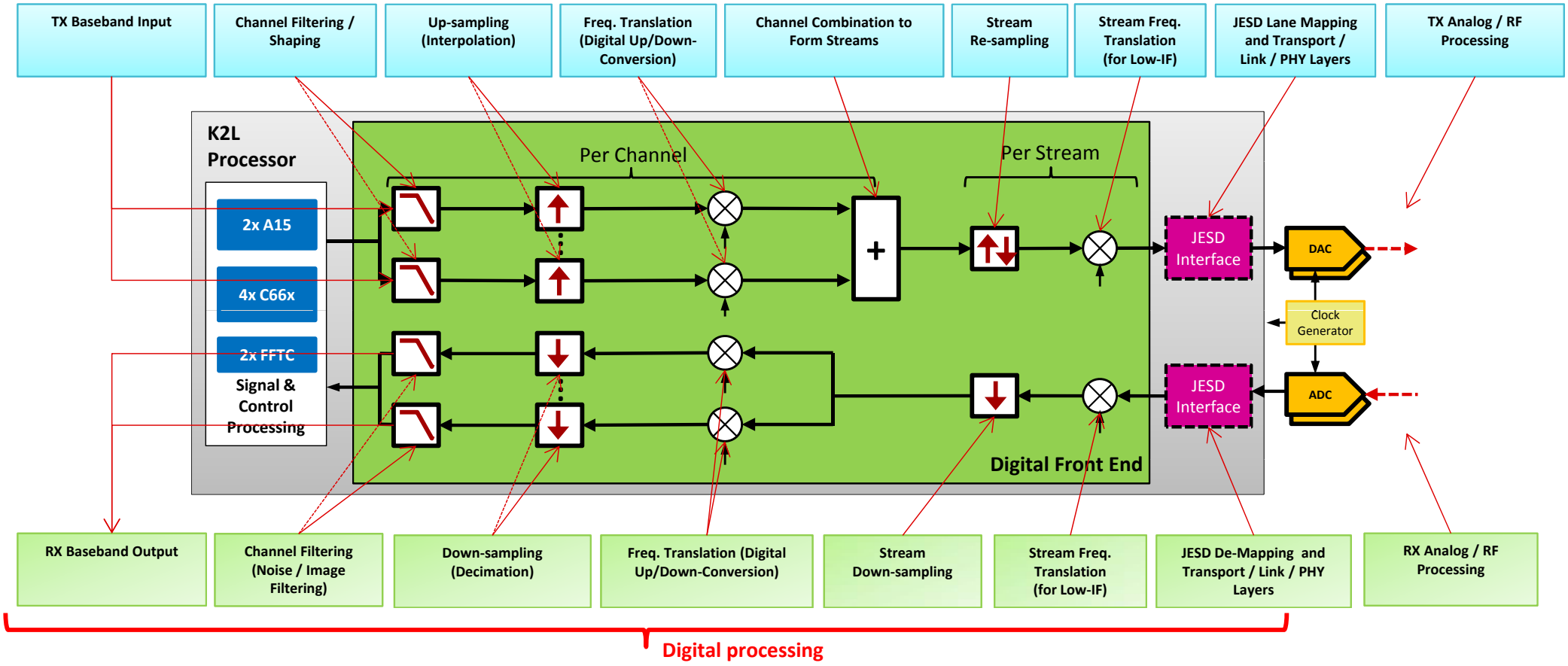
- Low-IF systems add one stage.
- The combined stream is up-converted to an Intermediate Frequency (IF) before going to RF.



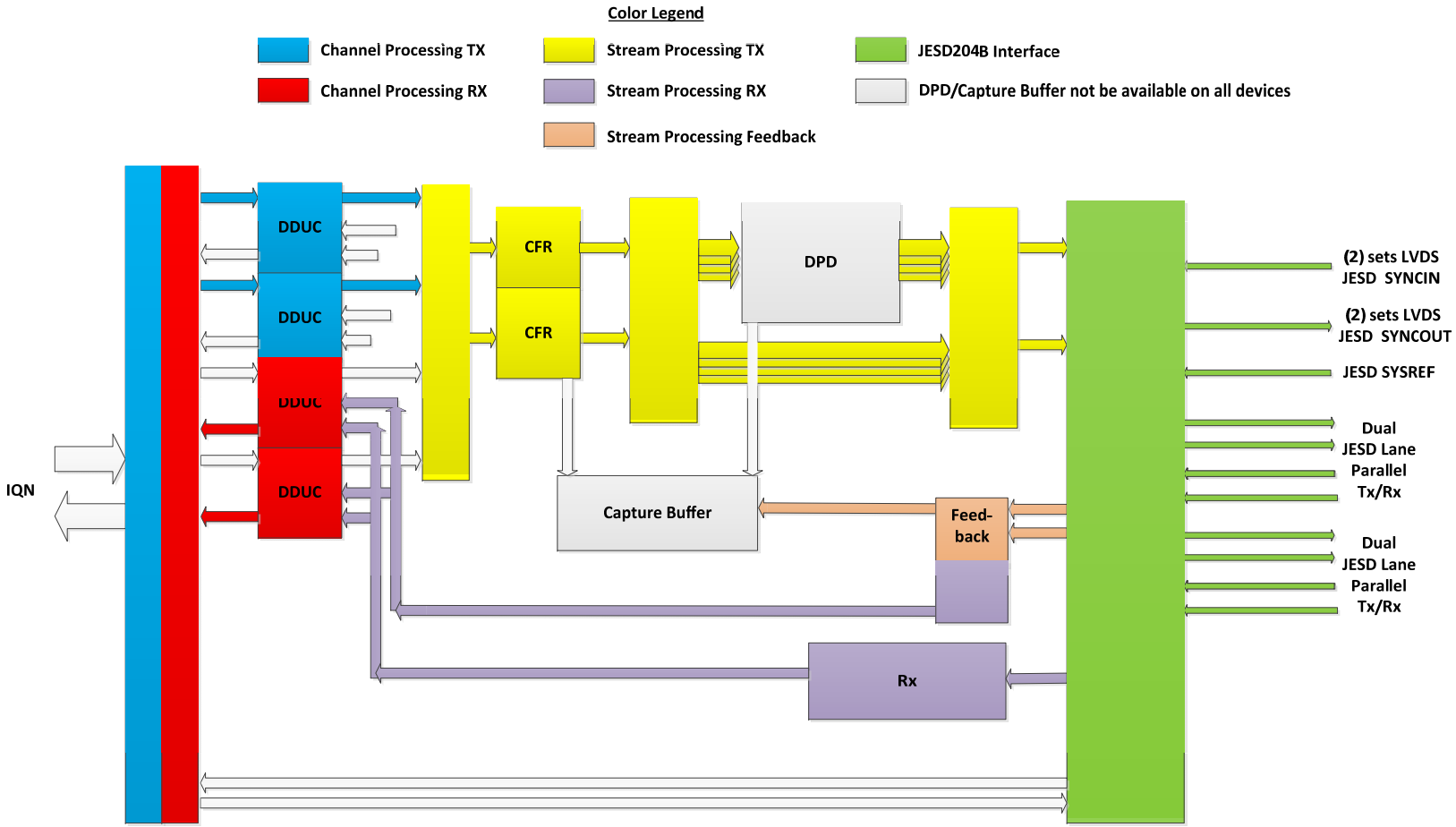
DFE High-level Overview



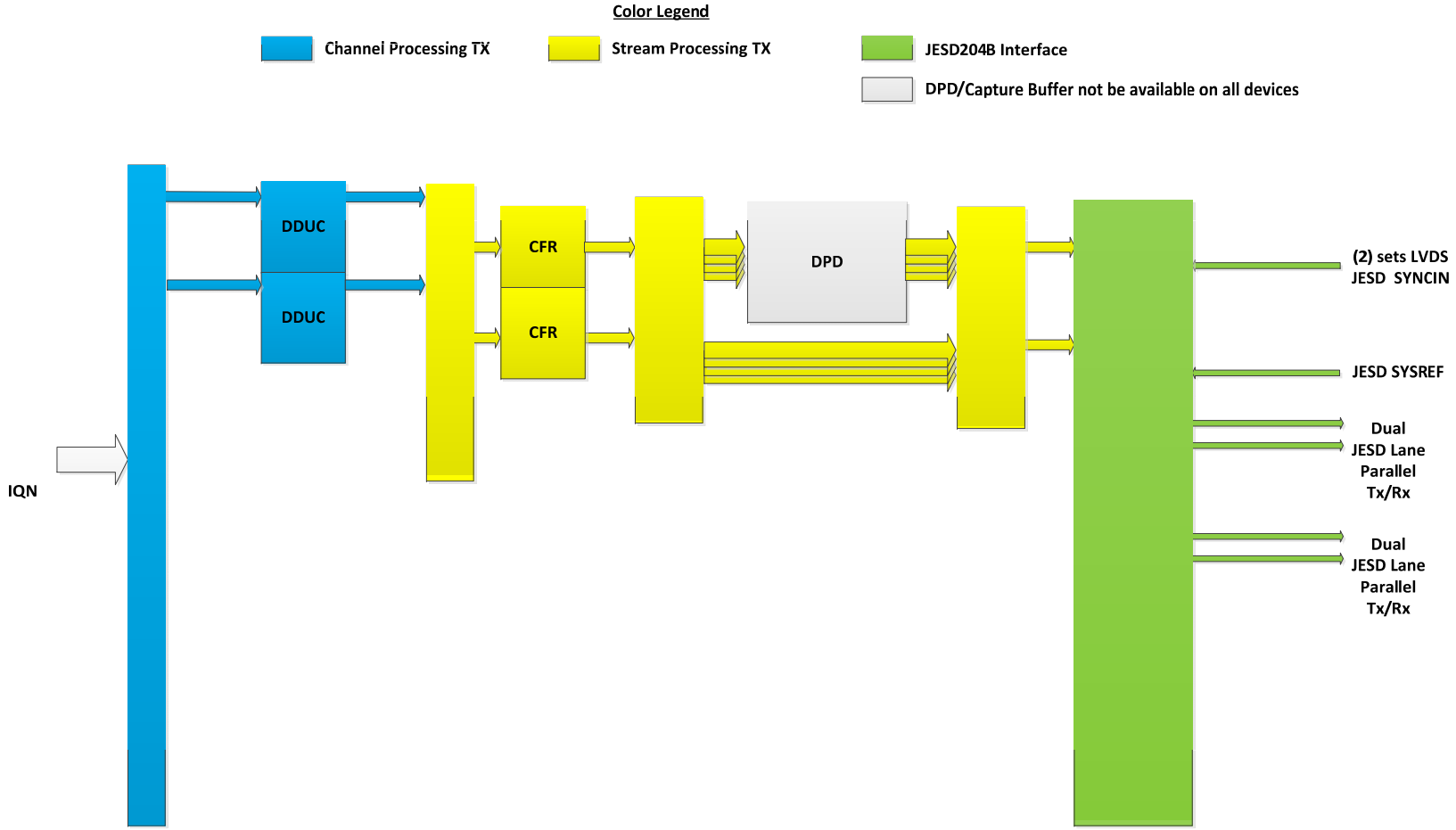
DFE Overview: Signal Processing Flow



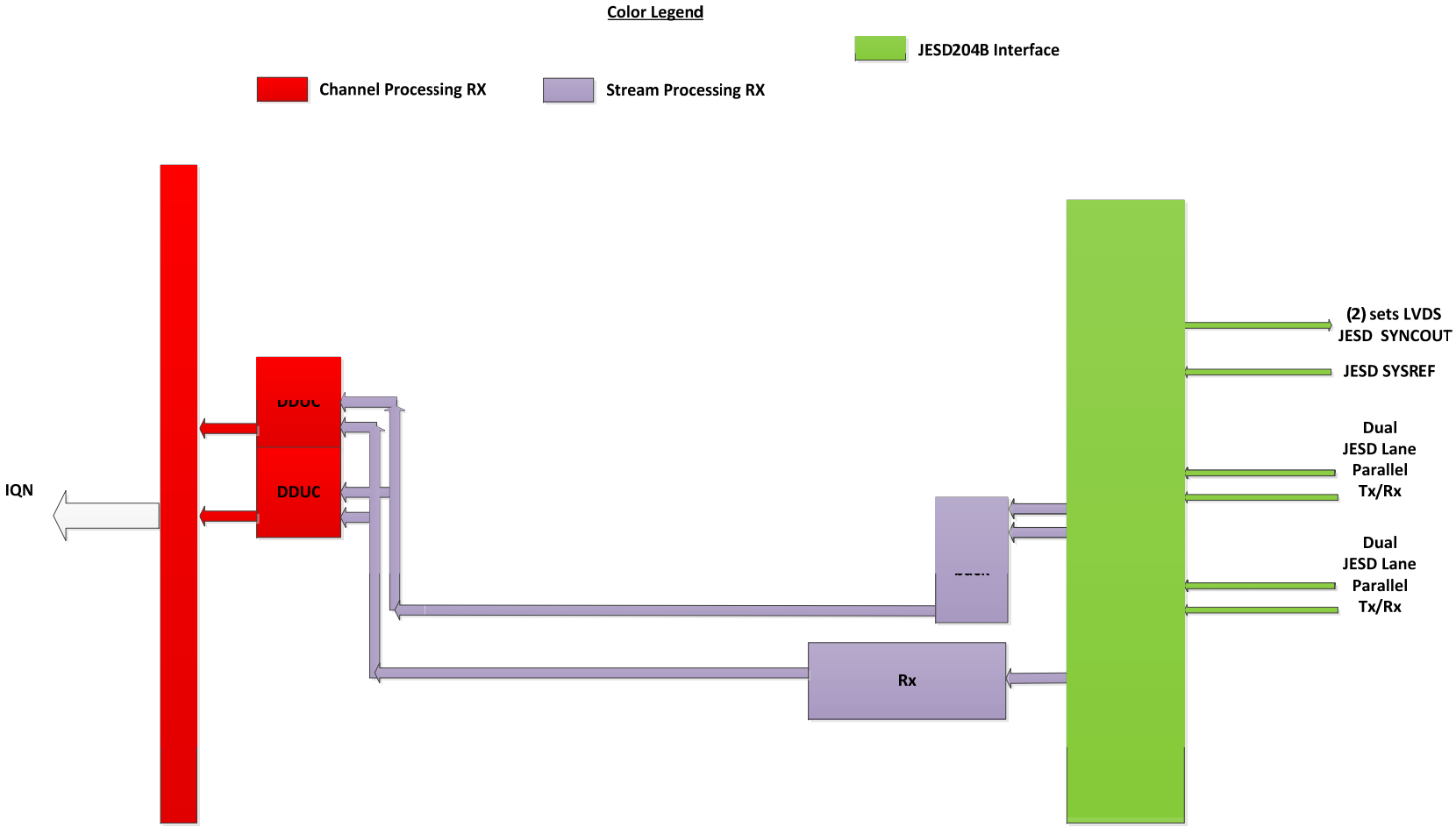
DFE Functional Block Diagram



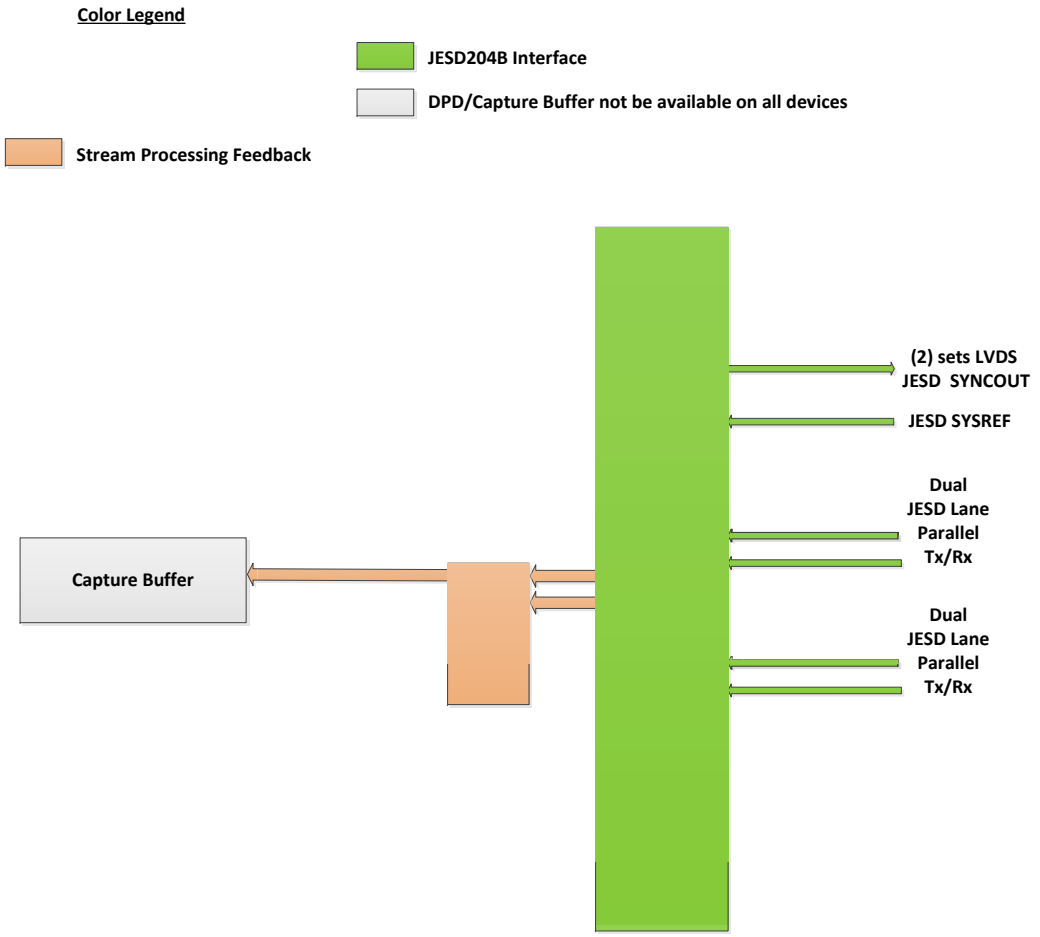
Transmit Path



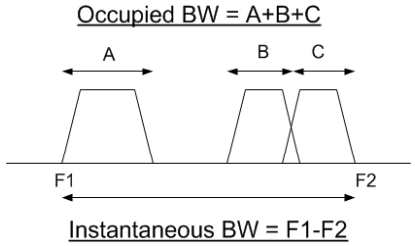
Receive Path



Feedback Path



DFE Features (1)



Key Features	Capacity
Direct JESD204B connectivity with high speed data converters	• Four JESD204B TX and RX Serdes lanes, each supporting data rates up to 7.37Gbps • Two sets of JESD SYNC IN/OUT signals allow connection with up to two devices simultaneously
Number of Streams (Antennas)	• Up to 4 transmit, 4 receive and 2 feedback streams (each RX and TX stream can be real or complex)

Number of Channels	• Four DDUCs (Digital Down/Up converters),each:
	  • Supports up to 12 channels
	  • Can be used for transmit or receive

Bandwidth Supported	• 368 MHz of instantaneous bandwidth • 150 MHz of occupied (processed) bandwidth • Fixed filters at the stream level provide 90% passband and 90dB stopband rejection

DFE Features (2)

Transmit processing	Receive processing
• **Channel processing**: Filtering (programmable FIR filter) , fractional re-sampling, frequency translation and summation (channel to stream conversion)	• **Channel processing**: Frequency translation, fractional re-sampling and filtering (programmable FIR filter)
• **Stream processing**: Fractional re-sampling, frequency translation (for low-IF support), JESD204B mapping and transport	• **Stream processing**: JESD204B transport and de-mapping, frequency translation (for low-IF support) and decimation
• Channel power meters for power monitoring	• Channel power meters for power monitoring
• Crest Factor Reduction (CFR)* and Digital Pre-Distortion (DPD)*	• Two feedback streams for TX monitoring (to support DPD*) or extra RX capacity
• TX signal processing bypass capability	• RX signal processing bypass capability

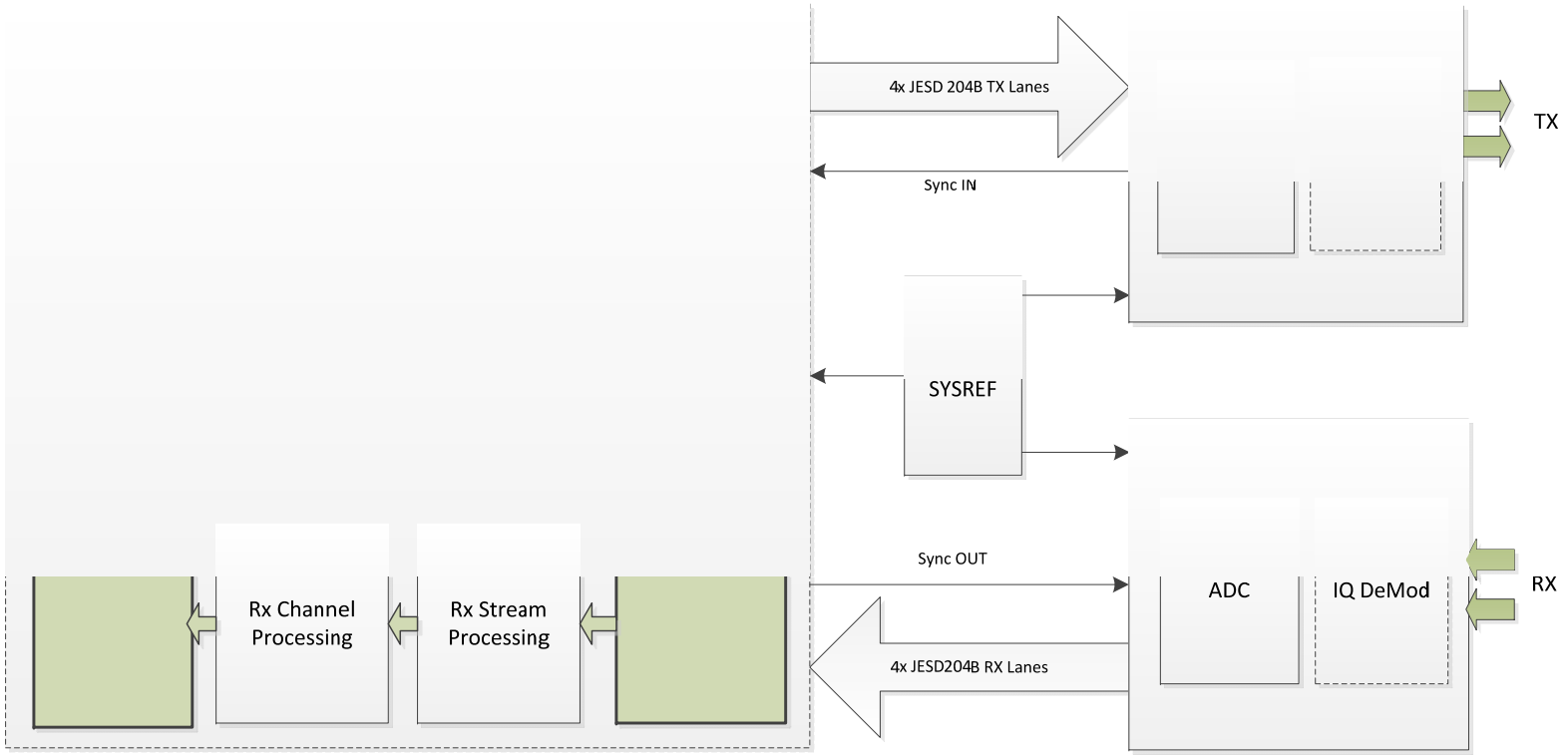
*Supported on K2L versions targeted towards wireless small cell base-station markets

DFE System Use Cases

Typical DFE system use-case scenarios include:

- Discrete ADC and DAC
- Integrated RF Transceiver
- DFE Signal processing bypass

Use Cases: Discrete ADC and DAC (1)

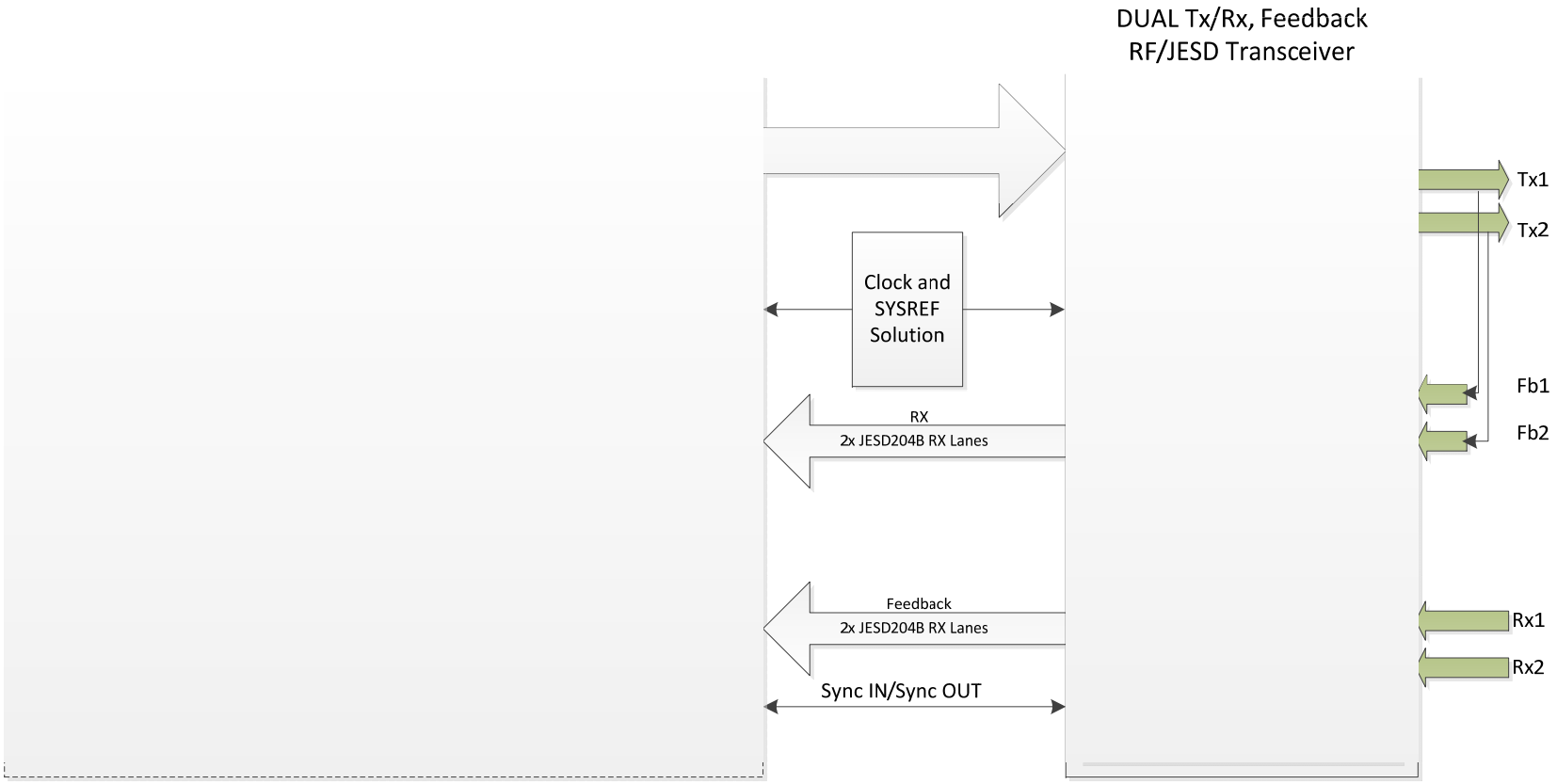


Use Cases: Discrete ADC and DAC (2)

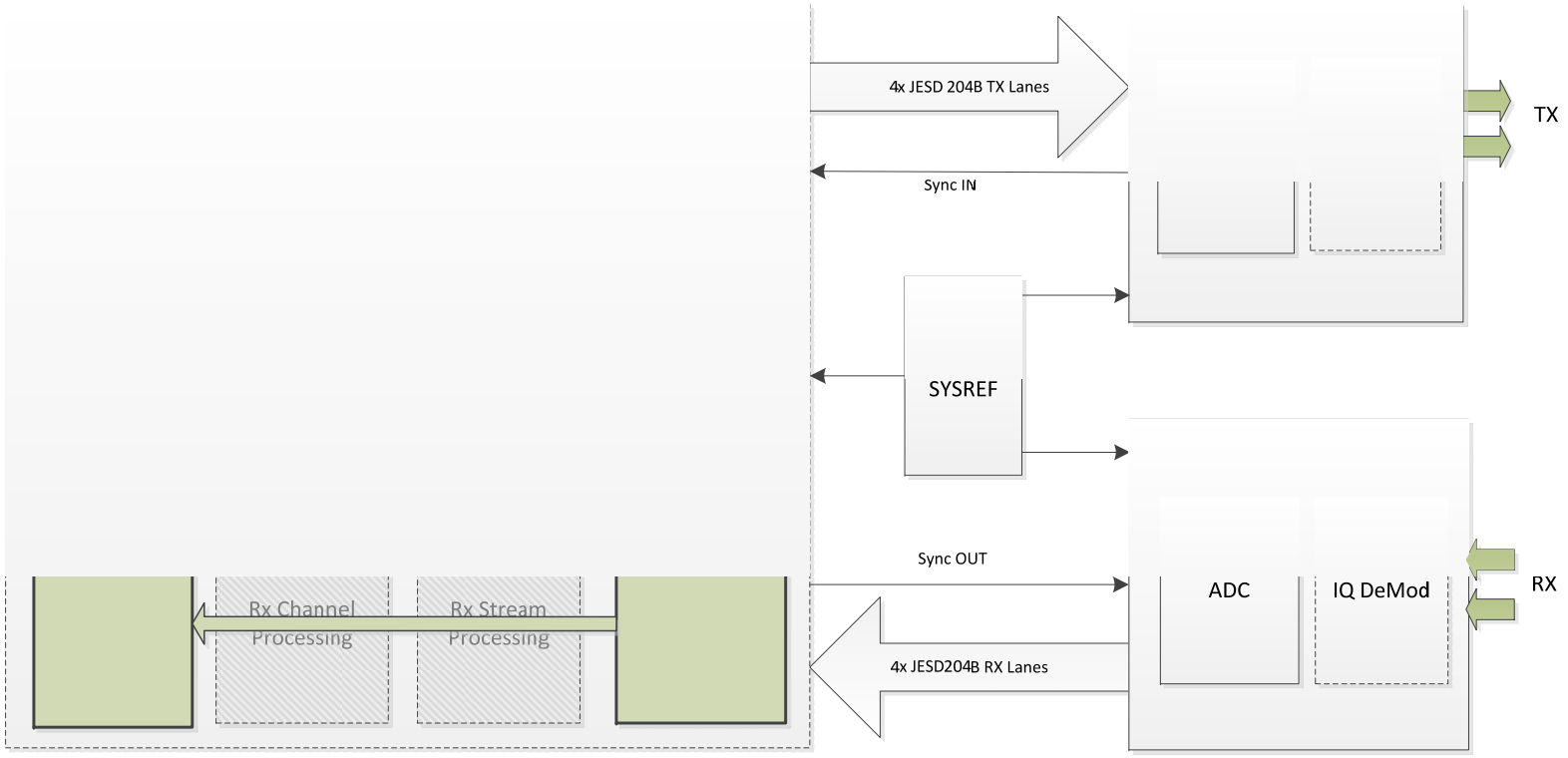
- Supported ADC classes:
  - RF Sampling: RF input/Complex output or Real input/Real output
  - Dual Real ADC (old technology): Complex input from IQ demodulator, Complex output
  - IF Sampling (Non zero-IF systems): Complex IF input, Complex output

- Supported DAC classes:
  - RF Sampling: Complex input, RF output (usually real)
  - Dual Real DAC (old technology): Complex input, Complex output at Zero-IF (for input to IQ modulator)
  - IF Sampling: Complex input, IF output (Real or Complex)
  - Single Real DAC: Real Input, Complex IF output

Use Cases: Integrated RF Transceiver



Use Cases: DFE Signal Processing Bypass

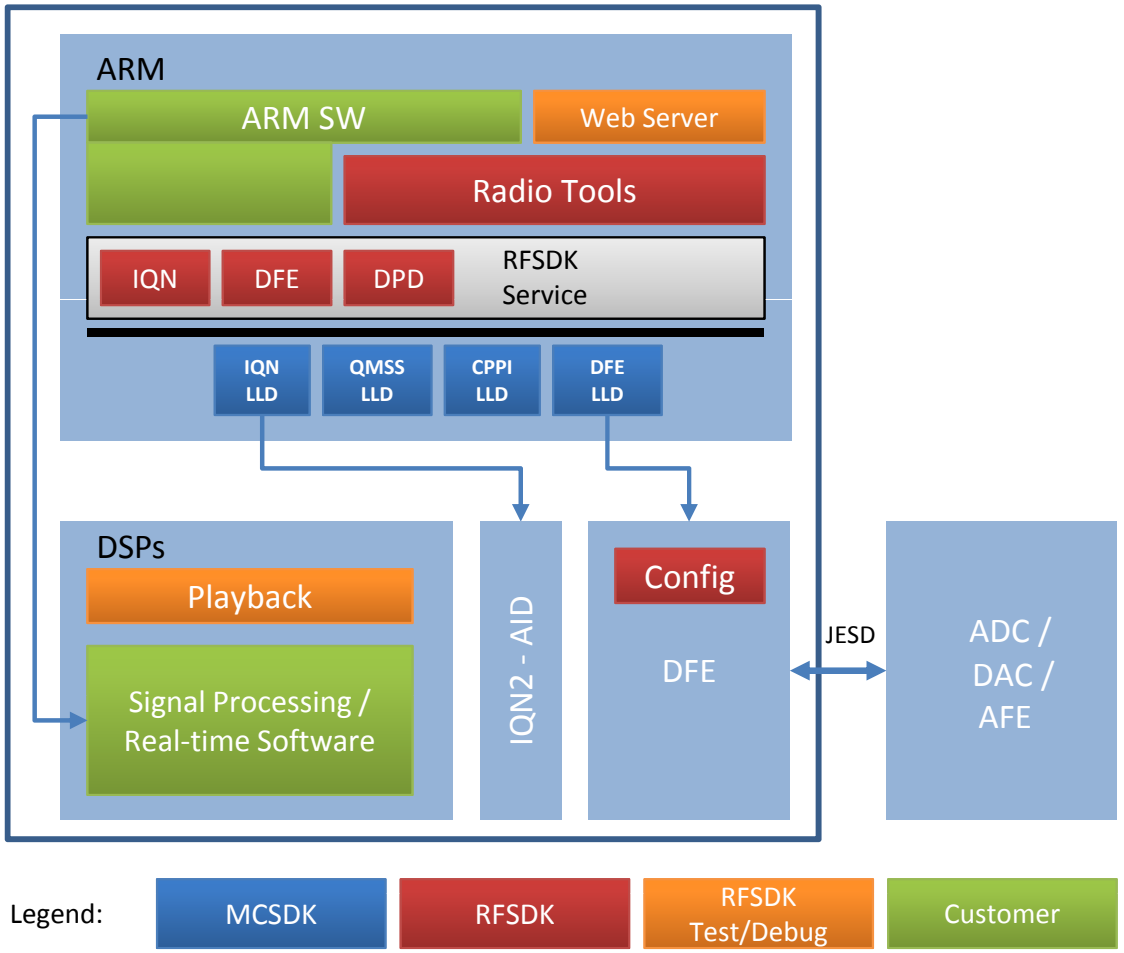


DFE Configuration

- The integrated DFE is configured using the RFSDK software provided by TI.
- RFSDK:
  - Runs on ARM/Linux
  - Uses TI-provided MCSDK Linux Dev Kit drivers to communicate with the hardware
  - Contains a set of pre-built radio configurations selectable by the customer
  - Provides set of APIs to start/stop operation and allow changing dynamic parameters (gain, etc.) during operation
  - Web server-based graphical interface for control and data visualization
- Data converters can also be configured from K2L device via I/O interfaces like SPI.

RFSDK Architecture

- RFSDK Radio Tools provide the top-level control interface.
- RFSDK Service performs actual control and configuration.
- Playback and Web Server provide RFSDK debug and test capabilities.



Get Started Today

Learn more:

- 66AK2Lx SoC Overview
- TI Design Page
- 66AK2L06 Product Folder
- SYS/BIOS and Linux-MCSDK for Keystone-II Devices