Processor SDK - Radar

Version 03.08.00

Release Notes
December 2019

Contents

Build ID: 03.08.00.00

IMPORTANT NOTE: Processor SDK Radar by default supports the TDA3xx, TDA2xx and TDA2px super set device configuration. Please refer to the Device Data Manual to know the details of the CPUs supported in that part. Processor SDK Radar supports selecting only the CPUs available for the specific part.

Major New Features in the Release

New features in the release vs previous Processor SDK Radar release are:

- None

Installation and Usage (BIOS ONLY)

- Kindly refer the user guide vision_sdk/docs/Radar/ProcessorSDKRadar_UserGuide.pdf

Example use-cases (BIOS ONLY)

- Processor SDK Radar demonstrates use-cases as examples. For the complete list of examples/usecases refer vision_sdk\docs\Radar\ProcessorSDKRadar_Usecases.xlsx

SDK Features

- Support the following SoC/Platforms
  - TDA3x SoC + AWR12 D3 RVP Board.
  - TDA3x SoC + FPDLink AWR12 D3 RVP Board.
  - TDA2x SoC ES1.1/ES2.0 (23x23) EVM
  - TDA2px SoC ES1.0 EVM
- Support for CPU's in the TDA3xx Device (IPU1-0, IPU1-1, DSP1, EVE)
  - Support for AR12xx Radar Sensor Data Capture
  - Support for Radar Processing Algorithm Plugin with sample Frame Copy Algorithm Function.
  - Support for Radar Processing Algorithm Plugin with FFT Algorithm Function and FFT Heat Map Draw Algorithm Functions.
  - Support for low latency inter-processor communication mechanism based on Work Queues (WorkQ).
  - EVE FFT, Peak detection and Beam forming algorithm integrated using WorkQ.
  - SD card based pre-recorded Radar Sensor ADC data read. (This feature is not supported on TDA3x modified EVM for AWR12 sensor integration with DIB and VAB)
  - SD card write of Algorithm processed output. (This feature is not supported on TDA3x modified EVM for AWR12 sensor integration with DIB and VAB)
  - Support for AWR12 Firmware Flash (on ALPS board)
  - Support for TI Fast Data Transfer Protocol (TFDTP) networking protocol.

- o Network (TCP/IP, TFDTP) based pre-recorded Radar Sensor ADC data read.
- o Network (TCP/IP, TFDTP) based write of Algorithm processed output.
- o Support for the TDA3xx RVP platform for direct connection of AWR12 with TDA3x CSI and single channel FPDLink based connection of AWR12 to TDA3xx.
- o Support for AWR12 advanced frame configuration, Dynamic Configuration of parameters to change the radar waveform properties.
- o Support for interpreting chirp profile data along with ADC data.
- o Support to read back programmed profile, chirp and frame configuration parameters.
- Support for CPU's in the TDA2xx Device (IPU1-0, IPU1-1, DSP1, EVE)
  - o Support for Radar Processing Algorithm Plugin with FFT Algorithm Function and FFT Heat Map Draw Algorithm Functions.
  - o Support for low latency inter-processor communication mechanism based on Work Queues (WorkQ).
  - o EVE FFT, peak detection and beam forming algorithm integrated using WorkQ.
  - o SD card based pre-recorded Radar Sensor ADC data read.
  - o SD card write of Algorithm processed output.
  - o Support for TI Fast Data Transfer Protocol (TFDTP) networking protocol.
  - o Network (TCP/IP, TFDTP) based pre-recorded Radar Sensor ADC data read.
  - o Network (TCP/IP, TFDTP) based write of Algorithm processed output.
- Support for TDA2px EVM using Network and File read and write of Radar Data.
- Support for Links Such as Dup, Merge, Select, Sync, NullSrc, Null and IPC (In/Out).
- Algorithm link with algorithm plug-in's support on all CPU's.
  - o Radar Process Algorithm Plugin which allows plugging in Algorithm Functions
  - o Sample Algorithm Function of Radar Frame Copy which copies the input frame data to output frame data.
  - o Radar FFT Algorithm Function which performs Range and Doppler FFT with work thread on EVE.
  - o Radar Peak detection CFAR-CA Algorithm with work thread on EVE.
  - o Radar Beam Forming Algorithm with work thread on EVE.
  - o Radar FFT Heat Map Draw, to display the FFT output data.
  - o Radar Object Draw algorithm to display the object detection output.
- Example usecases highlighting Radar Object Detection in terms of range, velocity and angle of arrival.
- Support for SPI communication to AWR12 over FPDLink Back Channel on the TDA3xx RVP setup.
- Support for multi-AWR12 radar configurations.
- Support for the Dynamic Chirp Configuration API for ES2.0/3.0 AWR1243.
- Support for Cascade Radar Board.
  - o Cascade Radar Data processing demonstration.
  - o DSP algorithms for second dimension, peak detection and angle of arrival detection.
- Driver support for Monitoring and run time calibration.
- Support for Radar System Planner to the documents section for offline analysis of TDA compute and bandwidth requirement.

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- Support for multi-channel processing as part of the Radar Algorithm Process.
- Linux Support for Processor SDK Vision for the Radar usecases. (Kindly use Processor SDK Vision package to access these features).
- PCIe based raw radar data capture and storage to SSD driver. (Kindly use Processor SDK Vision package to access these features).
- EVE 32-bit FFT integration for Doppler FFT processing for Cascade Radar.
- Upgrades to the Cascade Radar DSP based processing to support :
    - Different MIMO antenna configurations,
    - Beam forming based peak detection (angle information in case of beam forming not supported).
    - Support usecase create time selection of DSP or EVE based doppler FFT processing.
- Support for reading AWR1243 front end and algorithm parameters from a file residing in SD card without having to recompile the usecase for cascade radar parameter changes.
- Migrate DSP compiler version to ti-cgt-8.2.4.

Component Versions

The versions of the different components included in the Processor SDK Radar Package can be referred to at vision_sdk\docs\Radar\Processor_SDK_Radar_manifest.html

Validation Hardware

This software package is tested with the below hardware
- **TDA3xx, TDA2xx and TDA2px EVM**
    - Radar SD Card/Network Read and Write Usecase (Null Source Input + Radar FFT (EVE1) + Null output)
- **TDA3xx RVP + AWR1243 (Direct Connection & FPDLink)**
    - Radar (Single AWR1243) Capture + Radar FFT (EVE1) + Display (TDA3xx Only)
    - Satellite Radar (Single AWR1243) FPDLink Capture + Radar FFT (EVE1) + Display
- **TDA2xx 4 Chip AWR1243 Cascade Radar Board:**
    - Cascade Radar (4 AWR1243) Capture + Null (TDA2xx Only)
    - Cascade Radar (4 AWR1243) Capture + Radar Object Detect (DSP) + Null (TDA2xx Only)
- **Boot mode Supported**
    - TDA2x EVM: QSPI boot, SD boot, NOR boot, CCS boot
    - TDA3x EVM: QSPI boot, QSPI+SD boot (SBL in QSPI, AppImage in SD card), CCS boot
    - TDA3x RVP: QSPI boot, QSPI+SD boot (SBL in QSPI, AppImage in SD card), CCS boot

Refer user guide for exact board number and revision that this release is validated with.

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SW Quality – Status

Software Component	System Testing	MISRA - C *	Static analysis	Quality / Safety
SBL	Yes	Yes	Yes	TI SW Development process
CSL/FL / StarterWare	Yes	Yes	Yes	TI SW Development process
BSP / Drivers	Yes	Yes	Yes	TI SW Development process
EVE SW	Yes	Yes	Yes	TI SW Development process
VXLib (C66x)	Yes	Yes	Yes	TI SW Development process
NDK / NSP / AVB	Yes	Yes	Yes	TI SW Development process
IVAHD codecs	Yes	No	Yes	TI SW Development process
EDMA LLD	Yes	Yes	Yes	TI SW Development process
Framework Components	Yes	Yes	Yes	TI SW Development process
BIOS	Yes	Yes	Yes	TI SW Development process
BIOS-IPC	Yes	Yes	Yes	TI SW Development process
IPCLib	Yes	Yes	Yes	TI SW Development process
Links Framework‡	Yes	Yes	Yes	TI SW Development process
AutoSAR MCAL	Yes	Yes	Yes	ASIL – B

Processor SDK Radar/Vision Software Development Kit (Vision SDK) is broadly divided into
o **Core SDK Framework (links_fw)**
  o Core SDK – Contains Links and Chain Framework for both Bios and HLOS
  o SW quality processes like MISRA-C/KW static checker etc. are done only for links framework
o **Demo Application (apps)**
  o Demo applications to validate VSDK FW
  o SW quality processes like MISRA-C/KW static checker etc. are NOT done for apps and sample_app

Compilers	Production ready	Compiler Qualification Kit
EVE TI compiler	Yes	Available from TI
ARM M4 compiler	Yes	Available from TI
C66x TI compiler	Yes	Available from TI
ARM A15 compiler	Yes	3P

Bugs Fixed In This Release

Key	Summary	Description	Severity
ADASVISION-2621	Incorrect Cascade Radar Configuration in Example	In Cascade use case, the configuration example sets the following fields incorrectly. Bsp_Ar12xxConfigObj.ldoBypassCfgArgs.ldoBypassEnable should be 0x3, instead of 0x1. Bsp_Ar12xxConfigObj.calibEnArgs.calibEnMask should be 0x1ff0, instead of 0x0.	S3-Minor
ADASVISION-2718	TDA2x Cascade MIMO Point-Cloud Not Working	TDA2x Cascade MIMO Point-Cloud Not Working	S1-Critical

Known Issues / Limitations

Key	Summary	Description	Workaround	Severity	Affected Versions
ADASVISION-2218	CW streaming mode should be enabled in TDA2 capture software	CW streaming mode not enabled. Use ContStreaming Tab to configure CW mode. Use RadarStudio user guide. Trigger Slaves Trigger Master CSI2 data would not come with Frame end.	None	S3-Minor	VISION_SDK_03_07_00_00, VISION_SDK_03_07_00_01

Also refer to Process SDK Vision Release Notes for additional known issues.

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Compatibility Info

This section contains information about compatibility of APIs between this release and previous release.

NOTE: It is recommended to recompile the user created use-cases, alg plugins, links against the new release interface files even if no code level change is required in the user application.

Link API

Module	Interface file	Change in user application required	Change details
Algorithm Link	algorithmLink.h	No	Addition of algorithm ID for RGB algorithm. No impact on Processor SDK Radar.
Data Collect Link	dataCollectLink.h	Yes	New Parameters for number of frames to be captured and Captured file name prefix.
Display distribution Link	dispDistSrcLink.h	Yes	Added new parametes for DRM object type and ID. No impact on Processor SDK Radar.
System Link ID	system_linkId.h	No	Added support for dataCollect Links.