Processor SDK - Radar

Version 03.06.00

Release Notes
Dec 2018

Contents

IMPORTANT NOTES: <MUST READ>

- *This release is of Processor SDK Radar is focused on Radar Data Capture and Processing. Kindly do not use this for any Vision or Video Processing.*
- *CCS version 6.0.1.00040 or higher should be used along with Processor SDK Radar 3.06 release.*
- *BSP / Starterware is merged into single package – PDK Any reference to BSP/Starterware in the documentation refers to PDK.*

Build ID: 03.05.00.00

IMPORTANT NOTE: Processor SDK Radar by default supports the TDA3xx, TDA2xx and TDA2px super set device configuration. Please refer to the Device Data Manual to know the details of the CPUs supported in that part. Processor SDK Radar supports selecting only the CPUs available for the specific part.

Processor SDK Radar is based on the Vision SDK 03.06.00.00 release.
This is targeted for AWR12XX + TDA3xx and AWR12xx + TDA2xx Radar Data Processing and TDA2px Radar Data Processing.
Raw Data capture using PCIe is supported on Processor SDK Vision with Linux support. Kindly note the Processor SDK Radar supports only BIOS based usecases.

Major New Features in the Release

New features in the release vs previous Processor SDK Radar release are:

- Linux Support for Processor SDK Vision for the Radar usecases. (Kindly use Processor SDK Vision package to access these features).
- PCIe based raw radar data capture and storage to SSD driver. (Kindly use Processor SDK Vision package to access these features).
- EVE 32-bit FFT integration for Doppler FFT processing for Cascade Radar.
- Upgrades to the Cascade Radar DSP based processing to support :
    - Different MIMO antenna configurations,
    - Beam forming based peak detection (angle information in case of beam forming not supported).
    - Support usecase create time selection of DSP or EVE based doppler FFT processing.
- Support for reading AWR1243 front end and algorithm parameters from a file residing in SD card without having to recompile the usecase for cascade radar parameter changes.
- Migrate DSP compiler version to ti-cgt-8.2.4.

SDK Features (BIOS ONLY)

Installation and Usage (BIOS ONLY)

- Kindly refer the user guide vision_sdk/docs/Radar/ProcessorSDKRadar_UserGuide.pdf

Example use-cases (BIOS ONLY)

- Processor SDK Radar demonstrates use-cases as examples. For the complete list of examples/usecases refer vision_sdk\docs\Radar\ProcessorSDKRadar_Usecases.xlsx

SDK Features

- Support the following SoC/Platforms

    - TDA3x SoC + AWR12 D3 RVP Board.
    - TDA3x SoC + FPDLink AWR12 D3 RVP Board.
    - TDA2x SoC ES1.1/ES2.0 (23x23) EVM
    - TDA2px SoC ES1.0 EVM
- Support for CPU's in the TDA3xx Device (IPU1-0, IPU1-1, DSP1, EVE)
    - Support for AR12xx Radar Sensor Data Capture
    - Support for Radar Processing Algorithm Plugin with sample Frame Copy Algorithm Function.
    - Support for Radar Processing Algorithm Plugin with FFT Algorithm Function and FFT Heat Map Draw Algorithm Functions.
    - Support for low latency inter-processor communication mechanism based on Work Queues (WorkQ).
    - EVE FFT, Peak detection and Beam forming algorithm integrated using WorkQ.
    - SD card based pre-recorded Radar Sensor ADC data read. (This feature is not supported on TDA3x modified EVM for AWR12 sensor integration with DIB and VAB)
    - SD card write of Algorithm processed output. (This feature is not supported on TDA3x modified EVM for AWR12 sensor integration with DIB and VAB)
    - Support for AWR12 Firmware Flash (on ALPS board)
    - Support for TI Fast Data Transfer Protocol (TFDTP) networking protocol.
    - Network (TCP/IP, TFDTP) based pre-recorded Radar Sensor ADC data read.
    - Network (TCP/IP, TFDTP) based write of Algorithm processed output.
    - Support for the TDA3xx RVP platform for direct connection of AWR12 with TDA3x CSI and single channel FPDLink based connection of AWR12 to TDA3xx.
    - Support for AWR12 advanced frame configuration, Dynamic Configuration of parameters to change the radar waveform properties.
    - Support for interpreting chirp profile data along with ADC data.
    - Support to read back programmed profile, chirp and frame configuration parameters.
- Support for CPU's in the TDA2xx Device (IPU1-0, IPU1-1, DSP1, EVE)
    - Support for Radar Processing Algorithm Plugin with FFT Algorithm Function and FFT Heat Map Draw Algorithm Functions.
    - Support for low latency inter-processor communication mechanism based on Work Queues (WorkQ).
    - EVE FFT, peak detection and beam forming algorithm integrated using WorkQ.
    - SD card based pre-recorded Radar Sensor ADC data read.
    - SD card write of Algorithm processed output.
    - Support for TI Fast Data Transfer Protocol (TFDTP) networking protocol.
    - Network (TCP/IP, TFDTP) based pre-recorded Radar Sensor ADC data read.
    - Network (TCP/IP, TFDTP) based write of Algorithm processed output.
- Support for TDA2px EVM using Network and File read and write of Radar Data.
- Support for Links Such as Dup, Merge, Select, Sync, NullSrc, Null and IPC (In/Out).
- Algorithm link with algorithm plug-in's support on all CPU's.
    - Radar Process Algorithm Plugin which allows plugging in Algorithm Functions
    - Sample Algorithm Function of Radar Frame Copy which copies the input frame data to output frame data.

    - Radar FFT Algorithm Function which performs Range and Doppler FFT with work thread on EVE.
    - Radar Peak detection CFAR-CA Algorithm with work thread on EVE.
    - Radar Beam Forming Algorithm with work thread on EVE.
    - Radar FFT Heat Map Draw, to display the FFT output data.
    - Radar Object Draw algorithm to display the object detection output.
- Example usecases highlighting Radar Object Detection in terms of range, velocity and angle of arrival.
- Support for SPI communication to AWR12 over FPDLink Back Channel on the TDA3xx RVP setup.
- Support for multi-AWR12 radar configurations.
- Support for the Dynamic Chirp Configuration API for ES2.0/3.0 AWR1243.
- Support for Cascade Radar Board.
    - Cascade Radar Data processing demonstration.
    - DSP algorithms for second dimension, peak detection and angle of arrival detection.
- Driver support for Monitoring and run time calibration.
- Support for Radar System Planner to the documents section for offline analysis of TDA compute and bandwidth requirement.
- Support for multi-channel processing as part of the Radar Algorithm Process.

Component Versions

The versions of the different components included in the Processor SDK Radar Package can be referred to at vision_sdk\docs\Radar\Processor_SDK_Radar_manifest.html

Validation Hardware

This software package is tested with the below hardware

- **TDA3xx, TDA2xx and TDA2px EVM**
    - Radar SD Card/Network Read and Write Usecase (Null Source Input + Radar FFT (EVE1) + Null output)
- **TDA3xx RVP + AWR1243 (Direct Connection & FPDLink)**
    - Radar (Single AWR1243) Capture + Radar FFT (EVE1) + Display (TDA3xx Only)
    - Satellite Radar (Single AWR1243) FPDLink Capture + Radar FFT (EVE1) + Display
- **TDA2xx 4 Chip AWR1243 Cascade Radar Board:**
    - Cascade Radar (4 AWR1243) Capture + Null (TDA2xx Only)
    - Cascade Radar (4 AWR1243) Capture + Radar Object Detect (DSP) + Null (TDA2xx Only)
- **Boot mode Supported**
    - TDA2x EVM: QSPI boot, SD boot, NOR boot, CCS boot
    - TDA3x EVM: QSPI boot, QSPI+SD boot (SBL in QSPI, AppImage in SD card), CCS boot
    - TDA3x RVP: QSPI boot, QSPI+SD boot (SBL in QSPI, AppImage in SD card), CCS boot

Refer user guide for exact board number and revision that this release is validated with.

SW Quality – Status

Software Component	System Testing	MISRA - C *	Static analysis	Quality / Safety
SBL	Yes	Yes	Yes	TI SW Development process
CSL/FL / StarterWare	Yes	Yes	Yes	TI SW Development process
BSP / Drivers	Yes	Yes	Yes	TI SW Development process
EVE SW	Yes	Yes	Yes	TI SW Development process
VXLib (C66x)	Yes	Yes	Yes	TI SW Development process
NDK / NSP / AVB	Yes	Yes	Yes	TI SW Development process
IVAHD codecs	Yes	No	Yes	TI SW Development process
EDMA LLD	Yes	Yes	Yes	TI SW Development process
Framework Components	Yes	Yes	Yes	TI SW Development process
BIOS	Yes	Yes	Yes	TI SW Development process
BIOS-IPC	Yes	Yes	Yes	TI SW Development process
IPCLib	Yes	Yes	Yes	TI SW Development process
Links Framework‡	Yes	Yes	Yes	TI SW Development process
AutoSAR MCAL	Yes	Yes	Yes	ASIL – B

‡ Processor SDK Radar/Vision Software Development Kit (Vision SDK) is broadly divided into

- **Core SDK Framework (links_fw)**
  - Core SDK – Contains Links and Chain Framework for both Bios and HLOS
  - SW quality processes like MISRA-C/KW static checker etc. are done only for links framework
- **Demo Application (apps)**
  - Demo applications to validate VSDK FW
  - SW quality processes like MISRA-C/KW static checker etc. are NOT done for apps and sample_app

Compilers	Production ready	Compiler Qualification Kit
EVE TI compiler	Yes	Available from TI
ARM M4 compiler	Yes	Available from TI
C66x TI compiler	Yes	Available from TI
ARM A15 compiler	Yes	3P

Bugs Fixed In This Release

JIRA ID	Description	Severity	Affects Version/s
ADASVISION-2040	[RADAR] CSI Capture is in correct as the output container format is not set to 16 bits	S2-Major	VISION_SDK_03_05_00_00
ADASVISION-2015	[RADAR] Chains_radarunittest_programTestConfig does not have a break statement for advanced frame type	S3-Minor	VISION_SDK_03_05_00_00

Known Issues / Limitations

JIRA ID	Description	Severity	Workaround	Affects Version/s
ADASVISION-1882	Radar FFT and TIDL OD algorithm Links can't share the same EVE	S3-Minor	No	VISION_SDK_03_04_00_00, VISION_SDK_03_05_00_00
ADASVISION-1885	[Radar][Network] Network transmission fails when running only IPU1_0 and IPU1_1 on Cascade Radar EVM	S3-Minor	Enable any other cores	VISION_SDK_03_04_00_00, VISION_SDK_03_05_00_00

Also refer to Process SDK Vision and PDK Release Notes for additional known issues.

Compatibility Info

This section contains information about compatibility of APIs between this release and previous release.

NOTE: It is recommended to recompile the user created use-cases, alg plugins, links against the new release interface files even if no code level change is required in the user application.

Link API

Module	Interface file	Change in user application required	Change details
Data Collect Link	dataCollectLink.h	No	[New File] Defines the interfaces for the dummy terminating link.
Algorithm Link	algorithmLink.h	No	Addition of algorithm ID for TIOP algorithm running on DSP. Change not influencing Processor SDK Radar.
Autosar IPC Link	Autosar_ipcLink.h	No	New Macro for AUTOSAR IPC initialization. New structures for shared memory for AUTOSAR. Change not influencing Processor SDK Radar.
ISS M2M ISP Link	issM2mIspLink.h	No	Addition of resizer buffer alignment. Change not influencing Processor SDK Radar.
ISS M2M Resizer Link	issM2mResizerLink.h	No	Addition of resizer buffer alignment. Change not influencing Processor SDK Radar.
System Interlink API	system_inter_link_api.h	No	Updated IPC and Meta buffer structure. Change not influencing Processor SDK Radar.
System IPC	system_ipc_if.h	No	New structure member for AUTOSAR IPC initialization. Change not influencing Processor SDK Radar.