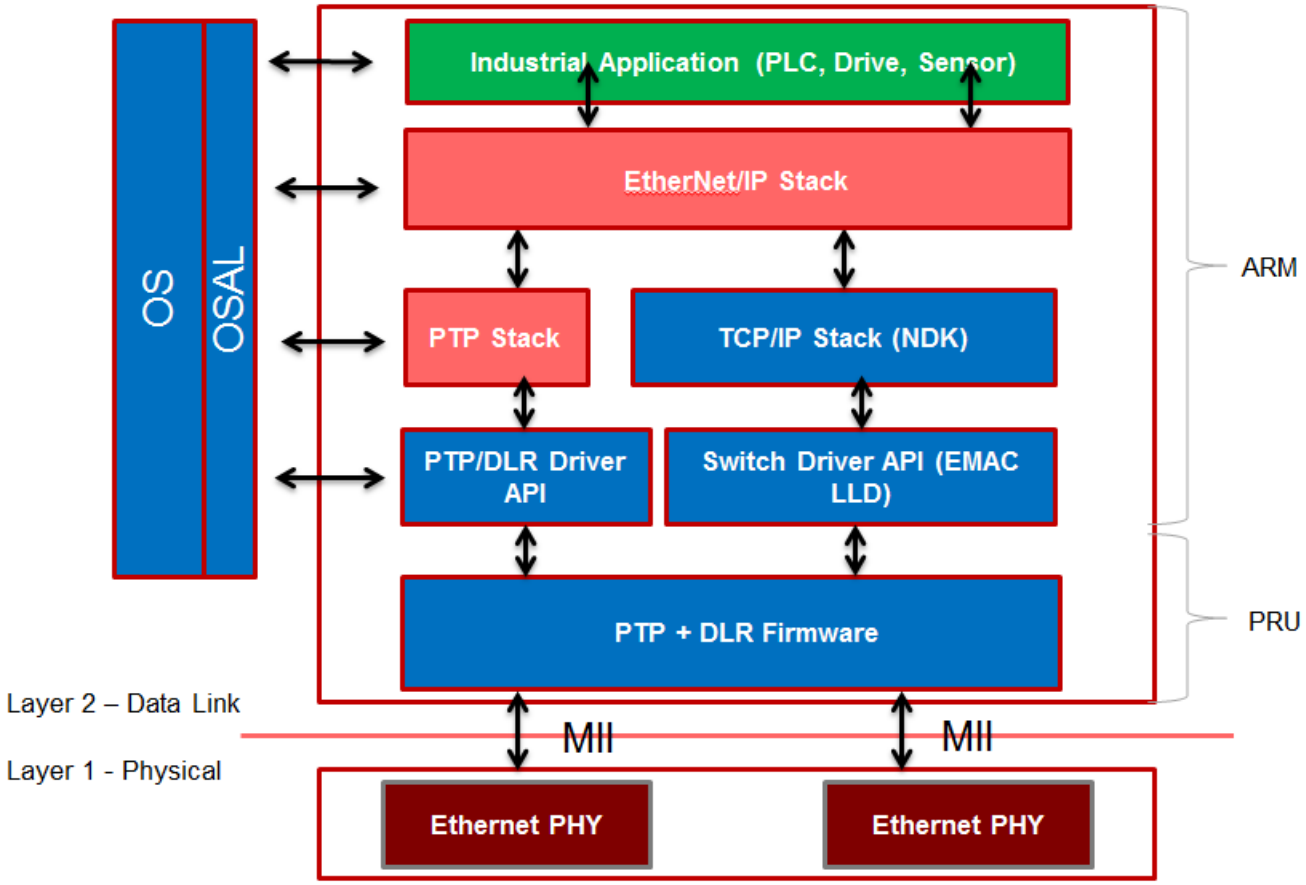
PRU-ICSS EtherNet/IP Adapter Firmware Data Sheet

FEATURES

- EtherNet/IP Adapter is compliant to Conformance Tool 15 from ODVA
- Declaration of Conformity [DOC] from ODVA with interoperability stamp*.
- Min RPI of 1ms
- Integrated two-port cut-through switch
  - 100 Mbps, 10Mbps
  - Full Duplex, Half Duplex
- Quality of Service (QoS)
  - Four priority receive queues on host port, each queue 6 KB in size
  - Four priority transmit queues on each physical port, each queue 3 KB in size
- Total CIP Connections - 9
  - IO Messaging – 6
  - Explicit Messaging - 3
- DLR – Device Level Ring
  - 100us beacon interval
  - 200us beacon timeout
  - Self-Configuring
- ACD support
- PTP/1588 – Time Synchronization
  - E2E mode supported
  - CIP Sync capable
  - Transparent and Ordinary Clock
- 1 ms buffering per port
- 802.1d learning bridge for received source MAC addresses
  - 1024 addresses per port
  - API's for port state configuration and flushing learning table upon change in network topology
  - Switch address learned table (FDB) is flushed in 2.4 us
- Multicast and Broadcast storm prevention per port
- API's to store configuration parameters in non-volatile memory
- Interrupt for Link loss detection.
  - Link loss detection in under 200us
  - Callback API's to perform tasks related to change in network topology
- Statistics
  - Media counters supported per port
  - Interface counters supported per port
- Learning/FDB : Yes
  - 1024 entries per port
  - Learning table on DDR
- Support for Multicast Filtering
  - Supported on all SoCs
  - Hash Table for faster lookup
  - O(1) complexity

Description

PRU-ICSS EtherNet/IP firmware implements EtherNet/IP + PTP + DLR functionality and provides EtherNet/IP ASIC like functionality integrated into AM335x, AM437x and AM57x class of devices. PRU-ICSS EtherNet/IP software from TI can be used by customers to add EtherNet/IP function on top of Processor SDK to Sitara processors.



When referring to EtherNet/IP we refer to the layer on top of TCP/IP layer. This can be implemented on the standard switch firmware and does not require any special driver support. The additional features in firmware and driver are PTP and DLR. When referring to the EtherNet/IP driver we refer to the standard switch driver and PTP and DLR driver layers.

EtherNet/IP firmware for PRU-ICSS is a black box product maintained by TI. EtherNet/IP driver allows loading and run EtherNet/IP firmware and interface with the firmware.

EtherNet/IP Driver is provided in full source so that customers can adapt this implementation to own hardware and Operating Systems. This driver provides stack interface for queue management, Rx, Tx, PTP Configuration, DLR management, interfacing PTP and EIP stack.

Operating System, Switch Driver (ICSS EMAC LLD), TCP/IP Stack (NDK) and associated documentation is available through Processor SDK. See Software section for details

Performance Summary

A 300 MHz CPU speed is sufficient to support a simple IO or sensor application. More complex applications can use higher speed grades of up to 1.5 GHz. The PRU core speed remains 200 MHz for all speed grades.

Memory Summary

This section describes memory usage of the EtherNet/IP PRU-ICSS firmware and Cortex-A driver.

Table 1 EtherNet/IP PRU-ICSS Firmware Memory Statistics

Memory	Program memory (AM3 Family)	Program memory (AM5 Family)	Data memory	Remarks
L3 OCMC RAM	NA	NA	54272 bytes	Receive and Transmit Queues

NOTE: Driver object files () used for this analysis with gcc-arm-none-eabi-4_8-2014q3 toolchain options : -mcpu=cortex-a8 -mtune=cortex-a8 -marm –mfloat-abi=hard -mfpu=neon -O2

Hardware Requirements

- Sitara Processor with PRU-ICSS IP and EtherNet/IP support
- EtherNet/IP implementation uses following interrupts mapped to Host Interrupt Controller

Stack/application interrupts		
Firmware interrupt	**Host Interrupt**	**Remarks**
Frame Receive	PRU_ICSS_EVTOUT0	Notifies host when firmware has stored a frame in host receive queue
DLR Port 0 Interrupt	PRU_ICSS_EVTOUT1	Raised when there is a state change in DLR on Port 0
DLR Port 1 Interrupt	PRU_ICSS_EVTOUT2	Raised when there is a state change in DLR on Port 1
Tx Callback Interrupt	PRU_ICSS_EVTOUT3	Raised when a PTP/1588 frame which requires Tx Timestamping is sent out
DLR Beacon Timeout Interrupt for Port 0	PRU_ICSS_EVTOUT4	Raised when the beacon timeout timer on Port 0 expires
DLR Beacon Timeout Interrupt for Port 1	PRU_ICSS_EVTOUT7	Raised when the beacon timeout timer on Port 1 expires
Link 0	PRU_ICSS_EVTOUT6	Interrupt is raised when the Link on MII0 port comes up or goes down
Link 1	PRU_ICSS_EVTOUT6	Interrupt is raised when the Link on MII1 port comes up or goes down

- EtherNet/IP implementation makes use of one channel of EDMA for PTP implementation
- HW signals required to implement EtherNet/IP adapter functionality is shown below, this info needs to be used in conjunction with http://www.ti.com/tool/PINMUXTOOL

NOTE: w.r.t prX, X is 1 or 2 (respectively PRU-ICSS1 and PRU-ICSS2 – refer to SOC TRM for availability)

Table 2 PRU-ICSS signals required for EtherNet/IP functionality

Signal name		Description
PRU-ICSS MDIO		
prX_mdio_mdclk	Mandatory	MDIO clock
prX_mdio_data	Mandatory	MDIO data
PRU-ICSS MII PORT0 **PRU-ICSS MII PORT1**		
prX_mii_mt0_clk	Mandatory	MII0 and MII1 transmit clock
prX_mii_mt1_clk		
prX_mii0_txd3	Mandatory	MII0 and MII1 transmit data3
prX_mii1_txd3		
prX_mii0_txd2	Mandatory	MII0 and MII1 transmit data2
prX_mii1_txd2		
prX_mii0_txd1	Mandatory	MII0 and MII1 transmit data1
prX_mii1_txd1		
prX_mii0_txd0	Mandatory	MII0 and MII1 transmit data0
prX_mii1_txd0		
prX_mii0_rxd3	Mandatory	MII0 and MII1 receive data3
prX_mii1_rxd3		
prX_mii0_rxd2	Mandatory	MII0 and MII1 receive data2
prX_mii1_rxd2		
prX_mii0_rxd1	Mandatory	MII0 and MII1 receive data1
prX_mii1_rxd1		
prX_mii0_rxd0	Mandatory	MII0 and MII1 receive data0
prX_mii1_rxd0		
prX_mii0_txen	Mandatory	MII0 and MII1 TX enable
prX_mii1_txen		
prX_mii_mr0_clk	Mandatory	MII0 and MII1 receive clock
prX_mii_mr1_clk		
prX_mii0_rxdv	Mandatory	MII0 and MII1 RX data valid
prX_mii1_rxdv		
prX_mii0_rxer	Mandatory	MII0 and MII1 RXERR
prX_mii1_rxer		
prX_mii0_rxlink	Optional	For fast link loss detection - connect LED_LINK/LED_SPEED from PHY here and enable MLINK mode in MDIO
prX_mii1_rxlink		
prX_mii0_crs	Optional	Required to enable half duplex support on MII0
prX_mii0_col		
prX_mii1_crs	Optional	Required to enable half duplex support on MII1
prX_mii1_col		
PRU-ICSS PTP/1588 Clocks (Network clock synchronization)		
prX_edc_sync0_out	Recommended (for PTP/1588 capable slaves)	SYNC0 out - Time synchronized OUT0

Certification Information

Certification was done on AM335x ICEv2 board on EtherNet/IP firmware using Industrial SDK 1.1.0.5 release as the base in July 2014.

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This Declaration of Conformity is issued on October 13, 2014, on behalf of ODVA by:

Katherine Voss
Executive Director

Vendor Information	
Vendor Name	Texas Instruments

Test Information	
Test Date	May 15, 2014
Composite Test Revision	CT11
ODVA File Number	11290.01

Product Information	**Network Category: Node**
Identity Object Instance	
Vendor ID (Attribute 1)	806
Device Type (Attribute 2)	0x0C
Device Profile Name	Communications Adapter

Products Covered under this Declaration of Conformity (Identity Object Instance)

No.	Product Code (Attribute 3)	Product Name (Attribute 7)	Product Revision (Attribute 4)	SOC File Name
1	1026	TI/Molex EIP Adapter	1.001	TI_EIP_ICSS_Adapter.stc

References

1. EtherNet/IP on Sitara Processors – spry249
2. Industrial Communications Solution Guide - slyy050b
3. EtherNet/IP Communications Development Platform
4. Certified EtherNet/IP Adapter device
5. Molex EtherNet/IP Stack
6. EtherNet/IP Developer Guide

Acronyms

Acronym	Description
AL	Application Layer
ASIC	Application Specific Integrated Circuit
AM3 family	Implies AM3x, AM4x, AMIC110x class of devices because they use identical firmware
AM5 family	Implies AM57x, K2G class of devices because they use identical firmware
DL	Datalink Layer
DLR	Device Level Ring
DOC	Declaration of Conformity (certification from ODVA)
EDMA	Enhanced Direct Memory Access
FDB	Forwarding Data Base
ISR	Interrupt Service Routine
MDIO	Management Data Input Output
MII	Media Independent Interface
ODVA	Open Device Vendors Association (Standards body for EtherNet IP)
OS	Operating Systems
PRUSS	Programmable RealTime Unit Sub System
PRU-ICSS	Programmable RealTime Unit - Industrial Communication Sub System - PRUSS with industrial communication support
PTP-1588	Precision Time Protocol (IEEE time synchronization protocol)
RPI	Requested Packet Interval

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