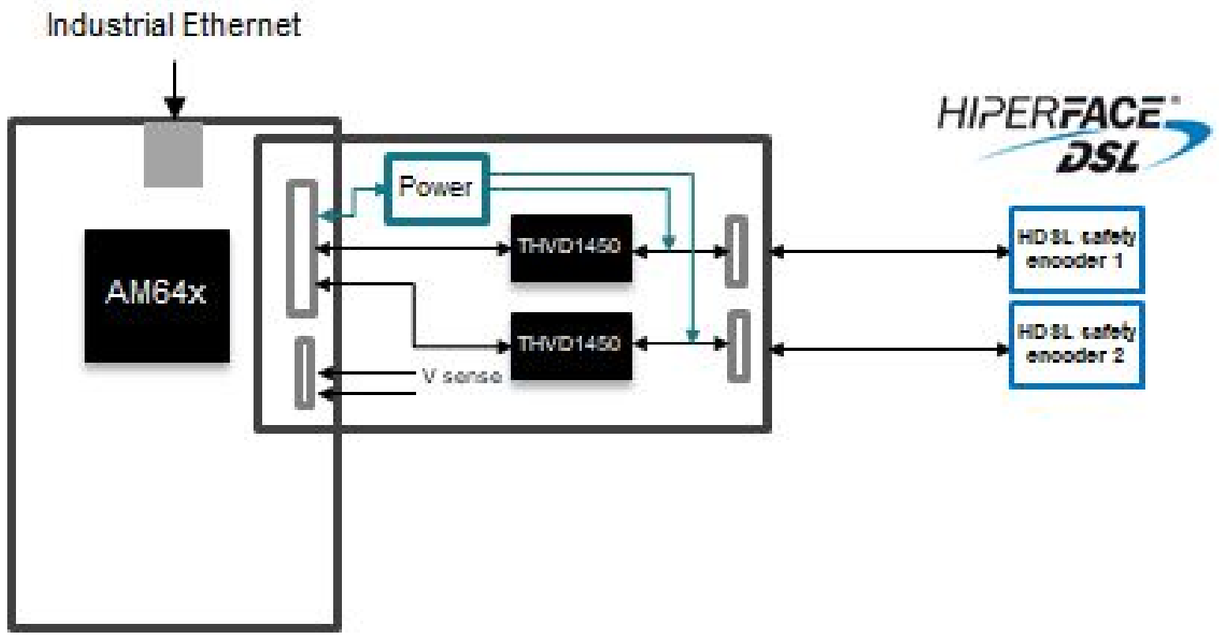
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



!!! With this board the Gigabit Ethernet PHY connected to the single RJ45 connector (DP83867) becomes unusable

		2 out of 6 channel HDSL interface mapping - ICSS_G0				
	Slice 0 RTU0	pin name	AM64x pin	HSE connector	comment	
	in	PRG0_PRU0_GPO9	w6	J2D - D28	indirect over mux	**Ethernet DP83867**
channel 1	out	PRG0_PRU0_GPO1	r4	J2E - E8	direct	
	out_en	PRG0_PRU0_GPO2	u2	J2A - A8	direct	
	PRU0					
	in	PRG0_PRU0_GPO10	aa5	J2B - B29	indirect over mux	**Ethernet DP83867**
channel 2	out	PRG0_PRU0_GPO4	aa2	J2A - A13	direct	
	out_en	PRG0_PRU0_GPO5	r3	J2C - C6	direct	
	TX_PRU0					
	in	PRG0_PRU0_GPO11	y3	J2B - B14	direct	
channel 3	out	PRG0_PRU0_GPO7	t1	J2B - B2	direct **Should be B7**	
	out_en	PRG0_PRU0_GPO8	t2	J2A - A7	direct	
	Slice 1 RTU0					
	in	PRG0_PRU1_GPO9	y5	J2E - E23	indirect over mux	**Ethernet DP83867**
channel 4	out	PRG0_PRU1_GPO1	w2	J2A - A13	direct **Should be A11**	
	out_en	PRG0_PRU1_GPO2	v3	J2D - D9	direct	
	PRU0					
	in	PRG0_PRU1_GPO10	v6	J2E - E27	indirect over mux	**Ethernet DP83867**
channel 5	out	PRG0_PRU1_GPO4	w3	J2B - B13	direct	
	out_en	PRG0_PRU1_GPO5	p4	J2D - D6	direct	
	TX_PRU0					
	in	PRG0_PRU1_GPO11	w4	J2D - D11	direct	
channel 6	out	PRG0_PRU1_GPO7	w5	J2D - D23	indirect over mux	**Ethernet DP83867**
	out_en	PRG0_PRU1_GPO8	r1	J2B - B4	direct	
					note: indirect goes over TS3DDR3812 with 3.3V VCC	

Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 2/22/2021
TID #: N/A	Project Title: Hiperface DSL 2 Channel Interface	
Number: HDSL_AM64x Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 5
Drawn By:	File: CoverSheet.SchDoc	Size: B
Engineer: Ingolf FRank	Contact: http://www.ti.com/support	

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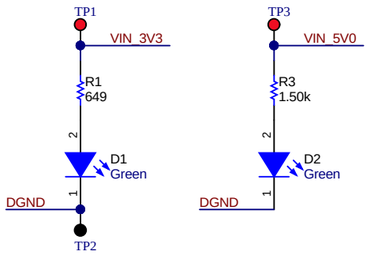
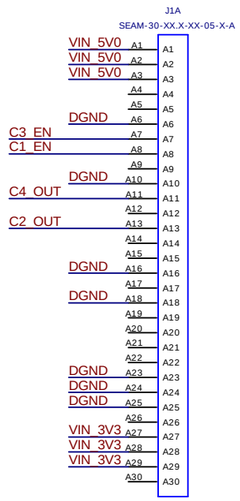
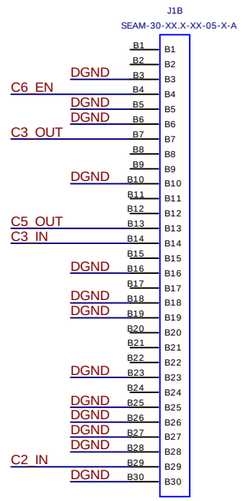
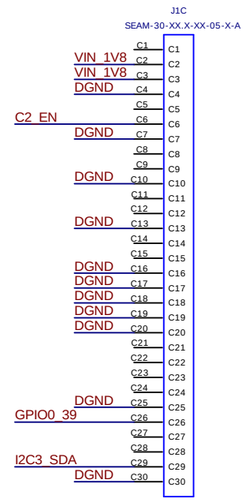
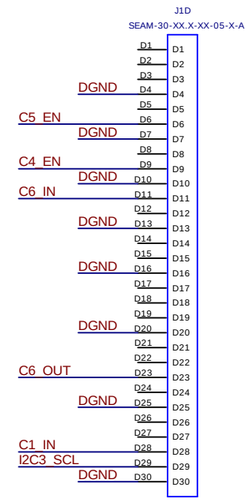
Connectors, Voltage Supervision and Board ID

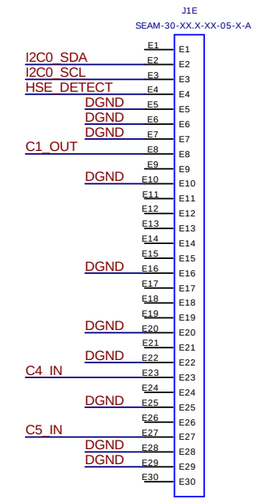


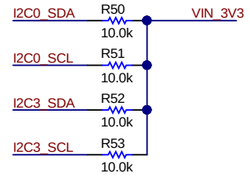


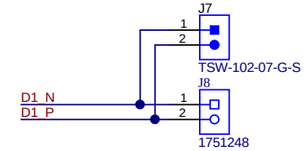


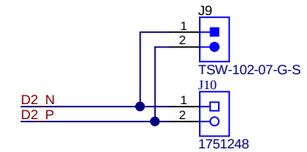


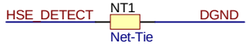


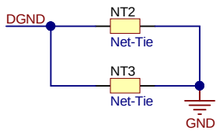










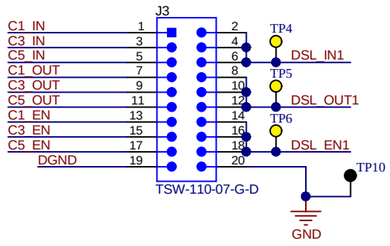


Channel Mapping

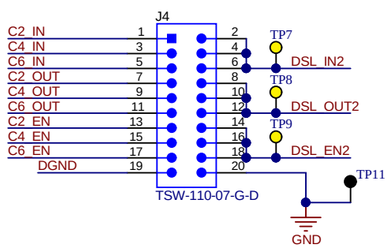
PRG0:
Slice 0
C1 - Channel 1 RTU0
C2 - Channel 2 PRU0
C3 - Channel 3 TX_PRU0

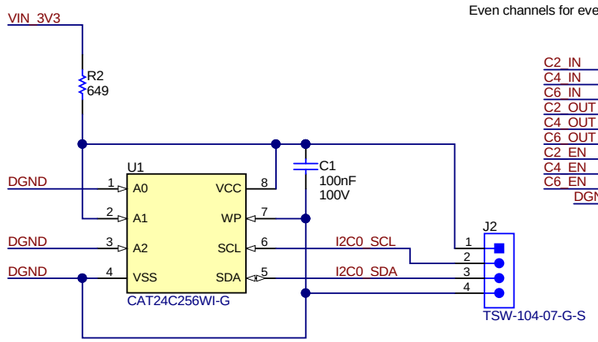
Slice 1
C4 - Channel 4 RTU0
C5 - Channel 5 PRU0
C6 - Channel 6 TX_PRU0

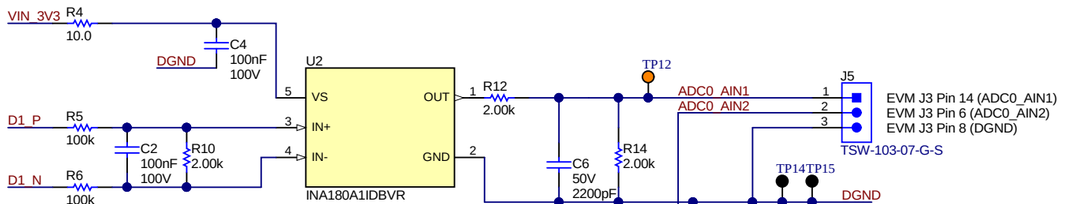
Odd channels for odd data output

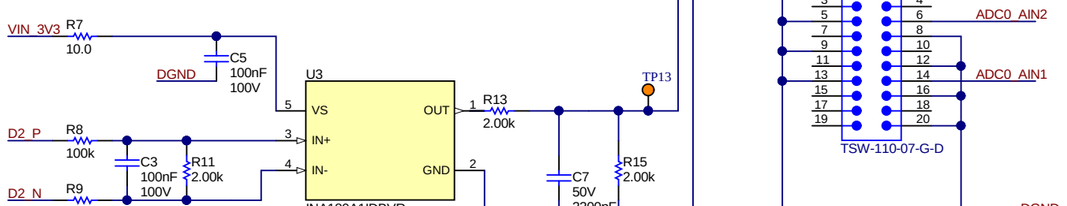


Even channels for even data output









Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 3/6/2021
TID #: N/A	Project Title: Hiperface DSL 2 Channel Interface	
Number: HDSL_AM64x Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 5
Drawn By:	File: Connectors.SchDoc	Size: B
Engineer: Ingolf FRank	Contact: http://www.ti.com/support	

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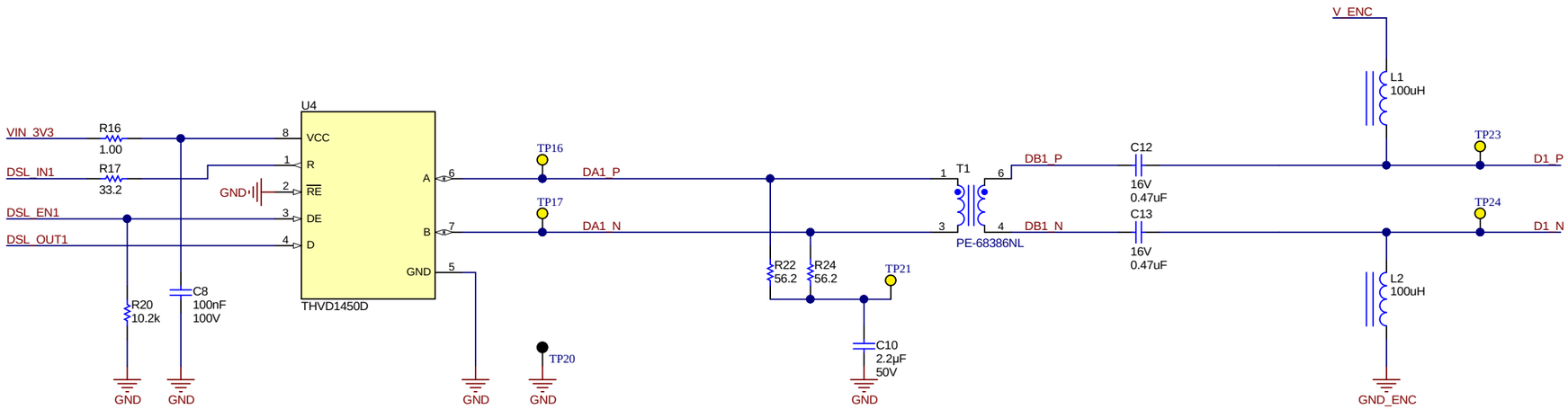
Communication Interfaces



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TID #: N/A	Project Title: Hiperface DSL 2 Channel Interface	
Number: HDSL_AM64x Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 5
Drawn By:	File: Communication.SchDoc	Size: B
Engineer: Ingolf FRank	Contact: http://www.ti.com/support	

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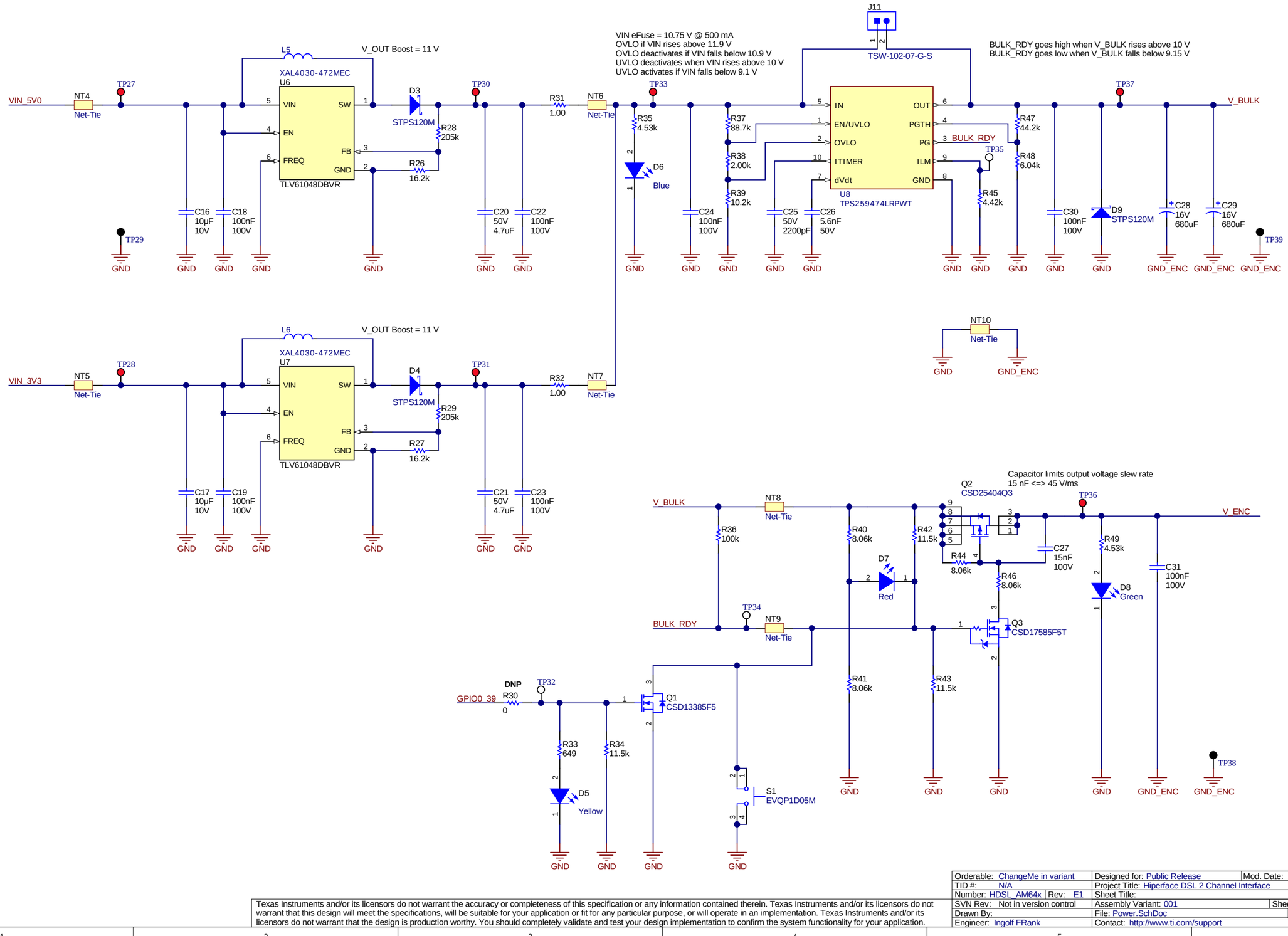
Power supplies, protection and load switches for two encoders



Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 3/5/2021
TID #: N/A	Project Title: Hiperface DSL 2 Channel Interface	
Number: HDSL_AM64x | Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 5
Drawn By:	File: Power.SchDoc	Size: B
Engineer: Ingolf FRank	Contact: http://www.ti.com/support	

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H1
1
NY PMS 440 0025 PH

H2
1
NY PMS 440 0025 PH

FID1 FID2 FID3

PCB Number: HDSL_AM64x
PCB Rev: E1

Logo1
PCB
LOGO
Texas Instruments

Logo2
CE Mark

Logo3
PCB
LOGO
FCC disclaimer

Logo4
PCB
LOGO
WEEE logo

Variant/Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Number: HDSL_AM64x Rev: E1	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 5 of 5
Drawn By:	File: Hardware.SchDoc	Size: B
Engineer: Ingolf FRank	Contact: http://www.ti.com/support	

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