



Release version: 00.05.01.00

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Algorithm	Algorithm Configuration	Processor	Processor Configuration	Cycle Per API Call
tiadalg_image_preprocessing (Creates 3 planes of planner RGB data for deep learning processing)	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x16</li> <li>• <b>Color conversion</b> : YUV420 nv12 to RGB planner (3 separate plane for B , G &amp; R)</li> <li>• <b>No Mean subtraction and scaling</b></li> </ul>	C66x	*common processor configuration	18K
	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x16</li> <li>• <b>Color conversion</b> : YUV420 nv12 to BGR planner (3 separate plane for B , G &amp; R)</li> <li>• <b>No Mean subtraction and scaling</b></li> </ul>	C66x	*common processor configuration	17K
	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x16</li> <li>• <b>Color conversion</b> : RGB interleaved to RGB planner (3 separate plane for R , G &amp; B)</li> <li>• <b>No Mean subtraction and scaling</b></li> </ul>	C66x	*common processor configuration	36K
	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x16</li> <li>• <b>Color conversion</b> : RGB interleaved to BGR planner (3 separate plane for B , G &amp; R)</li> <li>• <b>No Mean subtraction and scaling</b></li> </ul>	C66x	*common processor configuration	37K
tiadalg_image_color_blending (Color blending of input image for pixel level detection by semantic segmentation task or other similar task)	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x384</li> </ul>	C66x	*common processor configuration + Input and output present in cached DDR	1.2 Mega Cycle
tiadalg_fisheye_transformation (Transforms list of points from fish eye to rectilinear image)	<ul style="list-style-type: none"> <li>• <b>Number of Points</b> : 8</li> </ul>	C66x	*common processor configuration	330



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tiadalg_dof_plane_seperation (Creates 3 RGB plane data to be fed to deep learning network from packed flow data generated from DMPACK h/w accelerator)	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x384</li> </ul>	C66x	*common processor configuration + Input and output present in cached DDR	2.94 Mega Cycle
	<ul style="list-style-type: none"> <li>• <b>Image resolution</b> : 768x16</li> </ul>	C66x	*common processor configuration	30K
tiadalg_select_top_feature (Matching of list of 64 element descriptors, and finding top matches with 2-way consistency check)	<ul style="list-style-type: none"> <li>• <b>Number of current feature</b> : 187</li> <li>• <b>Number of map features</b>: 2619</li> <li>• <b>Descriptor size</b>: 64 int16</li> </ul>	C66x	*common processor configuration	10.8 Mega Cycle
	<ul style="list-style-type: none"> <li>• <b>Number of current feature</b> : 187</li> <li>• <b>Number of map features</b>: 2619</li> <li>• <b>Descriptor size</b>: 64 int8</li> </ul>	C66x	*common processor configuration	7.1 Mega Cycle
tiadalg_solve_pnp (Camera pose estimation from p3p technique)	<ul style="list-style-type: none"> <li>• <b>Number of points pair</b> : 50</li> <li>• <b>Number of RANSAC iteration</b> : 200</li> </ul>	C66x	*common processor configuration + 2d and 3d points are in L2 memory	4.95 Mega Cycle
tiadalg_sparse_upsampling (sparse up sampling of data and later 7x7 convolution)	<ul style="list-style-type: none"> <li>• <b>Number of sparse feature points</b>: 575</li> <li>• <b>Output descriptor in 16 bit</b></li> </ul>	C66x	*common processor configuration	1.07 Mega Cycle
tiadalg_visual_localization (Given the list of key points, and their descriptor, current frame location is estimated with the help of fixed map data at create time)	<ul style="list-style-type: none"> <li>• <b>Number of current Frame feature points</b> : 300</li> <li>• <b>Number of Map feature</b> : 7.5K</li> <li>• <b>Number of points pair for solvePnP</b>: 50</li> <li>• <b>Number of RANSAC iteration for solvePnP</b>: 200</li> </ul>	C66x	*common processor configuration	~ 44 Mega Cycle

\*Common Processor configuration

- Input and output in L2 internal memory (IF not mentioned explicitly)

- **Stack in L2 memory**
- **L1D 32 KB cache**
  - L2D 128 KB cache

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