

H.264 High Profile Encoder (v01.00.00) on DM365

FEATURES

- eXpressDSP[™] Digital Media (XDM 1.0 IVIDENC1) interface compliant
- Validated on DM365 EVM
- H.264 High Profile up to level 3.1 compliant
- Resolutions up to 720p(1280 x 720) supported
- YUV420 semi-planar input format for the frames supported
- Progressive and interlaced encoding supported
- Generates bit-stream compliant with H.264
 standard
- CAVLC and CABAC encoding supported
- 16x16, 8x16, 16x8, and 8x8 MB partition supported
- Sequence scaling matrix is supported
- Transform 8x8 and transform 4x4 is supported
- Frame based encoding with frame size being multiples of 2 supported
- Rate Control (CBR and VBR) supported
- Insertion of Buffering Period and Picture Timing Supplemental Enhancement Information (SEI) and Video Usability Information (VUI) supported
- Unrestricted Motion Vectors (UMV) supported
- Half pel and quarter pel interpolation for motion estimation supported
- Supported features in high quality mode:
 - TI's proprietary motion estimation supported (2 types of search algorithms supported
 - All 16x16, 8x8, and 4x4 Intra-Prediction Modes supported
 - Multiple slice encoding supported upto 720p resolution (for CAVLC only)
 - 4-motion vector per macroblock till 720p

resolution supported

- Adaptive Intra Refresh (AIR) supported
- Supported features in standard quality mode:
 - TI's proprietary motion estimation supported (low power ME supported)
 - All 16x16, 8x8, and 4x4 intra-prediction Modes supported in I-Frame and INTRA16x16 DC is supported in P-frames
 - Only single slice per frame is supported
 - Only single motion vector per macroblock supported
- This encoder does not support the following features:
 - Error resilience features such as ASO/FMO and redundant slices
 - Adaptive reference picture marking
 - Reference picture list reordering

DESCRIPTION

H.264 (from ITU-T, also called as H.264/AVC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H.264 standard defines several profiles and levels which specify restrictions on the bit stream and hence limits the capabilities needed to decode the bit streams. This project is developed using Code Composer Studio version 3.3.81.6 and using the code generation tools version 4.1.3.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

eXpressDSP is a trademark of Texas Instruments. Linux is a registered trademark of Linus Torvalds.

Monta Vista is a registered trademark of MontaVista Software, Inc. All other trademarks are the property of their respective owners.

Performance Summary

This section describes performance of Standalone H.264 Encoder validated on DM365 EVM.

Table 1. Configuration Table

CONFIGURATION	ID
H.264 High profile levels up to 3.1, UMV – OFF, PRC – ON, T8x8Inter – OFF and T8x8Intra – ON, SM – ON, CABAC – ON, Quality – Standard Quality, IntraPeriod-30	H264_ENC_01
H.264 High profile levels up to 3.1, UMV – OFF, PRC – ON, T8x8Inter – ON and T8x8Intra – ON, SM – ON, Quality – High Quality, MeAlgo = 1, IntraPeriod-30	H264_ENC_02

Performance Measurement Procedure

- Measured with program memory and I/O buffers in external memory, I/D cache enabled, ARM @297 MHz, HDVICP @243 MHz, DDR @243 MHz, Monta Vista[®] Linux[®] 5.0
- Linux is used to measure the performance numbers in this Datasheet.
- The process time is measured across algActivate/process/algDeactivate function call using gettimeofday() utility of Linux.
- NFS File system is used as an environment in performance measurement.

	PERFORMANC	RFORMANCE STATISTICS FOR STANDARD QUALITY SETTINGS (MEGA CYCLES) ⁽¹⁾						
			AVERAGE			PEAK		
INPUT NAME	RESOLUTION	ARM926 PER FRAME	ENCODE PER FRAME (ARM926 and ARM968)	FPS	ARM926 PER FRAME	ENCODE PER FRAME (ARM926 and ARM968)	FPS	
parkrun_p1280x720_30fps_420pl_300fr.yu v	720p@30fps, 4mbps	0.31	9.02	33.27	0.29	11.79	25.44	
shields_p720x480_25fps_420pl_252fr.yuv	D1@30fps, 2mbps	0.27	3.67	81.73	0.29	4.72	63.55	
foreman_i640x480_30fps_420pl_300fr .yuv	VGA @30fps, 3mbps	0.27	3.27	91.71	0.27	4.18	71.74	
akiyo_p352x288_30fps_420pl_300fr.yuv	CIF@30fps, 512kbps	0.25	1.59	188.90	0.27	1.91	157.38	

Table 2. Cycles Information for H264_ENC_01

(1) Average and peak values may vary by +/-5%.

Table 3. Cycles Information for H264_ENC_02

	PERFORMANCE STATISTICS FOR HIGH QUALITY SETTINGS (MEGA CYCLES) ⁽¹⁾							
			AVERAGE		PEAK			
INPUT NAME	RESOLUTION	ARM926 PER FRAME	ENCODE PER FRAME (ARM926 and ARM968)	FPS	ARM926 PER FRAME	ENCODE PER FRAME (ARM926 and ARM968)	FPS	
shields_p720x480_25fps_420pl_252fr.yuv	D1@30fps, 2mbps	0.26	7.34	40.86	0.26	7.63	39.35	
foreman_i640x480_30fps_420pl_300fr .yuv	VGA @30fps, 3mbps	0.28	6.53	45.88	0.22	6.88	43.59	
akiyo_p352x288_30fps_420pl_300fr.yuv	CIF@30fps, 512kbps	0.25	2.49	120.24	0.71	3.16	94.82	

(1) Average and peak values may vary by +/-5%.



Note:

- Encode frame MHz depicts the cumulative load on ARM926 and ARM968.
- ARM926 represents mega cycles per frame spend on ARM926.
- Encode frame time is the time seen from ARM926 only. Since most of the processing happens at HDVICP, the active load on ARM926 is the value mentioned in ARM926 column. Encoder frame time has no connection with HDVICP running at 243 MHz.
- All numbers are collected (both average and peak) at frame-level processing for first 300 frames.
- They are measured in presence of Linux without any system traffic.
- The version of the code used to collect these numbers have the following features included:
 - Interrupt mode of operation one interrupt signal processing overhead per frame.
 - Resetting of HDVICP and loading of code into ARM968 DTCM once per Process call.

Table 4	4. M	emory	Stat	istics
---------	------	-------	------	--------

CONFIGURATION ID		CONSTANT	HEAP		STACK	TOTAL
in Linoit		CONSTANT	PERSISTENT	SCRATCH	STACK	
H264_ENC_01 H264_ENC_02	256264	796	3247996	25960	12288	3543292

(1) All these memory requirements are for ARM926 encoder library(including DMA library). They do not include any memory requirements from test application side. Stack, heap and code requirements for test-application are extra. Constant memory size requirements include code memory of ARM968 since it forms a constant table on ARM926 before transfer.

(2) The constant size is the sum of .cinit, .bss, and .const sections used by H.264 encoder library.

Table 5. Internal Data Memory Split-Up - HDVICP

	DA	TA MEMORY - HDVICP (IN BYT	ES)
CONFIGURATION ID	ARM968 ITCM ARM968 I		HDVICP BUFFERS
H264_ENC_01 H264_ENC_02	49152	32768	ALL

Table 6. Internal Data Memory Split-Up - VICP and ARM TCM (with useARM926Tcm = 0)

	DATA MEMORY – VICP AND ARM TCM						
CONFIGURATION ID	VIC	P ⁽¹⁾	ARM TCM ⁽²⁾				
	REQUESTS	SIZE (BYTES)	REQUESTS	SIZE (BYTES)			
H264_ENC_01	1	24928(720p)	-	-			
H264_ENC_02	2	5408(720p)	-	-			
	3	2624(720p)	-	-			
	4	2624(720p)	-	-			
	TOTAL	35584(720p)	-	-			

 (1) Formula for VICP memory usage: REQUEST 1: ((no.of.rowmbpairs+1) * 608) REQUEST 2: maxSupportedWidth + 4096 + 32 REQUEST 3: ((no.of.rowmbs + 2) * 32) REQUEST 4: ((no.of.rowmbs + 2) * 32)

(2) Formula for ARM TCM memory usage: NA



Table 7. Internal Data Memory Split-Up – VICP and ARM TCM (with useARM926Tcm = 1)

	DATA MEMORY – VICP AND ARM TCM						
CONFIGURATION ID	VIC	p ⁽¹⁾	ARM TCM ⁽²⁾				
	REQUESTS	SIZE (BYTES)	REQUESTS	SIZE (BYTES)			
H264_ENC_01	1	5408(720p)	1	24928(720p)			
H264_ENC_02	2	2624(720p)	-	-			
	3	2624(720p)	-	-			
	TOTAL	10656(720p)	TOTAL	24928(720p)			

(1) Formula for VICP memory usage: REQUEST 1: maxSupportedWidth + 4096 + 32 REQUEST 2: ((no.of.rowmbs + 2) * 32) REQUEST 3: ((no.of.rowmbs + 2) * 32)

Formula for ARM TCM memory usage: (2) REQUEST 1: ((no.of.rowmbpairs+1) * 608)

Table 8. DM365 H264 Encoder usage of Memory through CMEM

BUFFER	YUV 420P
Input Buffer	1382400 (for 720p) (InputWidth * InputHeight * 1.5) ⁽¹⁾
Output Buffer	691200 (for 720p) (worst case: InputBuffer/2)
МЕМТАВ	SIZE (IN BYTES)
Memtab 0	1344
Memtab 1	4680
Memtab 2	4680
Memtab 3	20480
Memtab 4	2048
Memtab 5 ⁽²⁾	3112704
Memtab 6	800
Memtab 7	48548
Memtab 8	60288
Memtab 9	3600
Memtab 10	14400
Memtab 11	384

(1) 'Height' and 'Width' used in equations are the parameters specified at the creation time. The memory requirement calculation is theoretical worst case for a particular resolution. (2)

Memtab 5 is calculated based on the resolution. The formula is: If(interlaced) uHeight = maxHeight + (PAD_VERT << 2) else uHeight = maxHeight + (PAD_VERT << 1) uWidth = maxWidth + (PAD HORIZ << 1) uSize = (uHeight * uWidth * 3) >> 1 Example: If maxHeight = 144, maxWidth = 176, PAD_VERT = 26 and PAD_HORIZ = 32 uSize = (240*196*3) >> 1 = 70560 (for progressive)



Notes

- HDVICP and VICP
 - The entire HDVICP is a video resource and is used by the codec
 - The codec uses VICP memory as scratch buffers and hence there is restriction on the usage of VICP concurrently
- DMA configuration

TC Qs	TC 0	TC 1	TC 2	TC 3	TOTAL
Usage	Reserved for system	Used by codec	Used by codec	Used by codec	-
Priority	0	1	1	2	-
EDMA Channels	NA	22	7	7	36
PaRAM Entries	NA	45	10	7	62
QDMA Channels	0	0	0	0	0/8

Table 9. DMA Configuration

- The HDVICP/VICP/EDMA resources are acquired using a generic resource manager known as Framework Component. See H.264 High Profile Encoder User's Guide for details.
- Code Placement All the algorithm code are placed in external memory. The performance quoted is not sensitive to algorithm code placement.
- Memory requests mentioned in the table are as requested by codec. The actual memory allocation may be slightly different (on the higher side), based on the alignment implementation of the memory allocator.

References

- ISO/IEC 14496-10:2005 (E) Rec. Information technology Coding of audio-visual objects H.264 (E) ITU-T Recommendation
- H.264 High Profile Encoder User's Guide (literature number: SPRUEU9)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
ASO	Arbitrary Slice Order
CIF	Common Intermediate Format
D1	Video Resolution for PAL(720x576) and NTSC(720x480)
DMA	Direct Memory Access
DPB	Decoded Picture Buffer
EVM	Evaluation Module
FMO	Flexible Macro-block Ordering
HDVICP	High Definition Video and Imaging Co-Processor sub-system
MONA	Media Oriented Negotiation Acceleration
NTSC	National Television System Committee
PAL	Phase Alternating Line
PSNR	Peak Signal to Noise Ratio
QCIF	Quarter Common Intermediate Format
QVGA	Quarter Video Graphics Array



ACRONYM	DESCRIPTION		
RS	Redundant Slice		
SEI	Supplemental Enhancement Information		
SPS	Sequence Parameter Set		
SQCIF	Sub Quarter Common Intermediate Format		
UMV	Unrestricted Motion Vectors		
VGA	Video Graphics Array		
VICP	Video and Imaging Co-Processor sub-system		
VUI	Video Usability Information		
WVGA	Wide Video Graphics Array (864x480)		
XDM	eXpressDSP Digital Media		

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2009, Texas Instruments Incorporated