

H.264 High Profile Decoder (v01.00.00) on DM365

FEATURES

- eXpressDSP[™] Digital Media (XDM 1.0 IVIDDEC2) interface compliant
- Validated on DM365 EVM with and without Linux[®]
- H.264 High Profile up to level 3.1 compliant
- Byte stream NAL unit format for input bit-stream
- Progressive frame type picture decoding supported
- Multiple slices and multiple reference frames supported
- CAVLC and CABAC decoding supported
- Main Profile features like B-Slice decoding and CABAC supported
- Weighted prediction for motion compensation in both P and B-slices supported
- Transform 8x8 mode, interspersed with transform 4x4 MBs supported
- Parsing and decoding with scaling lists present both in SPS and PPS NAL units supported
- Second chroma qp index offset value present in PPS supported
- All intra-prediction and inter-prediction modes
 supported
- Up to 16 MV per MB supported
- Adaptive and sliding window DPB management supported
- Output order conformance using frame bumping process supported
- Frame based decoding with frame size being multiples of 2 supported
- Outputs are available in YUV420 interleaved

little endian format

- Supplemental Enhancement Information (SEI) and Video Usability Information (VUI) supported
- Uses configurable frame display delay for out of order display
- Performs basic error concealment on erroneous frames and reports the type of error occurred
- Resolution upto 720p supported
- This version of the decoder does not support the following features:
 - Error concealment features such as ASO/FMO and redundant slices
 - Dynamic change in resolution
 - Raw NAL unit format for input bit-stream

DESCRIPTION

H.264 (from ITU-T, also called as H.264/AVC) is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H.264 standard defines several profiles and levels which specify restrictions on the bit-stream and hence limits the capabilities needed to decode the bit-streams. This project is developed using Code Composer Studio version 3.3.81.6 and using the code generation tools version 4.1.3.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

eXpressDSP is a trademark of Texas Instruments.

Linux is a registered trademark of Linus Torvalds. Monta Vista is a registered trademark of MontaVista Software, Inc. All other trademarks are the property of their respective owners.



Performance Summary

This section describes the performance of Standalone H.264 High Profile Decoder validated on DM365 EVM resulting in performance equivalent to 30 fps.

Table 1. Configuration Table

CONFIGURATION	ID
H.264 High Profile levels up to 3.1	H264_DEC_01

Performance Measurement Procedure

- Measured with program memory and I/O buffers in external memory, I/D cache enabled, ARM @297 MHz, HDVICP @243 MHz, DDR @243 MHz, Monta Vista[®] Linux[®] 5.0
- Linux is used to measure the performance numbers in this Datasheet.
- The process time is measured across algActivate/process/algDeactivate function call using gettimeofday() utility of linux.
- NFS File system is used as an environment in performance measurement.

Table 2.	Cycles	Information	for H26	4_DEC_01
----------	--------	-------------	---------	----------

	PERFORMANCE STATISTICS (MEGA CYCLES) ⁽¹⁾							
		AVERAGE			PEAK			
INPUT NAME	RESOLUTI ON	ARM926 PER FRAME	DECODE PER FRAME (ARM926 and ARM968)	FPS	ARM926 PER FRAME	DECODE PER FRAME (ARM926 and ARM968)	FPS	
CIF_L1.2_384Kbps_15fps_news.264	CIF (352x288)	0.49	1.38	215.3	0.87	2.72	109.1	
foreman_p640x480_30fps_420pl_300fr_1ref.264	VGA (640x480)	0.50	3.07	96.6	0.57	3.33	89.3	
D1_football_720x480_384_30fBP.264	D1(720x480)	0.51	3.23	91.9	0.65	3.35	88.6	
16MV_lpb_city_p1280x720_30fps_420pl_600fr.264	720p (1280 x 720)	0.48	8.78	33.8	0.53	9.94	29.9	

(1) Average and peak values may vary by +/-5%.

Table 3. Cycles Information for H264_DEC_01 for Closed Loop Configuration⁽¹⁾

	PERFORMANCE STATISTICS (MEGA CYCLES) ⁽²⁾							
		AVERAGE				PEAK		
INPUT NAME	RESOLUTIO N	ARM926 PER FRAME	DECODE PER FRAME (ARM926 and ARM968)	FPS	ARM926 PER FRAME	DECODE PER FRAME (ARM926 and ARM968)	FPS	
akiyo_p352x288_30fps_420pl_300fr.264	CIF(352x288)	0.50	1.36	218.0	0.57	1.47	202.1	
foreman_i640x480_30fps_420pl_300fr.264	VGA(640x48 0)	0.50	3.16	93.9	0.65	4.85	61.3	
shields_p720x480_25fps_420pl_252fr.264	D1(720x480)	0.50	3.41	87.1	0.62	4.76	62.4	
parkrun_p1280x720_30fps_420pl_300fr.264	720p (1280 x 720)	0.50	7.65	38.8	0.61	9.23	32.2	

(1) Closed loop configuration refers to the streams encoded by DM365 H.264 encoder.

(2) Average and peak values may vary by +/-5%.



Note:

- Decode frame depicts the cumulative load on ARM926 and ARM968.
- The values in Table 2 and Table 3 are as measured on the ARM926 side. These are the actual cycles as seen from the host on the DM365 EVM board and will be close to cycles seen on the final system (for average case).
- ARM926 represents mega cycles per frame spend on ARM926.
- Decode frame time is the time seen from ARM926 only. Since most of the processing happens at HDVICP, the active load on ARM926 is the value mentioned in ARM926 column. Decoder frame time has no connection with HDVICP running at 243 MHz.
- All the values are collected (both average and peak) at frame-level processing.
- For streams with more than 50 frames, profiling is done for first 50 frames only.
- They are measured with Linux without any system traffic.
- The version of the code used to collect these numbers have the following features included:
 - Interrupt mode of operation one interrupt signal processing overhead per frame.
 - Resetting of HDVICP and loading of code into ARM968 DTCM once per stream.

Table 4. Memory Statistics (Host ARM926 External Memory)

	MEMORY STATISTICS (IN BYTES) ⁽¹⁾						
CONFIGURATION		DATA MEMORY					
ID	PROGRAM	CONSTANT ⁽²⁾	HEAP		STACK	DPB FOR LEVEL	TOTAL
		CONSTANT	PERSISTENT ⁽⁴⁾	SCRATCH	STACK	3.1 ⁽³⁾	
H264_DEC_01	314262	564	7247000	0	12288	9289728	16863842

(1) All these memory requirements are for ARM926 decoder library only. They do not include any memory requirements from test application side. Stack, heap and code requirements for test-application are additional.

(2) Constant memory size requirements include code memory of ARM968 since it forms a constant table on ARM926 before transfer.
 (3) DPB for level 3.1 indicates tentative buffer requirements on the test application side to manage the DPB requirements of level 3.1 compliant H.264 decoder library implementing XDM1.0 API. DPB memory requirements given here include padding requirements of 24 pixels on either sides of all dimensions (luma and packed chroma) assuming 4:2:0 format. It also includes memory required for holding the current frame. To enable optimal DMA transfers in the application, the picture width has been aligned to the next 32-byte boundary. For example, padded and aligned 720p picture will have a width of 1280 + 48 (padding) + 16(alignment) = 1344. Due to this padding and alignment constraints, the DPB requirement for a normal picture is different from its rotated version. The DPB requirement for some of the supported resolutions on the higher-end is provided in Table 5.

(4) Persistent memory includes space required for 256 PPS and 32 SPS.

Table 5. DPB Requirement (for level 3.1)

RESOLUTION	DPB REQUIREMENT
720p (1280x720)	9289728

Table 6. Internal Data Memory Split-Up

	DATA MEMORY - VICP AND HDVICP (IN BYTES)					
	HDVICP			VICD ⁽¹⁾		
	ARM 968 ITCM	ARM 968 DTCM	HDVICP BUFFERS	VICPY		
H264_DEC_01	48K	32K	ALL	30176		

(1) Three buffers are used in VICP, one buffer for storing ECD MB info and two buffers for storing intra prediction data. The number in the table is calculated for a 720p stream.

Formula for calculating ECD-MB information buffer size: Size = (maxWidthMbs + 2) * 304;

Formula for calculating intra prediction buffer size: Size = (((maxWidthMbs + 2) << 4) << 1);

Table 7. H264 Decoder DM365 Codec Usage of Memory Through CMEM

BUFFER	YUV420P
Input Buffer ⁽¹⁾	0x20000
Output Buffer	1548288

(1) The size of the input buffer should be equal to or greater than one frame data..



BUFFER	YUV420P			
MEMTAB NUMBER	SIZE IN BYTES ⁽²⁾			
Memtab 0	896			
Memtab 1	8704			
Memtab 2	8704			
Memtab 3	2688			
Memtab 4	5632			
Memtab 5	6650880			
Memtab 6	282624			
Memtab 7	47752			
Memtab 8	158368			
Memtab 9	26224			
Memtab 10	384			
Memtab 11	10240			
Memtab 12	13184			
Memtab 13	30720			

Table 7. H264 Decoder DM365 Codec Usage of Memory Through CMEM (continued)

(2) The table has numbers for 720p resolution.

The following CMEM allocations are dependent on the maxWidth and maxheight and it provides the formula for calculating the size based on the input resolution:

- Output Buffer = frameSize_padded frameSize_padded = ((maxWidth + 48 + alignment)*(maxHeight+ 48))
- Memtab 4 = 2 * ((((maxWidth + 4 * 16) * 2) + 8 + 127) & 0xFFFFF80)
- This is for storing the top rows for intra prediction. One for even row and one for odd row.
 Memtab 5 = ((((maxWidth >> 4) + 1) * (maxHeight >> 4)) + 1) * (dpb_limit at level 3.1 + 1) This is for storing ecd mb information.



Notes

- HDVICP and VICP
 - The entire HDVICP is a video resource and is used by the codec
 - The codec uses VICP memory as scratch buffers and hence there is restriction on the usage of VICP concurrently.
- DMA configuration

Table	8.	DMA	Configuration
	•••		••••••••••••••••••••••••••••••••••••••

TC Q's	TC 0	TC 1	TC 2	TC 3	TOTAL
Usage	Reserved for system	Used by codec	Used by codec	Used by codec	-
Priority	0	1	1	2	-
EDMA Channels	NA	16	9	1	26
PaRAM Entries	NA	14	52	1	67
QDMA Channels	0	0	0	0	0/8

 The HDVICP/VICP/EDMA resources are acquired using a generic resource manager known as Framework Component. See H.264 High Profile Decoder on DM365 User's Guide for details.

Code Placement

- All the algorithm code are placed in external memory. The performance quoted is not sensitive to algorithm code placement.

References

- ISO/IEC 14496-10:2005 (E) Rec. Information technology Coding of audio-visual objects H.264 (E) ITU-T Recommendation.
- *H.264 High Profile Decoder on DM365 User's Guide* (literature number: SPRUEV0)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION	
ASO	Arbitrary Slice Order	
CIF	Common Intermediate Format	
720p	1280x720 resolution	
DMA	Direct Memory Access	
DPB	Decoded Picture Buffer	
DTCM	Data Tightly Coupled Memory	
EVM	Evaluation Module	
FIQ	Fast Interrupt Request	
FMO	Flexible Macro-block Ordering	
HDVICP	High Definition Video and Imaging Co-Processor sub-system	
IRQ	Interrupt Request	
PPS	Picture Parameter Set	
QCIF	Quarter Common Intermediate Format	
QVGA	Quarter Video Graphics Array	
RS	Redundant Slice	



DESCRIPTION	
Supplemental Enhancement Information	
Sequence Parameter Set	
Sub Quarter Common Intermediate Format	
Unrestricted Motion Vectors	
Video and Imaging Co-Processor sub-system	
Video Usability Information	
Wait For Interrupt	
eXpressDSP Digital Media	

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2009, Texas Instruments Incorporated