H.264 High Profile Decoder (v01.10.05) on DM6467

Check for Samples:

FEATURES

- eXpressDSP™ Digital Media (XDM 1.0 IVIDDEC2) compliant
- **Up to level 4 features of the High Profile (HP) supported**
- **Validated on DM6467 EVM**
- **Progressive, interlaced, Picture Adaptive Frame Field (PicAFF) and Macro-block Adaptive Frame Field (MBAFF) type picture decoding supported**
- **Multiple slices and multiple reference frames supported**
- **CAVLC and CABAC decoding supported**
- **All intra-prediction and inter-prediction modes supported**
- **Up to 16 MV per MB supported**
- **Frame based decoding supported**

- **Picture width greater than 64 pixels supported**
- **Tested for compliance with JM version 10.1 reference decoder**
- **Long term reference frame and adaptive reference picture marking supported**
- **Reference picture list reordering supported**
- **PCM macro block decoding supported**
- **Gaps in frame_num supported**
- **Error resiliency and concealment supported**
- **SEI and VUI parsing supported**

DESCRIPTION

H.264 is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H264 Decoder is validated on DM6467 EVM with Code Composer Studio version 3.3.49 and code generation tools version 6.0.8.

PRODUCT PREVIEW

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Performance Summary

This section describes the performance of the H264 Decoder on DM6467 EVM.

Table 1. Configuration Table

CONFIGURATION	ID
H264 High Profile Decoder	DM6467_HP_001

Table 2. Cycles Information in MHz - Profiled on DM6467 EVM[1] with Code Generation Tools Version 6.0.8

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND)[2] [3]				
	TEST DESCRIPTION	NON-BLOCKING DSP CYCLES@675MHz		BLOCKING DSP CYCLES@675MHz	
		AVERAGE[4]	PEAK[5]	AVERAGE[4]	PEAK[5]
DM6467_HP_001	BALLOONS.264; High Profile, 1920 X 1088, MBAFF, IPBB…	320.2	355.3	571.3	598.5
	fball_60.264; High Profile, 1920 X 1088, MBAFF, IPBB…	333.1	352.4	584.2	597.1
	letterman1_30.264; High Profile, 1920 X 1088, MBAFF, IPBB…	334.3	352.6	584.4	596.1

(1) C64x+ is clocked at 675MHz. DDR is 32-bit, clocked at 310MHz, 8 bank. HDVICP is clocked at 337MHz.
(2) Measured with program memory, stack, and I/O buffers in external memory and with cache configuration 64 K bytes L2 cache, 32 K L1D and 32 K L1P cache.
(3) Average and peak MCPS measurements can vary by +/-5%.
(4) Average values are calculated based on the average of all frames in the sequence.
(5) Peak values are calculated assuming that the most demanding frame is repeated 30 times in the sequence, rather than finding the most demanding 30 frames sequence in the bit-stream.

Table 3. Memory Statistics - Generated with Code Generation Tools Version 6.0.8

CONFIGURATION ID	MEMORY STATISTICS[1]				
	PROGRAM MEMORY[2]	DATA MEMORY			TOTAL
		INTERNAL[3]	EXTERNAL[4]	STACK	
DM6467_HP_001	291.72	22.63	14214.70	4.00	14533.05

(1) All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).
(2) Program memory quoted also includes the HDVICP APIs used by the decoder.
(3) Internal memory is placed in L2 SRAM.
(4) Includes frame buffers for 1080P resolution.

Table 4. Internal Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - INTERNAL [1]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_HP_001	0	22.63	0

(1) All memory requirements are expressed in kilobytes.

Table 5. External Data Memory Split-Up

CONFIGURATION ID	DATA MEMORY - EXTERNAL [1]		
	SHARED		INSTANCE
	CONSTANTS	SCRATCH	
DM6467_HP_001	207.70	0	14007.00

(1) All memory requirements are expressed in kilobytes.

Notes

The performance values shown in Table 2 is a result of the following configurations:

- HDVICP
  - The entire HDVICP is a video resource and uses 16K ITCM and 8K DTCM.
  - The decoder is configured to run either on HDVICP-0 or HDVICP-1.
- Cache configuration

Table 6. Cache Configuration

	AVAILABLE	USED
L1 p (Program Memory)	32K	32K – cache
L1d (Data Memory)	32K	32K – cache
L2	128K	64K – cache

- DMA configuration

Table 7. DMA Configuration

TC Qs	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM[1]
Usage	Writes to L2 SRAM	Writes to HDVICP	Writes to HDVICP	Writes to HDVICP	-	-
Priority[2]	3	2	2	3	-	
EDMA channels	1	8	8	4	21	64
QDMA channels	0	0	0	0	0	8
Num PARAMS	-	-	-	-	159	512

(1) Maximum corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip. It does not indicate the maximum number requested by the codec.

(2) Lesser number corresponds to higher TC priority. Default priority is 2. When different TCs have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.

- Code Placement

  All the algorithm code are placed in external memory. The performance values in Table 2 are sensitive to algorithm code placement. See the sample linker file provided in the test application setup for algorithm code placement.

References

- ISO/IEC 14496-10: March 2005 (E) Rec. H.264 (E) ITU-T Recommendation
- *H.264 High Profile Decoder on DM6467 User's Guide* (literature number: SPRUFE0A)

Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

ACRONYM	DESCRIPTION
625SD	Level 3.0 Maximum resolution format size 720x576
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
D1	SDTV image resolution (720x480)
DMA	Direct Memory Access

PRODUCT PREVIEW

ACRONYM	DESCRIPTION
EVM	Evaluation Module
HD	High Definition
HDVICP	High Definition Video and Imaging Co-Processor
MBAFF	Macro Block Adaptive Frame Field
PCM	Pulse Code Modulation
PicAFF	Picture Adaptive Frame Field
QCIF	Quarter Common Intermediate Format
QDMA	Quick Direct Memory Access
SDTV	Standard Definition Television
SEI	Supplemental Enhancement Information
SRAM	Static Random Access Memory
VGA	Video Graphics Array (640x480 resolution)
VUI	Video Usability Information
XDM	eXpressDSP Digital Media

PRODUCT PREVIEW

IMPORTANT NOTICE