

eXpressDSP Digital Media (XDM 1.0 IVIDDEC2) interface compliant

- Validated on the TMS320C6678 EVM
- MPEG4 advanced simple profile, level 0, 1, 2, 3, 4 and 5 supported
- MPEG4 visual simple profile, level 0, 1, 2, 3, 4A and 5 supported
- H.263 profile 3 and level 10, 20, 30, 45, 50, 60 and 70 supported
- Supports H.263 Annex-IJKT
- Post-processing filter, de-blocking, and deringing supported
- Spatial and temporal error concealment supported only for I and P progressive frames
- Contains optimized I and P flow to decode frames up to WVGA (854 x 480 and 480 x 854) and D1 (720x576) resolution at 30 fps
- Half-pel and quarter-pel interpolation supported
- Outputs are available in YUV 420 planar and 422 interleaved little endian formats
- Display width feature supported
- Single object supported
- Supports streams that are non-multiple of 16

- Global Motion Compensation (GMC) 1, 2 and 3 warp supported for progressive frame
- Supports Frame level byte-swap. If it is enabled, algorithm will do byte-swap conversion at frame level dynamically. Also, encoded bytes per frame information need not be provided as input to the application.
- Supports ELF ABI format.
- Supports "ecpy" for EDMA and "IRES" interface.

description

MPEG4 is a popular video algorithm defined by Motion Picture Expert Group (MPEG) for video conferencing applications. This codec has been built and tested on the TMS320C6678 EVM. This version of codec is compiled, assembled, archived, and linked using the code generation tools version 7.4.0 and developed using Code Composer Studio version 5.2.1.00018.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



summary of performance

Table 1. Configuration Table

CONFIGURATION	ID
MPEG4 visual simple profile, levels 0, 1, 2, 3, 4A and 5 H263 profile 3, level 10, 20, 30, 45, 50, 60, and 70 MPEG4 Advanced Simple Profile level 0 to 5	MPEG4_DEC_001

Table 2. Cycles Information for MPEG-4 ASP Streams - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SECOND) 1			
	TEST DESCRIPTION		PEAK ³	
	akiyo.cif.890kbps.mta.cmp, YUV420, CIF @ 715 kbps, IQ and Interlace	35.25	63.48	
	viperkillercuts_p720x576_8000kbps_L5_25fps.m4v, YUV420, D1 @ 9 mbps, IQ and Quarterpel	213.95	300.92	
	harryPotter_p720x480_8000kbps_L5_30fps.m4v, YUV420, D1 @ 8 mbps, IQ and Quarterpel	173.35	189.04	
	harryPotter_p720x480_8000kbps_L5_30fps_BFRAME.m4v, YUV420, D1 @ 7 mbps, IQ, Quarterpel and B frames	214.35	243.71	
MPEG4_DEC_001	football_800x480_420_5mbps_30fps_BFRAME.m4v, YUV420, WVGA @ 5 mbps, B frames	176.31	238.93	
	jets_p848x480_420_5mbps_30fps_BFRAME.m4v,, YUV420, WVGA @ 5 mbps, B frames	170.52	236.92	
	jets_p854x480_420_5mbps_30fps_QUANT1.m4v YUV420, WVGA @ 5 mbps, Quant1	125.48	170.73	
	jets_p864x480_420_5mbps_30fps_QUANT1.m4v YUV420, WVGA @ 5 mbps, Quant1		175.39	
	shild_wp1_wa3_qpel0_IP_8mbps.m4v YUV420, D1 @ 8 mbps,GMC	140.75	361.41	
	shild_wp1_wa3_qpel0_IPB_8mbps.m4 YUV420, D1 @ 8 mbps,GMC	181.37	361.42	
	akiyo_cif_wp3_wa3_384kbps.cmp, YUV420, CIF @384kbps 3 warp GMC	103.9	116.77	

¹ Measured with program memory and I/O buffers in external memory, stack in internal memory and with cache configuration:



³² K-bytes L1P cache, 32 K-bytes L1D cache and 64 K-bytes L2 cache.

Average cycles are calculated by taking frame level average for entire sequence and then scaling it to 25/30 fps.

³ Peak cycles are calculated by taking frame level peak over entire sequence and then scaling it to 25/30 fps.



SPRS765A - January 2013

Table 3. Cycles Information for MPEG-4 SP Streams - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SECOND) 1			
	TEST DESCRIPTION	AVERAGE ²	PEAK ³	
	akiyo_qcif10_q1.m4v, MPEG4 SP, YUV420, QCIF @ 1 mbps	12.19	21.68	
	cif_high_256kbps_100f_fixedqp20_nofilter.m4v, MPEG4 SP, YUV420, CIF @ 256 kbps	28.69	38.27	
	foreman_vga_dp0.m4v, MPEG4 SP, YUV420, VGA @ 3 mbps	103.99	110.98	
	hp_720x480.m4v, MPEG4 SP, YUV420, D1 @ 10 mbps	149.51	227	
MPEG4_DEC_001	CIMG0389_480x854.m4v, MPEG4 SP, WVGA @ 6 mbps	141.6	159.73	
WI 201_920_001	football_p864x480_420_8mbps_30fps_NoTools.m4v, WVGA 8mbps	158.29	197.53	
	football_p800x480_420_8mbps_30fps_NoTools.m4v, WVGA 8mbps	150.51	179.6	
	football_p848x480_420_8mbps_30fps_NoTools.m4v, WVGA 8mbps	158.91	189.81	
	football_p854x480_420_8mbps_30fps_NoTools.m4v, WVGA 8mbps	159.62	194.29	

¹ Measured with program memory and I/O buffers in external memory, stack in internal memory and with cache configuration: 32 K-bytes L1P cache, 32 K-bytes L1D cache and 64 K-bytes L2 cache.

Table 4. Cycles Information for H263 Streams - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SECOND) 1				
	TEST DESCRIPTION	AVERAGE ²	PEAK ³		
	akiyo.qcif.263, H263, YUV420 , QCIF @ 122 kbps	8.82	12.37		
MPEG4_DEC_001	QCIF_64kbps_AnnexIJKT.mpg4, H263, YUV420, QCIF @ 300 kbps, Annex IJKT	15.79	25.25		
	D1p25_mobcal_420p_8Mbps_Level60.263, YUV420, H263 Level 60, 720x288 @ 8 Mbps	127.63	136.85		

¹ Measured with program memory and I/O buffers in external memory, stack in internal memory and with cache configuration: 32 K-bytes L1P cache, 32 K-bytes L1D cache and 64 K-bytes L2 cache.



² Average cycles are calculated by taking frame level average for entire sequence and then scaling it to 25/30 fps.

³ Peak cycles are calculated by taking frame level peak over entire sequence and then scaling it to 25/30 fps.

² Average cycles are calculated by taking frame level average for entire sequence and then scaling it to 25/30 fps.

³ Peak cycles are calculated by taking frame level peak over entire sequence and then scaling it to 25/30 fps.

Table 5. Cycles Information - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0 for foreman_vga_dp0.m4v, MPEG4 (YUV420, VGA @ 3 mbps)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SECOND) 1		
	AVERAGE ²	PEAK ³	
	With De-blocking enabled	171.09	178.78
MPEG4_DEC_001	With De-ringing enabled	191.26	198.21
	With De-blocking and De-ringing enabled	243.26	250.94

¹ Measured with program memory and I/O buffers in external memory, stack in internal memory and with cache configuration: 32 K-bytes L1P cache, 32 K-bytes L1D cache and 64 K-bytes L2 cache.

Table 6. Cycles Information - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0 for MPEG4 SP, MPEG4 ASP and H263 streams (YUV422)

CONFIGURATION ID	PERFORMANCE STATISTICS (IN MEGA CYCLES PER SECOND) 1			
	TEST DESCRIPTION	AVERAGE ²	PEAK ³	
MPEG4_DEC_001	foreman_vga_dp0.m4v, MPEG4 SP, YUV422, VGA @ 3 mbps	108.62	115.57	
MPEG4_DEC_001	viperkillercuts_p720x576_8000kbps_L5_25fps.m4v, MPEG4 ASP,YUV422, D1 @ 9 mbps, IQ and Quarterpel	220.13	306.59	
MPEG4_DEC_001	hp_720x480.m4v, MPEG4 SP, YUV422, D1 @ 10 mbps	154.41	232.71	
MPEG4_DEC_001	D1p25_mobcal_420p_8Mbps_Level60.263, YUV422, H263 Level 60, 720x288 @ 8 Mbps	126.76	135.64	

¹ Measured with program memory and I/O buffers in external memory, stack in internal memory and with cache configuration:

Notes:

- Profiled on TMS320C6678 EVM.
- Average and peak MCPS measurements can vary by +/-5%.

Table 7. Memory Statistics - Generated with Code Generation Tools Version 7.4.0

	MEMORY STATISTICS ¹				
CONFIGURATION ID	CONFIGURATION ID PROGRAM DATA MEMORY		TOTAL		
	MEMORY	INTERNAL ²	EXTERNAL	STACK	TOTAL
MPEG4_DEC_001 (QCIF)	395	61	678	12	1146
MPEG4_DEC_001 (CIF)	395	61	1628	12	2096



² Average cycles are calculated by taking frame level average for entire sequence and then scaling it to 25/30 fps.

³ Peak cycles are calculated by taking frame level peak over entire sequence and then scaling it to 25/30 fps.

³² K-bytes L1P cache, 32 K-bytes L1D cache and 64 K-bytes L2 cache.

Average cycles are calculated by taking frame level average for entire sequence and then scaling it to 25/30 fps.

³ Peak cycles are calculated by taking frame level peak over entire sequence and then scaling it to 25/30 fps.



SPRS765A - January 2013

	MEMORY STATISTICS ¹				
CONFIGURATION ID	PROGRAM	DATA MEMORY			TOTAL
	MEMORY	INTERNAL ²	EXTERNAL	STACK	TOTAL
MPEG4_DEC_001 (VGA)	395	61	4008	12	4476
MPEG4_DEC_001 (D1)	395	61	5225	12	5693
MPEG4_DEC_001 (WVGA)	395	61	5209	12	5677

All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes) and there could be a variation of approximately 1-2% in values.
² Internal memory is placed in L1D RAM.

Table 8. **Internal Data Memory Split-up**

	DATA MEMORY – INTERNAL ¹			
CONFIGURATION	SHA	INSTANCE ²		
	CONSTANTS	SCRATCH	INSTANCE	
MPEG4_DEC_001	0	61	0	

Internal memory refers to L1DRAM. All memory requirements are expressed in kilobytes and there could be a variation of approximately 1-2% in values.

2 I/O buffers not included. Some of the instance memory buffers could be scratch.



MPEG4 Advanced Simple Profile Decoder (v02.03.01) on C66x

SPRS765A - JANUARY 2013

notes

- I/O buffers:
- Input buffer size = 405 K-bytes (WVGA, one YUV422 interleaved frame)
- Output buffer size = 810 K-bytes (for decoding one WVGA frame)
- Memory Configuration
- L1P: 32 K-bytes program cache
- L1D: 32 K-bytes data cache
- L2: 128 K-bytes cache
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N*(Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N*(Instance + I/O buffers + Stack + Scratch)
- MCPS calculations are done in frame based mode. In case, it is run in buffer mode, MCPS increase can be upto 10% assuming additional buffer size of 10 K-bytes per frame.

references

- MPEG4 Standard (ISO_IEC_14496-2_2001)
- H.263 Standard (ITU-T Series H 02/98)
- MPEG4 Simple Profile Decoder on C66x User's Guide(literature number: SPRUH64A)

glossary

Constants Elements that go into .const memory section

Scratch Memory space that can be reused across different instances of the algorithm

Shared Sum of Constants and Scratch

Instance Persistent-memory that contains persistent information - allocated for each instance of

the algorithm





SPRS765A – January 2013

acronyms

ABI Application Binary Interface
CIF Common Intermediate Format
EDMA Enhanced Direct Memory Access
ELF Executable and Linkable Format
GMC Global Motion Compensation

NTSC National Television Standards Committee

QCIF Quarter Common Intermediate Format

QVGA Quarter Video Graphics Array

SQCIF Sub Quarter Common Intermediate Format

VGA Video Graphics Array

WVGA Wide Video Graphics Array
XDM eXpressDSP Digital Media



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products Audio www.ti.com/audio **Amplifiers** amplifier.ti.com dataconverter.ti.com **Data Converters DLP® Products** www.dlp.com DSP dsp.ti.com Clocks and Timers www.ti.com/clocks Interface interface.ti.com Logic logic.ti.com Power Mgmt power.ti.com defense Microcontrollers microcontroller.ti.com

Applications Automotive & Transportation <u>www.ti.com/automotive</u> Communications & Telecom www.ti.com/communications Computers & Peripherals www.ti.com/computers Consumer Electronics www.ti.com/consumer-apps Energy and Lighting www.ti.com/energyapps Industrial www.ti.com/industrial Medical www.ti.com/medical Security www.ti.com/security Space, Avionics & Defense www.ti.com/space-avionics-

Video & Imaging www.ti.com/video

www.ti.com/omap TI E2E Community e2e.ti.com

OMAP Applications Processors
Wireless Connectivity
www.ti.com/wirelessconnectivity

www.ti-rfid.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright© 2013, Texas Instruments Incorporated



RFID