MPEG2 Encoder (v01.00.00) on TMS320C6678 Platform

FEATURES

- **Supports MPEG2 Simple profile at Main level (SP@ML)**
- **Supports Main profile at Low, Main and High levels (MP@LL, MP@ML, and MP@HL)**
- **Supports arbitrary video resolutions from 64x64 to 1920x1080**
- **Supports B frame encoding**
- **Supports both progressive and interlaced encoding**
- **Supports user defined quantization matrix**
- **Supports non linear quantization**
- **Supports insertion of Intra frame at random point with force frame control**
- **Supports change of bitrate and frame rate dynamically**
- **Supports Rate control for Storage and low delay devices(VBR and CBR)**
- **Supports finer control of quantization parameter range.**
- **Supports Macro block level Perceptual rate control**
- **Supports Image width and height that are multiple of 16 also support image height being non multiple of 16**
- **Supports user controlled Half pel, Integer pel motion estimation**
- **Supports control to have bottom field first encoding**
- **Supports adaptive Intra refresh mechanism**
- **Supports user configurable Group of Pictures (GOP) length**
- **Supports YUV 420 Planar color sub sampling formats**
- **Supports multiple slices encoding based on number of MBs in slice**
- **Graceful exit under error conditions is supported**
- **Does not support sub frame level data synchronization.**
- **Encoder library validated on TMS320C6678 hardware EVM**
- **The other explicit features that TI's MPEG2 Encoder supports are**
  - **eXpressDSP Digital Media (XDM IVIDENC2) interface compliant**
  - **Supports multi-channel functionality**
  - **Independent of any operating system (DSP/BIOS, Linux etc)**
  - **Cache aware encoder library**
  - **Ability to get plugged in any multimedia frameworks (eg. MCSDK, Codec Engine, OpenMax, GStreamer etc)**

DESCRIPTION

MPEG2 is widely used as video standard for digital television signals. It also specifies the format of movies and other programs specified in DVD and similar discs. The video section, part 2 of MPEG2 specifies compression technology for encoding video standards. MPEG2 Video formally known as ISO/IEC-13838-2. This project is developed using Code Composer Studio version 5.1.0.09000 and code generation tools version 7.4.1.

PRODUCT PREVIEW

Performance and Memory Summary

This section describes the performance and memory usage of the MPEG2 encoder tested on TMS320C6678 EVM

Table 1 Configuration Table

CONFIGURATION	ID
MPEG2 Main Profile, YUV420, I, P & B frames, Low Main and High Level, Single Core	MPEG2_ENC_001
MPEG2 Main Profile, YUV420, I, P & B frames, Low Main and High Level, Multi Core(4 Cores)	MPEG2_ENC_002

Table 2 Cycles Information - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.1

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1)		
	TEST DESCRIPTION	AVERAGE(2)(4)	PEAK(3)(4)
MPEG2_ENC_001	Airshow_p1920x1080_420p_8bit.yuv, YUV420,VBR, IBBP @ 12Mbps @ 30 frames per second	3982	4162
	Fruits_i1920x1080_420p_8bit.yuv , YUV420, VBR, IBBP @ 12Mbps @ 30 frames per second	3835	3976
	Airshow_p720x480_420p_8bit.yuv, YUV420, VBR, IBBP @ 4Mbps @ 30 frames per second	721	758
MPEG2_ENC_002	Airshow_p1920x1080_420p_8bit.yuv, YUV420, VBR, IBBP @ 12Mbps @ 30 frames per second	1116	1153
	Fruits_i1920x1080_420p_8bit.yuv , YUV420, VBR, IBBP @ 12Mbps @ 30 frames per second	1126	1140

(1) Measured with C66x DSP 1250MHz clock, DDR3 1333MHZ clock, Program memory in SL2 memory, I/0 buffers in external memory and stack in internal L2 memory with cache configurations: 32KB L1P Program cache, 32KB L1D Data cache and 64KB L2 cache. Performance is measured using MCSDK test framework version 2.1.0.4 to make sure system overheads are included. There could be a variation of approximately 2-3% in the values.
(2) Average cycles are calculated as maximum of moving average of 30 frames, multiplied with 30 to get per second Mhz.
(3) Peak cycles are calculated as maximum of moving average of 3 frames multiplied with 30 to get per second Mhz. Peak cycles are considered only after initial 2 seconds of encoding (to allow encoder to reach steady state).
(4) Performance is measured across the process call after all cores reach same sync point over 90 frames.

Table 3 Memory Statistics of TMS320C6678 with Code Generation Tools Version 7.4.1

CONFIGURATION ID	MEMORY STATISTICS(1)(2)				
	PROGRAM MEMORY	DATA MEMORY (3) (4) (5)			TOTAL
		PERSISTENT	CONSTANT	SCRATCH	
MPEG2_ENC_001	359	12917	9	0	13285
MPEG2_ENC_002	359	17837	9	0	18205

(1) All these memory requirements are for MPEG2 encoder library only. They do not include any memory requirements from test application side. Stack, heap and code requirements for test-application are extra.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) The memory requirements given in Table 3 are calculated for1920x1080 resolution and YUV 420 Chroma sub sampling.
(4) Program code is stored in SL2 memory.
(5) Typical input and output buffers for 1920x1080 resolutions are as follows.
Input Buffer: 3060KB
Output Buffer: 2000KB

Table 4 Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL(1) (2)					
	LOCAL L2				SHARED L2	TOTAL
	CONSTANTS	PERSISTENT	SCRATCH	STACK		
MPEG2_ENC_001 MPEG2_ENC_002	0	0	244	16	40	300

(1) Encoder stack is mapped to Local L2 memory and not included in the above table.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).

Table 5 Cache/SRAM configuration (1)

NAME	AVAILABLE	CACHE	SRAM
L1P (Program Memory)	32KB	32KB	0KB
L1D(Data Memory)	32KB	32KB	0KB
L2	512KB	64KB	448KB

(1) All above mentioned numbers are for all configurations (MPEG2_ENC_001, MPEG2_ENC_002).

Table 6 EDMA Configuration (1) (5)

TC Q	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM(3)
Usage	R/W to DDR/L2	-	-	-	-	-
Priority(2)	0	-	-	-	-	-
EDMA Channels	8	-	-	-	8(4)	64
QDMA Channels	-	-	-	-	0(4)	8
Num PARAMS	32	-	-	-	32(4)	512

(1) All above mentioned numbers are for all configurations (MPEG2_ENC_001,MPEG2_ENC_002).
(2) Lesser number corresponds to higher TC priority. Default priority is TC0 > TC1 > TC2 > TC3. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.
(3) Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip for a channel controller. It does NOT indicate the maximum number requested by the codec.
(4) Same EDMA channel is used to copy data to DDR and to L2 memory at different instances.
(5) Above configuration table specifies EDMA hardware usage for each core in multicore scenario.

Notes

- I/O buffers:
  - Input buffer size = 3060 K-bytes (for 1920x1088 resolution, YUV420)
  - Output buffer size = 2000 K-bytes (for encoding 1920x1088 resolution)
- None of the output buffers are accessed by DSP cores hence the data should be valid in DDR (not in cache).

References

- ISOIEC 13838-2: MPEG2 Video coding specification
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard)
- MPEG2 Encoder on TMS320C6678 Platform User's Guide

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
DMA	Direct Memory Access
ISO/IEC	International Organization for Standardization/International Electro technical Commission
EVM	Evaluation Module
MPEG	Moving Picture Exerts Group
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265