



- eXpressDSP™ Digital Media (XDM IVIDENC2 Compliant)
- Multi-channel, reentrant implementation.
- Compliant with JPEG2K Core Coding System as specified in ISO/IES 15444-1 and ITU-T T.800.
- Optimized for C66x DSP and validated on the C6678 EVM
- Supports up to 12-bits per color sample
- Support grey-scale or 3 component images
- Supports RGB, YUV444, YUV422, and YUV420 image formats
- Supports ICT/RCT color transform
- Supports arbitrary tiling of image
- Supports 9/7 and 5/3 wavelet filters.
- Supports up to 6 resolution levels
- Support for image sizes up to 6600 x 4400 pixels
- Supports explicit and derived quantization modes under lossy compression mode.
- Supports code-block sizes of 64 and 32 respectively.
- Supports default, 128, 64, and 32 precinct sizes
- Supports up to 5 quality layers
- Supports LRCP, RPCL, RLCP, PCRL, and CPRL progression modes.
- Supports JP2/J2K and JPC file formats.
- Supports DCI 2K, DCI 4K bit-stream formats.

DESCRIPTION

JPEG2000 Standard was introduced in the year 2000. It provides improved compression performance and flexible code-stream format when compared to the JPEG Standard. It supports both lossy as well as lossless operating modes. JPEG2K Encoder is validated on C6678 EVM with Code Composer Studio version 5.2.1.00018 and code generation tools version 7.4.0.

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Copyright © 2015, Texas Instruments Incorporated



Summary of performance

Table 1. Configuration Table

CONFIGURATION	ID
VGA Profile on 1-core (640 x 480, RGB, 8 bits per component)	J2K_ENC_L1
2K Digital Cinema Profile on 1-core (2048 x 858, RGB, 12 bits per component, compression ratio = 0.16)	J2K_ENC_L2
2K Digital Cinema Profile on 1-core (2048 x 858, RGB, 12 bits per component, compression ratio = 0.08)	J2K_ENC_L3
4K Digital Cinema Profile on 1-core (4096 x 1716, RGB, 12 bits per component, compression ratio = 0.04)	J2K_ENC_L4
6K Profile on 1-core (6600 x 4400, RGB,, 8 bits per component)	J2K_ENC_L5
Full HD Profile on 1-core (1920 x 1080, YUV 422, 10 bits per component, compression ratio = 0.16)	J2K_ENC_L6

Table 2. Cycles Information – Profiled on C6678 EVM with CGTools Version 7.4.0

CONFIGURATION	PERFORMANCE STATISTICS (IN MILLION CYCLES) ¹	
	TEST DESCRIPTION	MILLION CYCLES ^{2,3}
J2K_ENC_L1	Orig01_bird_vga.ppm (640 x 480, 8 bits per components, lossless mode, decomposition level = 5, progression order = cprl)	206.7
J2K_ENC_L1	Orig01_bird_vga.ppm (640 x 480, 8 bits per components, rate = 0.25, explicit quantization, decomposition level = 5, progression order = cprl)	166.6
J2K_ENC_L1	Orig01_bird_vga.ppm (640 x 480, 8 bits per components, rate = 0.1, explicit quantization, decomposition level = 5, progression order = cprl)	165.6
J2K_ENC_L2	MM_2K_XYZ_1256.ppm (2048 x 858, 12 bits per component, rate = 0.16, mct enabled, explicit quantization, decomposition level = 5, progression order = cprl)	964
J2K_ENC_L3	MM_2K_XYZ_1256.ppm (2048 x 858, 12 bits per component, rate = 0.08, mct enabled, explicit quantization, decomposition level = 5, progression order = cprl)	1022
J2K_ENC_L4	Reel_2ab_1256_12b.ppm (4096 x 1716, 12 bits per component, rate = 0.04, mct enabled, explicit quantization, decomposition level = 6, progression order = cprl)	2876
J2K_ENC_L5	image000002b.ppm (6600 x 4400, 8 bits per component, rate = 0.03, mct enabled, explicit quantization, decomposition level = 6, progression order = pcrl, code-block size 64 x 64, precinct size = default, tile size = 512 x 512)	7843

PRODUCT PREVIEW

J2K _ ENC _L6	Ducks_take_off.yuv (1920x1080, 10 bits per component, rate = 0.16, mct enabled, explicit quantization, decomposition level = 5, progression order = cprl)	814
---------------	---	-----

¹Program placed in SL2, I/O buffers in external memory, stack in LL2, 32-KB L1P Cache, 32-KB L1D Cache, 64-KB L2 Cache, DDR speed at 1333 MHz, DSP at 1250 MHz.

²The MCycles numbers reported in this column were measured while running only on Core-0 of the device, while the other 7 cores were idling. If the codec is loaded on all 8 cores, the cycles consumed would be 6-10% higher, primarily due to DDR contention

³The MCycles numbers reported in this column are for a single Image in the video sequence

Table 3. Memory Statistics - Generated with Code Generation Tools Version 7.4.0

CONFIGURATION ID	MEMORY STATISTICS				
	PROGRAM MEMORY ²	DATA MEMORY			
		INTERNAL	EXTERNAL ³	STACK	TOTAL DATA
J2K _ ENC _L1	137 KB	290 KB	10319 KB	2 KB	10748 KB
J2K _ ENC _L2	137 KB	290 KB	10319 KB	2 KB	10748 KB
J2K _ ENC _L3	137 KB	290 KB	10319 KB	2 KB	10748 KB
J2K _ ENC _L4	137 KB	290 KB	10319 KB	2 KB	10748 KB
J2K _ ENC _L5	137 KB	290 KB	10319 KB	2 KB	10748 KB
J2K _ ENC _L6	137 KB	290 KB	10319 KB	2 KB	10748 KB

All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes)

²Program placed in SL2

³External memory placed in DDR3

Table 4. Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL ⁴		
	CONSTANTS	SCRATCH	INSTANCE ⁵
J2K _ ENC _L1	3 KB	280 KB	7 KB
J2K _ ENC _L2	3 KB	280 KB	7 KB
J2K _ ENC _L3	3 KB	280 KB	7 KB
J2K _ ENC _L4	3 KB	280 KB	7 KB
J2K _ ENC _L5	3 KB	280 KB	7 KB
J2K _ ENC _L6	3 KB	280 KB	7 KB

⁴Constants are placed in SL2 and Scratch buffer is placed in LL2. All memory requirements are expressed in kilobytes and there could be a variation of around 1-2% in numbers.

⁵I/O buffers not included. Some of the instance memory buffers could be scratch



notes

- Evaluation version performance values may be higher than the values specified in the performance table.
- Input buffer size for supporting up to 6600 x 4400 frame size and 16-bits per color component requires 166.2 MB.
- Maximum output buffer size allowed for a given input bit-stream is 16 MB.
- The performances obtained in Table 2 are sensitive to algorithm code placement. Refer the sample linker file provided in the test application setup for algorithm code placement. This is used for profiling in Table 2.
- Memory configuration:
 - L1P: 32 KB program cache
 - L1D: 32 KB data cache
 - L2: 64 KB cache
- The algorithm uses 6 EDMA channels. Channel 0 to 5 use a maximum of 6 PARAM sets.

references

1.	ITU-T T.800 ISO/IEC 15444-1	Information technology – JPEG 2000 image coding system: Core coding system (2004)
2.	ITU-T T.803 ISO/IEC 15444-4	Information technology -- JPEG 2000 image coding system: Conformance Testing (2004)
3.	DCI Specifications	Digital Cinema System Specification Version 1.2, March 07, 2008.

glossary

Constants	Elements that go into const memory section
Scratch	Memory space that can be reused across different instances of the algorithm or across different algorithms
Shared	Sum of Constants and Scratch
Instance	Memory that contains persistent information - allocated for each instance of the algorithm

acronyms

XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media



DMA	Direct Memory Access
EVM	Evaluation Module
JPEG	Joint Picture Expert Group
MJPEG	Motion JPEG
ISO	International Organization for Standardization
ITU-T	International Telecommunications Union – Telecommunications Standardization Sector

PRODUCT PREVIEW



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive & Transportation	www.ti.com/automotive
Communications & Telecom	www.ti.com/communications
Computers & Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energyps
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics & Defense	www.ti.com/space-avionics-defense
Video & Imaging	www.ti.com/video

TI E2E Community e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas
75265 Copyright© 2016, Texas Instruments Incorporate

PRODUCT PREVIEW



