HEVC/H.265 Main Profile Encoder (v02.00.01) on TMS320C6678 Platform

FEATURES

- **Supports encoding of HEVC Main, Main Still profile bitstreams up to level 5.0**
- **Supports arbitrary resolutions from 128x96 up to 4096x2160**
- **Supports standard resolutions which are multiple of 2**
- **Supports YUV 4:2:0 Planar Chroma format**
- **Supports encoding progressive content**
- **Supports SEI and VUI parameters encoding.**
- **Supports I , P and B frame encoding**
- **Supports CTU sizes 64x64,32x32,16x16**
- **Supports RDO based encoding**
- **Supports multiple slice, multiple tile encoding**
- **Supports multiple reference frame encoding**
- **Supports encoding of streams with Wave front parallel processing feature**
- **Supports Low delay and Random access configurations**
- **Supports encoding of streams with scaling matrices**
- **Supports Deblocking and SAO features**
- **Supports encoding with dependent slices**
- **Supports insertion of IDR frame at random point with force frame control**
- **Supports constrained intra prediction**
- **Supports AIR(Adaptive Intra Refresh) with cyclic intra macroblocks**
- **Supports user controllable quantization parameter range, initial quantization parameter, HRD buffer size.**
- **Supports separate Cb and Cr quantization parameter control**
- **Supports user controlled Quarter pel & Half pel MV accuracy**
- **Supports user controlled in loop filter & SAO features which can be enabled/disabled at picture offset.**
- **Supports transform skip and trans quant bypass mode**
- **Supports to control the balance between encoding speed and quality by using user definable encoding preset option**
- **Supports call back API functions at CTU row level decoding**
- **Supports change of frame rate, bitrate dynamically**
- **Supports user controlled IDR frequency control**
- **Supports user configurable group of pictures (GOP) length and different GOP structures.**
- **Supports capability to generate only header**
- **Encoder library validated on DSPC-8681 and DSPC-8682 card based on TMS320C6678 platform**
- **The other explicit features that TI's HEVC Main Profile Encoder supports are**
  - **eXpressDSP Digital Media (XDM IVIDENC2) interface compliant**
  - **TI's Multicore interface(IVIDMC3) compliant**
  - **Independent of any operating system (DSP/BIOS, Linux etc)**
  - **Cache aware Encoder library Ability to get plugged in any multimedia frameworks (eg. MCSDK, Codec Engine, OpenMax, GStreamer, etc)**

DESCRIPTION

HEVC/H265 is video compression standard from ITU-T Video Coding Experts Group and the ISO/IEC Moving Pictures Experts Group successor to H264/MPEG4 AVC. Higher Data compression ratio is achieved compared to H.264/MPEG-4 AVC at the same level of video quality. It can alternatively be used to provide substantially improved video quality at the same bit rate. It can support 8K UHD and resolutions up to 8192×4320

This project is developed and validated on DSPC- 8681 and DSPC-8682 cards based on TMS320C6678 platform using Code Composer Studio version 5.5.0.00077 and code generation tools version 7.4.6.

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Performance and Memory Summary

This section describes the performance and memory usage of the HEVC Main profile Encoder tested on DSPC-8681 and DSPC-8682 cards based on TMS320C6678 platform.

Table 1 Configuration Table

CONFIGURATION	ID
HEVC Main Profile, IBB, Random Access, Multi chip(6 Chips)	H265MP_ENC_001
HEVC Main Profile, IBB, Random Access, Multi chip(3 Chips)	H265MP_ENC_002
HEVC Main Profile, IBB, Random Access, Multi core(2 Chips)	H265MP_ENC_003
HEVC Main Profile, IPP, Low Delay, Multi Chip(2 Chips)	H265MP_ENC_004
HEVC Main Profile, IPP, Low Delay, Multi Chip(19 Cores)	H265MP_ENC_005
HEVC Main Profile, IBB, Random Access, Multi core(1 Chip)	H265MP_ENC_006
HEVC Main Profile, IBB, Random Access, Multi core(8 Chips)	H265MP_ENC_007

Table 2 Cycles Information - Profiled on DSPC-8681 card with Code Generation Tools Version 7.4.6

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1)		
	TEST DESCRIPTION	AVERAGE(2)	PEAK(3)
H265MP_ENC_001	Airshow_p1920x1080_420p.yuv, YUV420, Random Access, IBB @ 10Mbps @ 60 frames per second	1131	1156
H265MP_ENC_002	Airshow_p1920x1080_420p.yuv, YUV420, Random Access, IBB @ 5Mbps @ 30 frames per second	1083	1103
	Airshow_p1280x720_420p.yuv, YUV420, Random Access, IBB @ 6Mbps @ 60 frames per second	1123	1140
H265MP_ENC_003	Airshow_p1280x720_420p.yuv, YUV420, Random Access, IBB @ 3Mbps @ 30 frames per second	749	761
H265MP_ENC_004	Shyam_p1920x1080_420p.yuv, YUV420, Low Delay, IPP @ 2Mbps @ 60 frames per second	1225	1231
H265MP_ENC_005	Shyam_p1920x1080_420p.yuv, YUV420, Low Delay, IPP @ 4Mbps @ 60 frames per second	1227	1229
H265MP_ENC_006	Airshow_p720x480_420p.yuv, YUV420, Random Access, IBB @ 2Mbps @ 60 frames per second	976	989
H265MP_ENC_007	Airshow_p3840x2160_420p.yuv, YUV420, Random Access, IBB @ 16Mbps @ 30 frames per second	1158	1186

(1) Measured with C66x DSP 1250MHz clock, DDR3 1333MHZ clock, Program memory in SL2 memory, I/0 buffers in external memory and stack in internal L2 memory with cache configurations: 32KB L1P Program cache, 32KB L1D Data cache and 64KB L2 cache. Performance is measured using MCSDK Video version 2.2.0.42 to make sure system overheads are included. There could be a variation of approximately 2-3% in the values.
(2) Average cycles are calculated as maximum of moving average for frames in 1 sec, multiplied with frame rate to get per second Mhz.
(3) Peak cycles are calculated as maximum of moving average for frames in 0.5 sec, multiplied with frame rate to get per second Mhz.

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Table 3 Memory Statistics of HEVC Encoder with Code Generation Tools Version 7.4.6

CONFIGURATION ID	MEMORY STATISTICS[1][2]					
	PROGRAM MEMORY[4]	DATA MEMORY [3]				TOTAL
		PERSISTENT	CONSTANT	SHARED	SCRATCH	
H265MP_ENC_001	953	19	27	35264	0	36263
H265MP_ENC_002	953	19	27	42795	0	43794
H265MP_ENC_003	953	19	27	27999	0	28998
H265MP_ENC_004	953	19	27	49297	0	50296
H265MP_ENC_005	953	19	27	44346	0	45345
H265MP_ENC_006	953	19	27	17389	0	18388
H265MP_ENC_007	953	19	27	111157	0	112156

(1) All these memory requirements are for HEVC Main Profile Encoder library only. They do not include any memory requirements from application side. Stack, heap and code requirements for application are extra.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) Program code is stored in SL2 memory.

Table 4 Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL[1] [2]					
	LOCAL L2				SHARED L2[3]	TOTAL
	CONSTANTS	PERSISTENT	SCRATCH	STACK		
H265MP_ENC_001 H265MP_ENC_002 H265MP_ENC_003 H265MP_ENC_004 H265MP_ENC_005 H265MP_ENC_006 H265MP_ENC_007	0	0	283	8	1454	1745

(1) Internal memory requirements are for each individual core.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) Encoder tables are placed in Shared L2 (MSMC) memory.

Table 5 Cache/SRAM configuration [1]

NAME	AVAILABLE	CACHE	SRAM
L1P (Program Memory)	32KB	32KB	0KB
L1D(Data Memory)	32KB	32KB	0KB
L2	512KB	64KB	448KB

(1) All above mentioned numbers are for all configurations.

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Table 6 EDMA Configuration (1) (5)(6)

TC Q	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM(3)
Usage	R/W to DDR/L2	-	-	-	-	-
Priority(2)	0	-	-	-	-	-
EDMA Channels	8	-	-	-	8(4)	64
QDMA Channels	-	-	-	-	0(4)	8
Num PARAMS	48(4)	-	-	-	48(4)	512

(1) All above mentioned numbers are for all configurations (H265MP_ENC_001, H265MP_ENC_002, H265MP_ENC_003, H265MP_ENC_004, H265MP_ENC_005, H265MP_ENC_006 and H265MP_ENC_007).
(2) Lesser number corresponds to higher TC priority. Default priority is TC0 > TC1 > TC2 > TC3. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.
(3) Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip for a channel controller. It does NOT indicate the maximum number requested by the codec.
(4) Same EDMA channel is used to copy data to DDR and to L2 memory at different instances.
(5) Above configuration table specifies EDMA hardware usage for each core in multicore/multichip scenario.
(6) Core 0,1,2,3 uses EDMA CC1 and Core 4,5,6,7 uses EDMA CC2.

Notes

- I/O buffers:
  - Input buffer size = 3060 K-bytes (for 1920x1088 resolution, YUV420)
  - Input buffer size = 12150 K-bytes (for 3840x2160 resolution, YUV420)
  - Output buffer size = 3584 K-bytes

References

- ISO/IEC 23008-2:2013 Infrastructure of audiovisual services - Coding of moving video: High efficiency video encoding.
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard).
- HEVC Main Profile Encoder on TMS320C6678 Platform User's Guide.

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
HEVC	High Efficiency Video Codec
DMA	Direct Memory Access
ISO	International organization for standardization
EVM	Evaluation Module
AVC	Advanced Video Codec
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

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