HEVC/H.265 Main Profile Decoder (v01.00.00) on TMS320C6678 Platform

FEATURES

- **Supports decoding of HEVC Main, Main Still profile bitstreams up to level 5.0**
- **Supports arbitrary resolutions from 64x64 up to 4kx2k**
- **Supports width and height as non multiple of 16**
- **Supports YUV 4:2:0 Planar Chroma format**
- **Supports decoding progressive content**
- **Supports SEI and VUI parameters decoding.**
- **Supports B frame decoding**
- **Supports CTU sizes 64x64,32x32,16x16**
- **Supports multiple slice, multiple tile decoding**
- **Supports decoding of streams with Wave front parallel processing**
- **Supports bitstreams encoded with Low delay and Random access configurations**
- **Supports Multiple reference frames**
- **Supports decoding of streams with scaling matrices**
- **Supports decoding of streams with Weighted Prediction**
- **Supports decoding PCM encoded CTUs**
- **Supports Deblocking and SAO features decoding**
- **Supports dependent slice decoding**
- **Supports IDR & CRA frame decoding**
- **Supports IRAP frame decoding**
- **Supports TSA,STSA feature decoding**
- **Supports decoding frames with LTRP feature**
- **Supports AMP feature decoding**
- **Supports TMVP feature decoding**
- **Supports constrained intra prediction**
- **Supports transform skip and trans quant bypass mode**
- **Supports unrestricted motion vectors which allows motion vectors to be outside frame boundary**
- **Supports call back API functions at CTU row level decoding**
- **Supports decoding video elementary stream in big endian format**
- **Supports decode only header mode**
- **Error resilient codec, supports error codes**
- **Supports error concealment at slice level, CTU level**
- **Decoder library validated on DSPC-8681 and DSPC-8682 card based on TMS320C6678 platform**
- **The other explicit features that TI's HEVC Main Profile Decoder supports are**
  - **eXpressDSP Digital Media (XDM IVIDDEC3) interface compliant**
  - **TI's Multicore interface(IVIDMC3) compliant**
  - **Independent of any operating system (DSP/BIOS, Linux etc)**
  - **Cache aware Decoder library Ability to get plugged in any multimedia frameworks (eg. MCSDK, Codec Engine, OpenMax, GStreamer, etc)**

DESCRIPTION

HEVC/H265 is video compression standard from ITU-T Video Coding Experts Group and the ISO/IEC Moving Pictures Experts Group successor to H264/MPEG4 AVC. Higher Data compression ratio is achieved compared to H.264/MPEG-4 AVC at the same level of video quality. It can alternatively be used to provide substantially improved video quality at the same bit rate. It can support 8K UHD and resolutions up to 8192×4320

This project is developed and validated on DSPC- 8681 and DSPC-8682 cards based on TMS320C6678 platform using Code Composer Studio version 5.5.0.00077 and code generation tools version 7.4.6.

PRODUCT PREVIEW

Performance and Memory Summary

This section describes the performance and memory usage of the HEVC Main profile Decoder tested on DSPC-8681 and DSPC-8682 cards based on TMS320C6678 platform.

Table 1 Configuration Table (1)

CONFIGURATION	ID
HEVC Main Profile, IBB, Random Access, Multi core(8 Cores)	H265MP_DEC_001
HEVC Main Profile, IBB, Low Delay, Multi core(8 Cores)	H265MP_DEC_002
HEVC Main Profile, IBB, Random Access, Multi core(4 Cores)	H265MP_DEC_003
HEVC Main Profile, IBB, Low Delay, Multi core(4 Cores)	H265MP_DEC_004
HEVC Main Profile, IPP, Low Delay, Multi core(5 Cores)	H265MP_DEC_005
HEVC Main Profile, IBB, Random Access, Single Core	H265MP_DEC_006
HEVC Main Profile, IBB, Random Access, Multi chip(16 cores)	H265MP_DEC_007

(1) Multichip configuration H265MP_DEC_007 mandates 2 equally divided tiles either horizontally or vertically. Uses 2 EDMA CC0 channels for interchip data transfer

Table 2 Cycles Information - Profiled on DSPC-8681 card with Code Generation Tools Version 7.4.6

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1)		
	TEST DESCRIPTION	AVERAGE(2)(4)	PEAK(3)(4)(5)
H265MP_DEC_001	Airshow_p1920x1080_420p_8Mbps_RA.265, YUV420, Random Access, IBB @ 8Mbps @ 60 frames per second	1011	1246
H265MP_DEC_002	Airshow_p1920x1080_420p_8Mbps_LD.265, YUV420, Low Delay, IBB @ 8Mbps @ 60 frames per second	1151	1246
H265MP_DEC_003	Airshow_p1280x720_420p_4Mbps_RA.265, YUV420, Random Access, IBB @ 4Mbps @ 60 frames per second	784	971
H265MP_DEC_004	Airshow_p1280x720_420p_4Mbps_LD.265, YUV420, Low Delay, IBB @ 4Mbps @ 60 frames per second	957	1099
H265MP_DEC_005	Shyam_p1920x1080_420p_4Mbps_LD.265, YUV420, Low Delay, IPP @ 4Mbps @ 60 frames per second	1187	1351
H265MP_DEC_006	Airshow_p720x480_420p_1Mbps_RA.265, YUV420, Random Access, IBB @ 1Mbps @ 60 frames per second	864	1032
H265MP_DEC_007	Airshow_p3840x2160_420p_16Mbps_RA.265, YUV420, Random Access, 2 tiles, IBB @ 16Mbps @ 30 frames per second	1230	1270

(1) Measured with C66x DSP 1250MHz clock, DDR3 1333MHZ clock, Program memory in SL2 memory, I/0 buffers in external memory and stack in internal L2 memory with cache configurations: 32KB L1P Program cache, 32KB L1D Data cache and 64KB L2 cache. In case of Multichip scenario hyper link is used for data communication between chips. Performance is measured using MCSDK Video version 2.2.0.42 to make sure system overheads are included. There could be a variation of approximately 2-3% in the values.
(2) Average cycles are calculated as maximum of moving average of 30 frames, multiplied with 60 to get per second Mhz.
(3) Peak cycles are calculated as maximum of moving average of 3 frames multiplied with 60 to get per second Mhz.
(4) Performance is considered across the frames with moving average of 3 frames less than target bit rate to allow average bit rate for encoder.
(5) Peak cycles of 2-3% of frames are considered to go beyond 1250 MHz.

Table 3 Memory Statistics of HEVC Decoder with Code Generation Tools Version 7.4.6

CONFIGURATION ID	MEMORY STATISTICS(1)(2)					
	PROGRAM MEMORY(4)	DATA MEMORY (3) (5)				TOTAL
		PERSISTENT	CONSTANT	SHARED	SCRATCH	
H265MP_DEC_001 H265MP_DEC_002	574	88	0	96045	0	96133
H265MP_DEC_003 H265MP_DEC_004	574	44	0	47260	0	47304
H265MP_DEC_005	574	55	0	96045	0	96100
H265MP_DEC_006	574	11	0	21240	0	21251

(1) All these memory requirements are for HEVC Main Profile Decoder library only. They do not include any memory requirements from application side. Stack, heap and code requirements for application are extra.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) The memory requirements given in Table 3 are calculated for1920x1080 resolution and YUV 420 Chroma sub sampling.
(4) Program code is stored in SL2 memory.
(5) Typical input and output buffers for 1920x1080 resolutions with YUV planar 4:2:0 formats are as follows.
Input Buffer: 3072 KB
Output Buffer: 3060 KB

Table 4 Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL(1) (2)					
	LOCAL L2				SHARED L2(3)	TOTAL
	CONSTANTS	PERSISTENT	SCRATCH	STACK		
H265MP_DEC_001 H265MP_DEC_002 H265MP_DEC_003 H265MP_DEC_004 H265MP_DEC_005 H265MP_DEC_006	0	0	390	4	1007	1401

(1) Internal memory requirements are for each individual core.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) Decoder tables are placed in Shared L2 (MSMC) memory.

Table 5 Cache/SRAM configuration (1)

NAME	AVAILABLE	CACHE	SRAM
L1P (Program Memory)	32KB	32KB	0KB
L1D(Data Memory)	32KB	32KB	0KB
L2	512KB	64KB	448KB

(1) All above mentioned numbers are for all configurations.

Table 6 EDMA Configuration (1) (5)(6)

TC Q	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM(3)
Usage	R/W to DDR/L2	-	-	-	-	-
Priority(2)	0	-	-	-	-	-
EDMA Channels	10	-	-	-	10(4)	64
QDMA Channels	-	-	-	-	0(4)	8
Num PARAMS	65	-	-	-	65(4)	512

(1) All above mentioned numbers are for all configurations (H265MP_DEC_001, H265MP_DEC_002, H265MP_DEC_003, H265MP_DEC_004, H265MP_DEC_005 and H265MP_DEC_006).
(2) Lesser number corresponds to higher TC priority. Default priority is TC0 > TC1 > TC2 > TC3. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.
(3) Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip for a channel controller. It does NOT indicate the maximum number requested by the codec.
(4) Same EDMA channel is used to copy data to DDR and to L2 memory at different instances.
(5) Above configuration table specifies EDMA hardware usage for each core in multicore scenario.
(6) Core 0,1,2,3 uses EDMA CC1 and Core 4,5,6,7 uses EDMA CC2.

Notes

- I/O buffers:
  - Input buffer size = 3072 K-bytes (for 1920x1088 resolution, YUV420)
  - Output buffer size = 3060 K-bytes (for decode 1920x1088 resolution)

References

- ISO/IEC 23008-2:2013 Infrastructure of audiovisual services - Coding of moving video: High efficiency video encoding.
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard).
- HEVC Main Profile Decoder on TMS320C6678 Platform User's Guide.

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
HEVC	High Efficiency Video Codec
DMA	Direct Memory Access
ISO	International organization for standardization
EVM	Evaluation Module
AVC	Advanced Video Codec
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications	
Automotive & Transportation	www.ti.com/automotive
Communications & Telecom	www.ti.com/communications
Computers & Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energyapps
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics & Defense	www.ti.com/space-avionics-defense
Video & Imaging	www.ti.com/video
TI E2E Community	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265