H264 High Profile Encoder (v01.00.00) on TMS320C6678 Platform

FEATURES

- **Supports Baseline, Main, High profiles up to level 4.0**
- **Supports B frame encoding**
- **Supports arbitrary resolutions from 64x64 upto 4kx4k**
- **Supports width and height as non multiple of 16**
- **Supports YUV 4:2:0 Planar chroma format**
- **Supports Progressive and field based interlaced encoding with different controls as MRF, SPF, ARF**
- **Supports control to have bottom field first for interlaced coding**
- **Supports user controlled partition size till 8x8 block for inter prediction**
- **Supports user controlled all intra modes(16x16,8x8,4x4)**
- **Supports user controllable quantization parameter range, initial quantization parameter, HRD buffer size**
- **Supports 8x8, 4x4 transform block size**
- **Supports separate Cb and Cr quantization parameter control**
- **Supports both CABAC and CAVLC entropy coding**
- **Supports user controlled quarter-pel interpolation and integer pel for motion estimation**
- **Supports in-loop filtering which can be switched off picture as well for slice boundaries**
- **Supports unrestricted motion vectors which allows motion vectors to be outside frame boundary**
- **Supports running on multiple DSP (66x) cores**
- **Supports multiple slices per picture based on number of macroblocks in each slice**
- **Support to control the balance between encoder speed and quality by using user definable encoding present option**
- **Supports constrained intra prediction**
- **Supports user controlled POC types(0,1,2)**
- **Supports user configurable parameters like log2_max_frame_num_minus4 and chroma_qp_index_offset**
- **Supports insertion of IDR frame at random point with force frame control**
- **Supports AIR(Adaptive Intra Refresh) with cyclic intra macro blocks**
- **Supports change of frame rate, bit rate parameters dynamically**
- **Supports user controlled IDR frequency control**
- **Supports user configurable Group of pictures(GOP) length and different GOP Structures: Non uniform (IBBP) and uniform (BBIBBP)**
- **Supports capability to generate only header Graceful exit under error conditions is supported**
- **Encoder library validated on TMS320C6678 hardware EVM**
- **The other explicit features that TI's H264 High Profile Encoder supports are**
  - **eXpressDSP Digital Media (XDM IVIDENC2) interface compliant**
  - **Independent of any operating system (DSP/BIOS, Linux etc)**
  - **Cache aware encoder library Ability to get plugged in any multimedia frameworks (eg. MCSDK, Codec Engine, OpenMax, GStreamer, etc)**

PRODUCT PREVIEW

DESCRIPTION

H264 is video compression standard from ITU-T Video Coding Experts Group and the ISO/IEC Moving Pictures Experts Group.

This project is developed and validated on TMS320C6678 EVM using Code Composer Studio version 5.1.0.09000 and code generation tools version 7.4.1.

Performance and Memory Summary

This section describes the performance and memory usage of the H264 High Profile encoder tested on TMS320C6678 EVM

Table 1 Configuration Table

CONFIGURATION	ID
H264 High Profile, VBR, IBBP, CABAC, Single Core	H264HP_ENC_001
H264 Base Profile, CBR, IPPP, CAVLC, Single Core	H264HP_ENC_002
H264 High Profile, VBR, IBBP, CABAC, Multi Core(8 Cores)	H264HP_ENC_003
H264 Base Profile, CBR, IPPP, CAVLC, Multi Core(4 Cores)	H264HP_ENC_004
H264 Base Profile, CBR, IPPP, CAVLC, Multi Core(2 Cores)	H264HP_ENC_005

Table 2 Cycles Information - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.1

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) (1)		
	TEST DESCRIPTION	AVERAGE(2)(4)	PEAK(3)(4)
H264HP_ENC_001	Airshow_p1920x1080_420p_8bit.yuv, YUV420, CABAC, VBR, IBBP @ 8Mbps @ 30 frames per second	7360	7618
	Fruits_i1920x1080_420p_8bit.yuv , YUV420, CABAC, VBR, IBBP @ 8Mbps @ 30 frames per second	6157	6268
	Airshow_p1280x720_420p_8bit.yuv, YUV420, CABAC, VBR, IBBP @ 4Mbps @ 30 frames per second	3346	3409
H264HP_ENC_002	Shyam_p720x480_420p_8bit.yuv, YUV420, CAVLC, CBR, IPPP @ 2Mbps @ 30 frames per second	758	837(5)
H264HP_ENC_003	Airshow_p1920x1080_420p_8bit.yuv, YUV420, CABAC, VBR, IBBP @ 8Mbps @ 30 frames per second	1209	1219
	Fruits_i1920x1080_420p_8bit.yuv , YUV420, CABAC, VBR, IBBP @ 8Mbps @ 30 frames per second	1269	1337
	Airshow_p1280x720_420p_8bit.yuv, YUV420, CABAC, VBR, IBBP @ 4Mbps @ 30 frames per second	564	585
H264HP_ENC_004	Shyam_p1920x1080_420p_8bit.yuv, YUV420, CAVLC, CBR, IPPP @ 5Mbps @ 30 frames per second	1171	1326(5)
H264HP_ENC_005	Shyam_p1280x720_420p_8bit.yuv, YUV420, CAVLC, CBR, IPPP @ 3Mbps @ 30 frames per second	983	1079(5)

(1) Measured with C66x DSP 1250MHz clock, DDR3 1333MHZ clock, Program memory in SL2 memory, I/0 buffers in external memory and stack in internal L2 memory with cache configurations: 32KB L1P Program cache, 32KB L1D Data cache and 64KB L2 cache. Performance is measured using MCSDK test framework version 2.1.0.4 to make sure system overheads are included. There could be a variation of approximately 2-3% in the values.
(2) Average cycles are calculated as maximum of moving average of 30 frames, multiplied with 30 to get per second Mhz.
(3) Peak cycles are calculated as maximum of moving average of 3 frames multiplied with 30 to get per second Mhz. Peak cycles are considered only after initial 2 seconds of encoding (to allow encoder to reach steady state).
(4) Performance is measured across the process call after all cores reach same sync point over 90 frames.
(5) Instantaneous peak cycles are calculated as maximum frame cycles multiplied by 30 to get per second Mhz.

Table 3 Memory Statistics of TMS320C6678 with Code Generation Tools Version 7.4.1

CONFIGURATION ID	MEMORY STATISTICS[1][2]					
	PROGRAM MEMORY[4]	DATA MEMORY [3] [5]				TOTAL
		PERSISTENT	CONSTANT	SHARED	SCRATCH	
H264HP_ENC_001 H264HP_ENC_002	1143	9529	22	19303	3127	31981
H264HP_ENC_003	1143	76047	22	19322	3519	98910
H264HP_ENC_004	1143	14624	22	19311	3295	37252
H264HP_ENC_005	1143	7312	22	19311	3183	29828

(1) All these memory requirements are for H264 High profile encoder library only. They do not include any memory requirements from test application side. Stack, heap and code requirements for test-application are extra.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
(3) The memory requirements given in Table 3 are calculated for1920x1080 resolution and YUV 420 Chroma sub sampling.
(4) Program code is stored in SL2 memory.
(5) Typical input and output buffers for 1920x1080 resolutions with yuv planer 4:2:0 formats are as follows.
Input Buffer: 3060KB
Output Buffer: 500KB

Table 4 Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL[1] [2]					
	LOCAL L2				SHARED L2	TOTAL
	CONSTANTS	PERSISTENT	SCRATCH	STACK		
H264HP_ENC_001 H264HP_ENC_002	0	0	230	16	31	277

(1) Internal memory requirements are for each individual core.
(2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).

Table 5 Cache/SRAM configuration [1]

NAME	AVAILABLE	CACHE	SRAM
L1P (Program Memory)	32KB	32KB	0KB
L1D(Data Memory)	32KB	32KB	0KB
L2	512KB	64KB	448KB

(1) All above mentioned numbers are for all configurations.

PRODUCT PREVIEW

Table 6 EDMA Configuration (1) (5)(6)

TC Q	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM(3)
Usage	R/W to DDR/L2	-	-	-	-	-
Priority(2)	0	-	-	-	-	-
EDMA Channels	8	-	-	-	8(4)	64
QDMA Channels	-	-	-	-	0(4)	8
Num PARAMS	38	-	-	-	38(4)	512

(1) All above mentioned numbers are for all configurations (H264HP_ENC_001, H264HP_ENC_002, H264HP_ENC_003, H264HP_ENC_004, H264HP_ENC_005).
(2) Lesser number corresponds to higher TC priority. Default priority is TC0 > TC1 > TC2 > TC3. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.
(3) Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip for a channel controller. It does NOT indicate the maximum number requested by the codec.
(4) Same EDMA channel is used to copy data to DDR and to L2 memory at different instances.
(5) Above configuration table specifies EDMA hardware usage for each core in multicore scenario.
(6) Core 0,1,2,3 uses EDMA CC1 and Core 4,5,6,7 uses EDMA CC2.

Notes

- I/O buffers:
  - Input buffer size = 3060 K-bytes (for 1920x1088 resolution, YUV420)
  - Output buffer size = 500 K-bytes (for encoding 1920x1088 resolution)

References

- ISO/IEC 14496-10:2005 Information technology -- Coding of audio-visual objects -- Part 10: Advanced Video Coding.
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard).
- H264 High Profile Encoder on TMS320C6678 Platform User's Guide.

Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

Acronyms

Acronym	Description
DMA	Direct Memory Access
ISO	International organization for standardization
EVM	Evaluation Module
AVC	Advanced Video Codec
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

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