- **eXpressDSP™ Digital Media (XDM IVIDDEC1.2 Compliant)**
- **Up to level 5 features of the High Profile (HP) supported**
- **Validated on the TMS320C6678 EVM**
- **Progressive, interlaced, Picture Adaptive Frame Field (PicAFF) and Macro-block Adaptive Frame Field (MBAFF) type picture decoding supported**
- **Multiple slices and multiple reference frames supported**
- **CAVLC and CABAC decoding supported**
- **All intra-prediction and inter-prediction modes supported**
- **Up to 16 MV per MB supported**
- **Frame based decoding supported**
- **Picture width greater than 32 pixels supported**
- **Tested for compliance with JM version 16.1 reference decoder**
- **Long term reference frame and Adaptive reference picture marking supported**
- **Reference picture list reordering supported**
- **PCM Macroblock decoding supported**
- **Gaps in frame number supported**
- **Error resiliency and concealment supported**
- **SEI and VUI parsing supported**
- **Supports ELF ABI format.**
- **Supports "ecpy" for EDMA and "IRES" interface.**
- **Support for single- or multi- (2 or 4) core implementation.**
- **ASO and FMO error concealment features supported in single core implementation.**
- **Redundant slices supported in single core implementation.**

DESCRIPTION

H.264 is a popular video coding algorithm enabling high quality multimedia services on a limited bandwidth network. H264 is validated on TMS320C6678 EVM with Code Composer Studio version 5.2.1.00018 and code generation tools version 7.4.0.

PRODUCT PREVIEW

Summary of performance

Table 1. Configuration Table

CONFIGURATION	ID
Baseline Profile up to Level 1, single core	H264_DEC_1Core_L1
Baseline Profile up to Level 2, single core	H264_DEC_1Core_L2
Baseline Profile up to Level 3, single core	H264_DEC_1Core_L3
Baseline Profile up to Level 4, single core	H264_DEC_1Core_L4
Baseline Profile up to Level 5, single core	H264_DEC_1Core_L5
Baseline | Main | High Profiles, up to Level 3, two DSP cores	H264_DEC_2Core_L3
Baseline | Main | High Profiles, up to Level 4, two DSP cores	H264_DEC_2Core_L4
Baseline | Main | High Profiles, up to Level 5, two DSP cores	H264_DEC_2Core_L5
Baseline | Main | High Profiles, up to Level 4, four DSP cores	H264_DEC_4Core_L4

Table 2. Cycles Information – Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.4.0

CONFIGURATION	PERFORMANCE STATISTICS (IN MILLION CYCLES PER SECOND) [1]		
	TEST DESCRIPTION	AVERAGE [2]	PEAK [3]
H264_DEC_1Core_L1	174x144_mobile_IPP_CAVLC_16mv_512kbps_30fps.264	35	44
H264_DEC_1Core_L2	352x288_mobile_IPP_CAVLC_16mv_1Mbps_25fps.264	99	111
H264_DEC_1Core_L3	D1p720x480_parkrun_420p_IPP_CAVLC_16mv_Progr_4Mbps_30fps(BP stream)	302	330

	football_704x480_IBBP_CABAC_16mv_Intlcd_4Mbps_30fps (MP Stream)	497	745
	football_704x480_IBBP_CABAC_16mv_Intlcd_4Mbps_hp_30fps (HP Stream)	518	718
H264_DEC_1Core_L4	720p_parkrun_420p_IBBP_CABAC_16mv_Progr_4Mbps_30fps (HP Stream)	931	1103
H264_DEC_2Core_L4	720p_parkrun_420p_IBBP_CABAC_16mv_Progr_4Mbps_30fps (HP Stream)	615	766
H264_DEC_4Core_L4	720p_parkrun_420p_IBBP_CABAC_16mv_Progr_4Mbps_30fps (HP Stream)	372	-
	fullHD_fb_IBBP_CABAC_16mv_Progr_8Mbps_30fps (HP Stream)	789	-

[1]Program placed in external memory and in MSMCSRAM, I/O buffers in external memory, stack in L2SRAM, 32-KB L1P Cache, 32-KB L1D Cache, 64-KB L2 Cache, DDR speed at 1333 MHz, and DSP at 1250 MHz.
[2]Based on peak of total cycles consumed per one second.
[3]Based on peak of rolling average cycles over 3 frames multiplied by fps.

Table 3. Memory Statistics - Generated with Code Generation Tools Version 7.4.0

CONFIGURATION ID	MEMORY STATISTICS[4]				
	PROGRAM MEMORY[5]	DATA MEMORY			
		INTERNAL	EXTERNAL[6]	STACK	TOTAL DATA
H264_DEC_1Core_L1	769.75	95.21	1177.33	24	1296.54
H264_DEC_1Core_L2	769.75	102.04	1928.17	24	2054.41
H264_DEC_1Core_L3	769.75	102.04	4359.81	24	4485.85
H264_DEC_1Core_L4	769.75	189.02	14041.69	24	14254.71
H264_DEC_1Core_L5	769.75	187.07	21407.75	24	21628.82
H264_DEC_2Core_L3	769.75	311.68	4359.81	24	4695.49
H264_DEC_2Core_L4	769.75	322.86	11363.69	24	11710.55
H264_DEC_2Core_L5	769.75	335.78	18729.75	24	19089.53
H264_DEC_4Core_L4	780	603.33	22619.68	24	24127.01

[4]All memory requirements are expressed in kilobytes (1 kilobyte = 1024 bytes) and there could be a variation of around 1-2% in numbers.
[5]744.34 KB placed in MSMCSRAM memory and rest of the memory placed in external memory.
[6]Does not include DPB. External memory is the accumulation of external persistent buffers.
Internal Data Memory = Const Memory + Scratch Memory + Persistent Memory for Single Core
Internal Data Memory = Const Memory + (Scratch + Persistent) Memory for Core1 + (Scratch + Persistent) Memory for Core2 for two core implementation.
Internal Data Memory = Const Memory + (Scratch + Persistent) Memory for Core1 + (Scratch + Persistent) Memory for Core2 + + (Scratch + Persistent) Memory for Core3 + (Scratch + Persistent) Memory for Core4 for four core implementation.

Table 4. Internal Data Memory Split-up

CONFIGURATION ID	DATA MEMORY – INTERNAL[7]					
	SHARED					INSTANCE[8]
	CONSTANTS	SCRATCH				
		CORE 1	CORE 2	CORE 3	CORE 4	
H264_DEC_1Core_L1	23.49	62.27	--	--	--	9.45
H264_DEC_1Core_L2	23.49	69.09	--	--	--	9.46
H264_DEC_1Core_L3	23.49	69.09	--	--	--	9.46
H264_DEC_1Core_L4	23.49	156.08	--	--	--	9.45
H264_DEC_1Core_L5	23.49	164.13	--	--	--	9.45
H264_DEC_2Core_L3	23.49	149.09	120.20	--	--	18.9
H264_DEC_2Core_L4	23.49	156.08	124.39	--	--	18.9
H264_DEC_2Core_L5	23.49	164.13	129.26	--	--	18.9
H264_DEC_4Core_L4	23.49	156.08	124.39	156.08	124.39	18.9

[7]Constants are placed in MSMCSRAM and Scratch buffers are placed in L2SRAM. All memory requirements are expressed in kilobytes and there could be a variation of around 1-2% in numbers.
[8]I/O buffers not included. Some of the instance memory buffers could be scratch

notes

- Evaluation version performance values may be higher than the values specified in the performance table.
- Display buffer for YUV420 planar format is 4.26MB for 720x480 resolution including the padding samples.
- Input buffer to algorithm is assumed to have at least one encoded frame data. Maximum input buffer size for input bitstream allowed is 6 MB

- The library requests for 256 bytes shared L2SRAM memory region from the framework during run-time for inter-core communication.
- The performances obtained in Table 2 are sensitive to algorithm code placement. Refer the sample linker file provided in the test application setup for algorithm code placement. Some of the code is placed in MSMCSRAM memory, as specified in linker file.

Table 5. Cache Configuration

	Core 1		Core 2		Core 3		Core 4	
	Available	Used	Available	Used	Available	Used	Available	Used
L1P	32KB	32 KB	32KB	32 KB	32KB	32 KB	32KB	32 KB
L1D	32KB	32 KB	32KB	32 KB	32KB	32 KB	32KB	32 KB
L2	512KB	64 KB	512KB	64 KB	512KB	64 KB	512KB	64 KB

Table 6. EDMA Configuration

TC Q's	TC 0	TC 1	TC 2	TC 3	Total	Max[9]
Usage	--	--	Writes to DDR	Writes to LL2 SRAM	-	-
Priority[10]	--	--	2	2	-	-
EDMA channels	--	--	6[11]	6[12]	12	64
QDMA channels	--	--	-	-	0	4
Num PARAMS	--	--	42	30	72	256

[9]Lesser number corresponds to higher TC priority. Default priority is 2. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.

[10]Max corresponds to the maximum number of EDMA channels or maximum number of PARAMS available on the chip. It does NOT indicate the maximum number requested by the codec.

[11]2 from master core and 1 from slave core in each core group.

[12]1from master and 2 from slave in each core group.

references

- ISO/IEC 14496-10:2005 (E) Rec. - Information technology – Coding of audio-visual objects – H.264 (E) ITU-T Recommendation.

glossary

Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm or across different algorithms
Shared	Sum of Constants and Scratch

Instance	Memory that contains persistent information - allocated for each instance of the algorithm

acronyms

625SD	Level 3.0 Maximum resolution format size 720x576
ABI	Application Binary Interface
CIF	Common Intermediate Format
CPB	Coded Picture Buffer
DMA	Direct Memory Access
EDMA	Enhanced Direct Memory Access
ELF	Executable and Linkable Format
EVM	Evaluation Module
QCIF	Quarter Common Intermediate Format
DMA	Direct Memory Access
SDTV	Standard definition television
VGA	Video Graphics Array (640x480 resolution)
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

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