

## AVC Intra & Ultra Encoder (v01.00.00) on TMS320C6678 Platform

### FEATURES

- Supports AVC Intra 50 encoding as per SMPTE RP 2027:2011
- Supports AVC Intra 100 encoding as per SMPTE RP 2027:2011
- Supports Panasonic AVC Intra 50 and AVC Intra 100
- Supports H264 High 10 Intra Profile up to level 4.2
- Supports H264 High 4:2:2 Intra Profile up to level 4.2
- Supports fixed frame size as per the AVC Intra standard
- Supports 4:2:0, 4:2:2 and 4:4:4 Chroma formats
- Supports both interlace(PAFF & MBAFF) and progressive sequence
- Supports customized scaling matrix
- Supports 8, 10 and 12 bit input pixel precision
- Supports 16x16, 8x8 and 4x4 intra prediction modes
- Supports user controllable quantization parameter range
- Supports both CABAC and CAVLC entropy coding
- Supports arbitrary video resolutions from 64x64 up to 4kx4k which are multiple of 2
- Supports 4x4 verses 8x8 transform adaptability at macro block level
- Supports algorithm to minimize the flickering artifacts
- Supports running on multiple DSP (66x) cores
- Supports separate Cb and Cr Quantization parameter control
- Supports big endian and little endian input
- Supports user configurable parameters like `log2_max_frame_num_minus4` and `chroma_qp_index_offset`
- Supports multiple slices encoding based on number of MBs in slice
- Graceful exit under error conditions is supported
- Supports dynamic slice resize for CABAC enabled AVC Intra 50 streams
- Does not support sub frame level data synchronization.
- Encoder library validated on TMS320C6678 hardware EVM
- The other explicit features that TI's AVC Intra & Ultra Encoder supports are
  - eXpressDSP Digital Media (XDM IVIDENC2) interface compliant
  - Independent of any operating system (DSP/BIOS, Linux etc)
  - Cache aware encoder library Ability to get plugged in any multimedia frameworks (eg. Codec Engine, OpenMax, GStreamer, etc)

### DESCRIPTION

AVC Intra & Ultra, the industry's most advanced compression technology, is a professional intra-frame video codec with bit rates of 50 and 100 Mb/s, Utilizing the High 10 Intra and High 4:2:2 Intra profiles of H.264. AVC Intra & Ultra provides high quality 10 bit and 12 bit intra frame coding. AVC Intra & Ultra, a fully compliant H.264 codec implementation, offers significantly better compression efficiency than old codec families (DVCPro HD). AVC Intra & Ultra is explicitly designed and optimized for broadcast and production use rather than low bandwidth distribution. This project is developed using Code Composer Studio version 5.1.0.09000 and code generation tools version 7.3.5.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Performance and Memory Summary

This section describes the performance and memory usage of the AVC Intra & Ultra encoder tested on TMS320C6678 EVM

**Table 1 Configuration Table**

CONFIGURATION	ID
AVC Intra 50 mode, YUV420, 10 bit, 8x8 Intra Pred, CABAC, Single Core	AVCIU_ENC_001
AVC Intra 50 mode, YUV420, 10 bit, 8x8 Intra Pred, CABAC, Multi Core(8 Cores)	AVCIU_ENC_002
AVC Intra 100 mode, YUV422, 10 bit, 8x8 Intra Pred, CAVLC, Single Core	AVCIU_ENC_003
AVC Intra 100 mode, YUV422, 10 bit, 8x8 Intra Pred, CAVLC, Multi Core(8 Cores)	AVCIU_ENC_004
AVC Ultra mode, 200Mbps, YUV444, 12 bit, 8x8 Intra Pred, CAVLC, Single Core	AVCIU_ENC_005
AVC Ultra mode, 200Mbps, YUV444, 12 bit, 8x8 Intra Pred, CAVLC, Multi Core(8 Cores)	AVCIU_ENC_006

### Cycles Information - Profiled on TMS320C6678 EVM with Code Generation Tools Version 7.3.5

CONFIGURATION ID	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) <sup>(1)</sup>		
	TEST DESCRIPTION	AVERAGE <sup>(2)(3)</sup>	PEAK <sup>(2)(3)</sup>
AVCIU_ENC_001	Airshow_p960x720_420p_10bit.yuv @ 30 frames per second	3869	3889
	Airshow_p1440x1080_420p_10bit.yuv @ 30 frames per second	8391	8421
	Fruits_i1440x1080_420p_10bit.yuv @ 60 fields per second	8992	9030
AVCIU_ENC_002	Airshow_p960x720_420p_10bit.yuv @ 30 frames per second	679	685
	Airshow_p1440x1080_420p_10bit.yuv @ 30 frames per second	1199	1345
	Fruits_i1440x1080_420p_10bit.yuv @ 60 fields per second	1650	1672
AVCIU_ENC_003	Airshow_p1280x720_422p_10bit.yuv @ 30 frames per second	3473	3480
	Airshow_p1920x1080_422p_10bit.yuv @ 30 frames per second	7854	7886
	Fruits_i1920x1080_422p_10bit.yuv, @ 60 fields per second	8337	8374
AVCIU_ENC_004	Airshow_p1280x720_422p_10bit.yuv @ 30 frames per second	535	538
	Airshow_p1920x1080_422p_10bit.yuv @ 30 frames per second	1140	1148
	Fruits_i1920x1080_422p_10bit.yuv, @ 60 fields per second	1534	1545
AVCIU_ENC_005	Airshow_p1920x1080_444p_12bit.yuv @ 30 frames per second	10446	10767
	Fruits_i1920x1080_444p_12bit.yuv @ 60 fields per second	11221	11433
AVCIU_ENC_006	Airshow_p1920x1080_444p_12bit.yuv @ 30 frames per second	1512	1543
	Fruits_i1920x1080_444p_12bit.yuv @ 60 fields per second	2035	2080

(1) Measured with C66x DSP 1250MHz clock, DDR2 1333MHZ clock, Program memory in SL2 memory, I/O buffers in external memory and stack in internal L2 memory with cache configurations: 32KB L1P Program cache, 32KB L1D Data cache and 64KB L2 cache. There could be a variation of approximately 1-2% in the values.

(2) First 30frames have been considered for calculating the average and peak cycle consumption by the encoder library for each of the listed input files.

(3) Performance is measured across the process call after all cores reach same sync point.

**Table 3 Memory Statistics of TMS320C6678 with Code Generation Tools Version 7.3.5**

CONFIGURATION ID	MEMORY STATISTICS <sup>(1)(2)</sup>					
	PROGRAM MEMORY <sup>(4)</sup>	DATA MEMORY <sup>(3) (5)</sup>				TOTAL
		PERSISTENT	CONSTANT	SHARED	SCRATCH	
AVCIU_ENC_001 AVCIU_ENC_003 AVCIU_ENC_005	719	368	20	17360	5209	23676
AVCIU_ENC_002 AVCIU_ENC_004 AVCIU_ENC_006	719	2821	20	17360	41665	62585

- (1) All these memory requirements are for AVC Intra & Ultra encoder library only. They do not include any memory requirements from test application side. Stack, heap and code requirements for test-application are extra.
- (2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).
- (3) The memory requirements given in Table 3 are calculated for 1920x1080 resolution and YUV 422 chroma sub sampling.
- (4) Program code is stored in SL2 memory.
- (5) Typical input and output buffers for 1920x1080 resolutions with yuv planer 4:2:2 formats are as follows.  
Input Buffer: 8160KB

**Output Buffer: 5120KB Table 4 Internal Data Memory Split-up**

CONFIGURATION ID	DATA MEMORY – INTERNAL <sup>(1) (2)</sup>					
	LOCAL L2				SHARED L2	TOTAL
	CONSTANTS	PERSISTENT	SCRATCH	STACK		
AVCIU_ENC_001 AVCIU_ENC_002 AVCIU_ENC_003 AVCIU_ENC_004 AVCIU_ENC_005 AVCIU_ENC_006	0	0	256	16	34	306

- (1) Internal memory requirements are for each individual cores.
- (2) All memory requirements are expressed in kilobytes (1K bytes = 1024 bytes).

**Table 5 Cache/SRAM configuration<sup>(1)</sup>**

NAME	AVAILABLE	CACHE	SRAM
L1P (Program Memory)	32KB	32KB	0KB
L1D (Data Memory)	32KB	32KB	0KB
L2	512KB	64KB	256KB

- (1) All above mentioned numbers are for all configurations.

**Table 6 EDMA Configuration** <sup>(1) (5)</sup>

TC Q	TC 0	TC 1	TC 2	TC 3	TOTAL	MAXIMUM <sup>(3)</sup>
Usage	R/W to DDR/L2	R/W to DDR/L2	R/W to DDR/L2	R/W to DDR/L2	-	-
Priority <sup>(2)</sup>	0	1	2	3	-	-
EDMA Channels <sup>(6)</sup>	-	-	-	-	8 <sup>(4)</sup>	18
QDMA Channels	-	-	0	0	0 <sup>(4)</sup>	32
Num PARAMS	-	-	-	-	32 <sup>(4)</sup>	144

- (1) All above mentioned numbers are for all configurations (AVCIU\_ENC\_001, AVCIU\_ENC\_002).  
 (2) Lesser number corresponds to higher TC priority. Default priority is 2. When different TC's have same priority, the arbitration order is TC0 > TC1 > TC2 > TC3.  
 (3) Max corresponds to the maximum number of EDMA/QDMA channels or maximum number of PARAMS available on the chip. It does NOT indicate the maximum number requested by the codec.  
 (4) Same EDMA channel is used to copy data to DDR and to L2 memory at different instances.  
 (5) Above configuration table specifies EDMA hardware usage for each core in multicore scenario.  
 (6) Resource manager decides TC for each EDMA channel while allocating

### Notes

- I/O buffers:
  - Input buffer size = 8160 K-bytes (for 1920x1088 resolution, YUV422)
  - Output buffer size = 5120 K-bytes (for encoding 1920x1088 resolution)
- None of the output buffers are accessed by DSP cores hence the data should be valid in DDR (not in cache).

### References

- SMPTE RP 2027:2011: AVC Intra-Frame coding specification for SSM card applications
- eXpressDSP Algorithm Interoperability Standard (TMS320 Algorithm Interface Standard) AVC Intra & Ultra Encoder on TMS320C6678 Platform User's Guide

### Glossary

Term	Description
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

### Acronyms

Acronym	Description
DMA	Direct Memory Access
SMPTE	Society of Motion Picture and Television Engineers
EVM	Evaluation Module
AVC	Advanced Video Codec
XDAIS	eXpressDSP Algorithm Interface Standard
XDM	eXpressDSP Digital Media

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

TI E2E Community Home Page [e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright 2012, Texas Instruments Incorporated