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May 2014 – Revision 5.0

Mailing Address

Texas Instruments
Training Technical Organization
6500 Chase Oaks Blvd Building 2
M/S 8437
Plano, Texas 75023
The objective of this workshop is to gain a fully understand and a complete working knowledge of the C2000 microcontroller. This will be accomplished through detailed presentations and hands-on lab exercises.

The workshop will start with the basic topics and progress to more advanced topics in a logical flow such that each topic and lab exercise builds on the previous one presented. At the end of the workshop, you should be confident in applying the skills learned in your product design.
# C2000™ Microcontroller Workshop Outline

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<td>8. Numerical Concepts</td>
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<td>11. Viterbi, Complex Math, CRC Unit (VCU)</td>
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<td>12. System Design</td>
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<td>13. Communications</td>
</tr>
<tr>
<td>14. Support Resources</td>
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</tbody>
</table>

## Required Workshop Materials

<table>
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<tr>
<th>Required Workshop Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>♦ F28069 Experimenter’s Kit (<a href="TMDXDOCK28069">TMDXDOCK28069</a>)</td>
</tr>
<tr>
<td>♦ Install Code Composer Studio v6.0.0</td>
</tr>
<tr>
<td>♦ Run the workshop installer</td>
</tr>
</tbody>
</table>
| *C2000 Microcontroller Workshop-5.0-Setup.exe*
| ♦ Lab Files / Solution Files |
| ♦ Student Guide and Documentation |

The materials required for this workshop are available using the links shown at the top of this slide. An F28069 Experimenter’s Kit and a jumper wire will be needed for the lab exercises. The
lab directions are written based on the version of Code Composer Studio as shown on this slide. The workshop installer will automatically install the lab files, solution files, workshop manual, and documentation.

**C2000™ Experimenter Kit**

The development tool for this workshop will be the TMS320F28069 Experimenter’s Kit. The kit consists of a controlCARD and USB Docking Station. It is a self-contained system that plugs into a free USB port on your computer. The USB port provides power, as well as communicates to the onboard JTAG emulation controller. LED LD1 on the Docking Station and LED LD1 on the controlCARD illuminates when the board is powered. LED LD2 on the controlCARD is connected to GPIO34. We will be using this LED as a visual indicator during the lab exercises. The GPIO and ADC lines from the F28069 device are pinned out to the Docking Station headers. We will be using a jumper wire to connect various GPIO and ADC lines on these headers.
When comparing the Delfino and Piccolo product lines, you will notice that the Piccolo F2806x devices share many features with the Delfino product line. The Delfino product line is shown in the table by the F2833x column; therefore, the F28069, being the most feature-rich Piccolo device, was chosen as the platform for this workshop. The knowledge learned from this device will be applicable to all C2000 product lines.

<table>
<thead>
<tr>
<th>Feature</th>
<th>F2833x</th>
<th>F2803x</th>
<th>F2806x</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>150 MHz</td>
<td>60 MHz</td>
<td>90 MHz</td>
</tr>
<tr>
<td>Flash / RAM</td>
<td>128Kw / 34Kw</td>
<td>64Kw / 10Kw</td>
<td>128Kw / 50Kw</td>
</tr>
<tr>
<td>On-chip Oscillators</td>
<td>-</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>VREG / POR / BOR</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Watchdog Timer</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>12-bit ADC</td>
<td>SEQ - based</td>
<td>SOC - based</td>
<td>SOC - based</td>
</tr>
<tr>
<td>Analog COMP w/ DAC</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>FPU</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>6-Channel DMA</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>CLA</td>
<td>-</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>VCU</td>
<td>-</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>ePWM / HR ePWM</td>
<td>✓</td>
<td>✓</td>
<td>✓/✓</td>
</tr>
<tr>
<td>eCAP / HR eCAP</td>
<td>✓</td>
<td>✓</td>
<td>✓/✓</td>
</tr>
<tr>
<td>eQEP</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>SCI / SPI / I2C</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>LIN</td>
<td>-</td>
<td>✓</td>
<td>-</td>
</tr>
<tr>
<td>McBSP</td>
<td>✓</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>USB</td>
<td>-</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>External Interface</td>
<td>✓</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Introduction

This architectural overview introduces the basic architecture of the C2000™ Piccolo™ series of microcontrollers from Texas Instruments. The Piccolo™ series adds a new level of general purpose processing ability unseen in any previous DSP/MCU chips. The C2000™ is ideal for applications combining digital signal processing, microcontroller processing, efficient C code execution, and operating system tasks.

Unless otherwise noted, the terms C28x, F28x and F2806x refer to TMS320F2806x devices throughout the remainder of these notes. For specific details and differences please refer to the device data sheet and user’s guide.

Module Objectives

When this module is complete, you should have a basic understanding of the F28x architecture and how all of its components work together to create a high-end, uniprocessor control system.

- Review the F28x block diagram and device features
- Describe the F28x bus structure and memory map
- Identify the various memory blocks on the F28x
- Identify the peripherals available on the F28x
Module Topics

Architecture Overview

Module Topics

What is the TMS320C2000™?

TMS320C2000™ Internal Bussing

F28x CPU + FPU + VCU and CLA

Special Instructions

Pipeline Advantage

F28x CPU + FPU + VCU Pipeline

Memory

Memory Map

Code Security Module (CSM)

Peripherals

Fast Interrupt Response

Summary
What is the TMS320C2000™?

The TMS320C2000™ is a 32-bit fixed point microcontroller that specializes in high performance control applications such as, robotics, industrial automation, mass storage devices, lighting, optical networking, power supplies, and other control applications needing a single processor to solve a high performance application.

This block diagram represents an overview of all device features and is not specific to any one device. The F28069 device is designed around a multibus architecture, also known as a modified Harvard architecture. This can be seen in the block diagram by the separate program bus and data bus, along with the link between the two buses. This type of architecture greatly enhances the performance of the device.

In the upper left area of the block diagram, you will find the memory section, which consists of the boot ROM, sectored flash, and RAM. Also, you will notice that the six-channel DMA has its own set of buses.

In the lower left area of the block diagram, you will find the execution section, which consists of a 32-bit by 32-bit hardware multiplier, a read-modify-write atomic ALU, a floating-point unit, and a Viterbi complex math CRC unit. The control law accelerator coprocessor is an independent and separate unit that has its own set of buses.

The peripherals are grouped on the right side of the block diagram. The upper set is the control peripherals, which consists of the ePWM, eCAP, eQEP, and ADC. The lower set is the communication peripherals and consists of the multichannel buffered serial port, I2C, SCI, SPI, CAN, and USB.

The PIE block, or Peripheral Interrupt Expansion block, manages the interrupts from the peripherals. In the bottom right corner is the general-purpose I/O. Also, the CPU has a watchdog module and three 32-bit general-purpose timers available.
TMS320C2000™ Internal Bussing

As with many DSP-type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The F28x memory bus architecture contains:

- A program read bus (22-bit address line and 32-bit data line)
- A data read bus (32-bit address line and 32-bit data line)
- A data write bus (32-bit address line and 32-bit data line)

The 32-bit-wide data busses provide single cycle 32-bit operations. This multiple bus architecture, known as a Harvard Bus Architecture, enables the F28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories are attached to the memory bus and will prioritize memory accesses.
F28x CPU + FPU + VCU and CLA

The F28x is a highly integrated, high performance solution for demanding control applications. The F28x is a cross between a general purpose microcontroller and a digital signal processor, balancing the code density of a RISC processor and the execution speed of a DSP with the architecture, firmware, and development tools of a microcontroller.

The DSP features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and a modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation.

The F28x design supports an efficient C engine with hardware that allows the C compiler to generate compact code. Multiple busses and an internal register bus allow an efficient and flexible way to operate on the data. The architecture is also supported by powerful addressing modes, which allow the compiler as well as the assembly programmer to generate compact code that is almost one to one corresponded to the C code.

The F28x is as efficient in DSP math tasks as it is in system control tasks. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the F28x and its 64-bit processing capabilities, enable the F28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive solution. Along with this is the capability to perform two 16 x 16-bit multiply accumulate instructions simultaneously or Dual MACs (DMAC). Also, some devices feature a floating-point unit.

The, F28x is source code compatible with the 24x/240x devices and previously written code can be reassembled to run on a F28x device, allowing for migration of existing code onto the F28x.
Special Instructions

F28x Atomic Read/Modify/Write

Atomic Instructions Benefits
- Simpler programming
- Smaller, faster code
- Uninterruptible (Atomic)
- More efficient compiler

Atomics are small common instructions that are non-interuptable. The atomic ALU capability supports instructions and code that manages tasks and processes. These instructions usually execute several cycles faster than traditional coding.
Pipeline Advantage

The F28x uses a special 8-stage protected pipeline to maximize the throughput. This protected pipeline prevents a write to and a read from the same location from occurring out of order.

This pipelining also enables the F28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.
Floating-point and VCU operations are not pipeline protected. Some instructions require delay slots for the operation to complete. This can be accomplished by insert NOPs or other non-conflicting instructions between operations.

In the user’s guide, instructions requiring delay slots have a ‘p’ after their cycle count. The 2p stands for 2 pipelined cycles. A new instruction can be started on each cycle. The result is valid only 2 instructions later.

Three general guidelines for the FPU/VCU pipeline are:

<table>
<thead>
<tr>
<th>Math</th>
<th>Conversion</th>
<th>Everything else*</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPYF32, ADDF32, SUBF32, MACF32, VCMYP</td>
<td>I16TOF32, F32TOI16, F32TOI16R, etc…</td>
<td>Load, Store, Compare, Min, Max, Absolute and Negative value</td>
</tr>
<tr>
<td>2p cycles</td>
<td>2p cycles</td>
<td>Single cycle</td>
</tr>
<tr>
<td>One delay slot</td>
<td>One delay slot</td>
<td>No delay slot</td>
</tr>
</tbody>
</table>

* Note: MOV32 between FPU and CPU registers is a special case.
Memory

The memory space on the F28x is divided into program memory and data memory. There are several different types of memory available that can be used as both program memory and data memory. They include the flash memory, single access RAM (SARAM), OTP, and Boot ROM which is factory programmed with boot software routines and standard tables used in math related algorithms.

Memory Map

The F28x CPU contains no memory, but can access memory on chip. The F28x uses 32-bit data addresses and 22-bit program addresses. This allows for a total address reach of 4G words (1 word = 16-bits) in data memory and 4M words in program memory. Memory blocks on all F28x designs are uniformly mapped to both program and data space.

This memory map shows the different blocks of memory available to the program and data space.

The F28069 utilizes a contiguous memory map, also known as a von-Neumann architecture. This type of memory map lends itself well to higher-level languages. This can be seen by the labels located at the top of the memory map where the memory blocks extend between both the data space and program space.

At the top of the map, we have two blocks of RAM called M0 and M1. Then we see PF0 through PF3, which are the peripheral frames. This is the area where you will find the peripheral registers. Also in this space, you will find the PIE block. Memory blocks L0 through L8 are grouped together. L0 through L3 are accessible by the CPU and CLA. L5 through L8 are accessible by the DMA.
The user OTP is a one-time, programmable, memory block. TI reserves a small space in the map for the ADC and oscillator calibration data. The flash block contains a section for passwords, which are used by the code security module. The boot ROM and boot ROM vectors are located at the bottom of the memory map.

**Code Security Module (CSM)**

- Prevents reverse engineering and protects valuable intellectual property
- 128-bit user defined password is stored in Flash
- 128-bits = \(2^{128} = 3.4 \times 10^{38}\) possible passwords
- To try 1 password every 8 cycles at 80 MHz, it would take at least \(1.1 \times 10^{24}\) years to try all possible combinations!

---

**Peripherals**

The F28x comes with many built in peripherals optimized to support control applications. These peripherals vary depending on which F28x device you choose.

- ePWM
- eCAP
- eQEP
- Analog-to-Digital Converter
- Watchdog Timer
- CLA
- DMA
- SPI
- SCI
- I2C
- McBSP
- eCAN
- USB
- GPIO
The fast interrupt response, with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. F28x implements a zero cycle penalty to do 14 registers context saved and restored during an interrupt. This feature helps reduces the interrupt service routine overheads.

The C2000 devices feature a very fast interrupt response manager using the PIE block. This allows up to 96 possible interrupt vectors to be processed by the CPU. More details about this will be covered in the reset, interrupts, and system initialization modules.
<table>
<thead>
<tr>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>- High performance 32-bit CPU</td>
</tr>
<tr>
<td>- 32x32 bit or dual 16x16 bit MAC</td>
</tr>
<tr>
<td>- IEEE single-precision floating point unit (FPU)</td>
</tr>
<tr>
<td>- Hardware Control Law Accelerator (CLA)</td>
</tr>
<tr>
<td>- Viterbi, complex math, CRC unit (VCU)</td>
</tr>
<tr>
<td>- Atomic read-modify-write instructions</td>
</tr>
<tr>
<td>- Fast interrupt response manager</td>
</tr>
<tr>
<td>- 128Kw on-chip flash memory</td>
</tr>
<tr>
<td>- Code security module (CSM)</td>
</tr>
<tr>
<td>- Control peripherals</td>
</tr>
<tr>
<td>- 12-bit ADC module</td>
</tr>
<tr>
<td>- Comparators</td>
</tr>
<tr>
<td>- Direct memory access (DMA)</td>
</tr>
<tr>
<td>- Up to 54 shared GPIO pins</td>
</tr>
<tr>
<td>- Communications peripherals</td>
</tr>
</tbody>
</table>
Programming Development Environment

Introduction

This module will explain how to use Code Composer Studio (CCS) integrated development environment (IDE) tools to develop a program. Creating projects and setting building options will be covered. Use and the purpose of the linker command file will be described.

Module Objectives

- Use Code Composer Studio to:
  - Create a Project
  - Set Build Options
- Create a user linker command file which:
  - Describes a system’s available memory
  - Indicates where sections will be placed in memory
Module Topics

Programming Development Environment ................................................................. 2-1

Module Topics ............................................................................................................. 2-2

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  Software Development and COFF Concepts .......................................................... 2-3
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Software Development and COFF Concepts

In an effort to standardize the software development process, TI uses the Common Object File Format (COFF). COFF has several features which make it a powerful software development system. It is most useful when the development task is split between several programmers.

Each file of code, called a module, may be written independently, including the specification of all resources necessary for the proper operation of the module. Modules can be written using Code Composer Studio (CCS) or any text editor capable of providing a simple ASCII file output. The expected extension of a source file is .ASM for assembly and .C for C programs.

Code Composer Studio

Code Composer Studio includes:
- Integrated Edit/Debug GUI
- Code Generation Tools
- TI-RTOS

Code Composer Studio includes a built-in editor, compiler, assembler, linker, and an automatic build process. Additionally, tools to connect file input and output, as well as built-in graph displays for output are available. Other features can be added using the plug-ins capability.

Numerous modules are joined to form a complete program by using the linker. The linker efficiently allocates the resources available on the device to each module in the system. The linker uses a command (.CMD) file to identify the memory resources and placement of where the various sections within each module are to go. Outputs of the linking process includes the linked object file (.OUT), which runs on the device, and can include a .MAP file which identifies where each linked section is located.

The high level of modularity and portability resulting from this system simplifies the processes of verification, debug and maintenance. The process of COFF development is presented in greater detail in the following paragraphs.
The concept of COFF tools is to allow modular development of software independent of hardware concerns. An individual assembly language file is written to perform a single task and may be linked with several other tasks to achieve a more complex total system.

Writing code in modular form permits code to be developed by several people working in parallel so the development cycle is shortened. Debugging and upgrading code is faster, since components of the system, rather than the entire system, is being operated upon. Also, new systems may be developed more rapidly if previously developed modules can be used in them.

Code developed independently of hardware concerns increases the benefits of modularity by allowing the programmer to focus on the code and not waste time managing memory and moving code as other code components grow or shrink. A linker is invoked to allocate systems hardware to the modules desired to build a system. Changes in any or all modules, when re-linked, create a new hardware allocation, avoiding the possibility of memory resource conflicts.

**Code Composer Studio**

**Code Composer Studio: IDE**

- Integrates: edit, code generation, and debug
- Single-click access using buttons
- Powerful graphing/profiling tools
- Automated tasks using Scripts
- Built-in access to BIOS functions
- Based on the Eclipse open source software framework

Code Composer Studio™ (CCS) is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCS comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before and add functionality to their application thanks to sophisticated productivity tools.

CCS is based on the Eclipse open source software framework. The Eclipse software framework was originally developed as an open framework for creating development tools. Eclipse offers an excellent software framework for building software development environments and it is
becoming a standard framework used by many embedded software vendors. CCS combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. CCS supports running on both Windows and Linux PCs. Note that not all features or devices are supported on Linux.

Edit and Debug Perspective (CCSv6)

A perspective defines the initial layout views of the workbench windows, toolbars, and menus that are appropriate for a specific type of task, such as code development or debugging. This minimizes clutter to the user interface.

Code Composer Studio has “Edit” and “Debug” perspectives. Each perspective provides a set of functionality aimed at accomplishing a specific task. In the edit perspective, views used during code development are displayed. In the debug perspective, views used during debug are displayed.
Target Configuration

A Target Configuration tells CCS how to connect to the device. It describes the device using GEL files and device configuration files. The configuration files are XML files and have a *.ccxl file extension.

Creating a Target Configuration

- File → New → Target Configuration File
- Select connection type
- Select device
- Save configuration
CCSv6 Project

Code Composer works with a *project* paradigm. Essentially, within CCS you create a project for each executable program you wish to create. Projects store all the information required to build the executable. For example, it lists things like: the source files, the header files, the target system’s memory-map, and program build options.

- **List of files:**
  - Source (C, assembly)
  - Libraries
  - DSP/BIOS configuration file
  - Linker command files

- **Project settings:**
  - Build options (compiler, assembler, linker, and TI-RTOS)
  - Build configurations

A project contains files, such as C and assembly source files, libraries, BIOS configuration files, and linker command files. It also contains project settings, such as build options, which include the compiler, assembler, linker, and BIOS, as well as build configurations.

To create a new project, you need to select the following menu items:

**File → New → CCS Project**

Along with the main Project menu, you can also manage open projects using the right-click popup menu. Either of these menus allows you to modify a project, such as add files to a project, or open the properties of a project to set the build options.
Creating a New CCSv6 Project

A graphical user interface (GUI) is used to assist in creating a new project. The GUI is shown in the slide below.

After a project is created, the build options are configured.
CCSv6 Build Options – Compiler / Linker

Project options direct the code generation tools (i.e. compiler, assembler, linker) to create code according to your system’s needs. When you create a new project, CCS creates two sets of build options – called Configurations: one called Debug, the other Release (you might think of as Optimize).

To make it easier to choose build options, CCS provides a graphical user interface (GUI) for the various compiler and linker options. Here’s a sample of the configuration options.

There is a one-to-one relationship between the items in the text box on the main page and the GUI check and drop-down box selections. Once you have mastered the various options, you can probably find yourself just typing in the options.

There are many linker options but these four handle all of the basic needs.

- `-o <filename>` specifies the output (executable) filename.
- `-m <filename>` creates a map file. This file reports the linker’s results.
- `-c` tells the compiler to autoinitialize your global and static variables.
- `-x` tells the compiler to exhaustively read the libraries. Without this option libraries are searched only once, and therefore backwards references may not be resolved.

To help make sense of the many compiler options, TI provides two default sets of options (configurations) in each new project you create. The Release (optimized) configuration invokes the optimizer with –o3 and disables source-level, symbolic debugging by omitting –g (which disables some optimizations to enable debug).
CCSv6 Debug Environment

The basic buttons that control the debug environment are located in the top of CCS:

![Image of CCSv6 Debug Environment buttons]

The common debugging and program execution descriptions are shown below:

**Start debugging**

<table>
<thead>
<tr>
<th>Image</th>
<th>Name</th>
<th>Description</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="new_target_configuration.png" alt="Image" /></td>
<td>New Target Configuration</td>
<td>Creates a new target configuration file.</td>
<td>File New Menu Target Menu</td>
</tr>
<tr>
<td><img src="debug.png" alt="Image" /></td>
<td>Debug</td>
<td>Opens a dialog to modify existing debug configurations. Its drop down can be used to access other launching options.</td>
<td>Debug Toolbar Target Menu</td>
</tr>
<tr>
<td><img src="connect_target.png" alt="Image" /></td>
<td>Connect Target</td>
<td>Connect to hardware targets.</td>
<td>TI Debug Toolbar Target Menu Debug View Context Menu</td>
</tr>
<tr>
<td><img src="terminate_all.png" alt="Image" /></td>
<td>Terminate All</td>
<td>Terminates all active debug sessions.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
</tbody>
</table>
Program execution

<table>
<thead>
<tr>
<th>Image</th>
<th>Name</th>
<th>Description</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Image" /></td>
<td>Halt</td>
<td>Halts the selected target. The rest of the debug views will update automatically with most recent target data.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image2" alt="Image" /></td>
<td>Run</td>
<td>Resumes the execution of the currently loaded program from the current PC location. Execution continues until a breakpoint is encountered.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image3" alt="Image" /></td>
<td>Run to Line</td>
<td>Resumes the execution of the currently loaded program from the current PC location. Execution continues until the specific source/assembly line is reached.</td>
<td>Target Menu Disassembly Context Menu Source Editor Context Menu</td>
</tr>
<tr>
<td><img src="image4" alt="Image" /></td>
<td>Go to Main</td>
<td>Runs the program until the beginning of the function main is reached.</td>
<td>Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image5" alt="Image" /></td>
<td>Step Into</td>
<td>Steps into the highlighted statement.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image6" alt="Image" /></td>
<td>Step Over</td>
<td>Steps over the highlighted statement. Execution will continue at the next line either in the same method or (if you are at the end of a method) it will continue in the method from which the current method was called. The cursor jumps to the declaration of the method and selects this line.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image7" alt="Image" /></td>
<td>Step Return</td>
<td>Steps out of the current method.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image8" alt="Image" /></td>
<td>Reset</td>
<td>Resets the selected target. The drop-down menu has various advanced reset options, depending on the selected device.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image9" alt="Image" /></td>
<td>Restart</td>
<td>Restores the PC to the entry point for the currently loaded program. If the debugger option &quot;Run to main on target load or restart&quot; is set the target will run to the specified symbol, otherwise the execution state of the target is not changed.</td>
<td>Target Menu Debug View Toolbar</td>
</tr>
<tr>
<td><img src="image10" alt="Image" /></td>
<td>Assembly Step Into</td>
<td>The debugger executes the next assembly instruction, whether source is available or not.</td>
<td>TI Explicit Stepping Toolbar Target Advanced Menu</td>
</tr>
<tr>
<td><img src="image11" alt="Image" /></td>
<td>Assembly Step Over</td>
<td>The debugger steps over a single assembly instruction. If the instruction is an assembly subroutine, the debugger executes the assembly subroutine and then halts after the assembly function returns.</td>
<td>TI Explicit Stepping Toolbar Target Advanced Menu</td>
</tr>
</tbody>
</table>
Creating a Linker Command File

Sections

Looking at a C program, you'll notice it contains both code and different kinds of data (global, local, etc.). All code consists of different parts called sections. All default section names begin with a dot and are typically lower case. The compiler has default section names for initialized and uninitialized sections. For example, x and y are global variables, and they are placed in the section .ebss. Whereas 2 and 7 are initialized values, and they are placed in the section called .cinit. The local variables are in a section .stack, and the code is placed in a section called .text.

In the TI code-generation tools (as with any toolset based on the COFF – Common Object File Format), these various parts of a program are called Sections. Breaking the program code and data into various sections provides flexibility since it allows you to place code sections in ROM and variables in RAM. The preceding diagram illustrated four sections:

- Global Variables
- Initial Values for global variables
- Local Variables (i.e. the stack)
- Code (the actual instructions)
Following is a list of the sections that are created by the compiler. Along with their description, we provide the Section Name defined by the compiler. This is a small list of compiler default section names. The top group is initialized sections, and they are linked to flash. In our previous code example, we saw .text was used for code, and .cinit for initialized values. The bottom group is uninitialized sections, and they are linked to RAM. Once again, in our previous example, we saw .ebss used for global variables and .stack for local variables.

### Compiler Section Names

<table>
<thead>
<tr>
<th>Initialized Sections</th>
<th>Description</th>
<th>Link Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>.text</td>
<td>code</td>
<td>FLASH</td>
</tr>
<tr>
<td>.cinit</td>
<td>initialization values for global and static variables</td>
<td>FLASH</td>
</tr>
<tr>
<td>.econst</td>
<td>constants (e.g. const int k = 3;)</td>
<td>FLASH</td>
</tr>
<tr>
<td>.switch</td>
<td>tables for switch statements</td>
<td>FLASH</td>
</tr>
<tr>
<td>.pinit</td>
<td>tables for global constructors (C++)</td>
<td>FLASH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Uninitialized Sections</th>
<th>Description</th>
<th>Link Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>.ebss</td>
<td>global and static variables</td>
<td>RAM</td>
</tr>
<tr>
<td>.stack</td>
<td>stack space</td>
<td>low 64Kw RAM</td>
</tr>
<tr>
<td>.esysmem</td>
<td>memory for far malloc functions</td>
<td>RAM</td>
</tr>
</tbody>
</table>

Note: During development initialized sections could be linked to RAM since the emulator can be used to load the RAM.

Sections of a C program must be located in different memories in your target system. This is the big advantage of creating the separate sections for code, constants, and variables. In this way, they can all be linked (located) into their proper memory locations in your target embedded system. Generally, they're located as follows:

**Program Code (.text)**

Program code consists of the sequence of instructions used to manipulate data, initialize system settings, etc. Program code must be defined upon system reset (power turn-on). Due to this basic system constraint it is usually necessary to place program code into non-volatile memory, such as FLASH or EPROM.

**Constants (.cinit – initialized data)**

Initialized data are those data memory locations defined at reset. It contains constants or initial values for variables. Similar to program code, constant data is expected to be valid upon reset of the system. It is often found in FLASH or EPROM (non-volatile memory).

**Variables (.ebss – uninitialized data)**

Uninitialized data memory locations can be changed and manipulated by the program code during runtime execution. Unlike program code or constants, uninitialized data or variables must reside
in volatile memory, such as RAM. These memories can be modified and updated, supporting the way variables are used in math formulas, high-level languages, etc. Each variable must be declared with a directive to reserve memory to contain its value. By their nature, no value is assigned, instead they are loaded at runtime by the program.

Next, we need to place the sections that were created by the compiler into the appropriate memory spaces. The uninitialized sections, .ebss and .stack, need to be placed into RAM; while the initialized sections, .cinit, and .txt, need to be placed into flash.

![Placing Sections in Memory](image)

Linking code is a three step process:

1. Defining the various regions of memory (on-chip SARAM vs. FLASH vs. External Memory).
2. Describing what sections go into which memory regions
3. Running the linker with “build” or “rebuild”
Linker Command Files (.cmd)

The linker concatenates each section from all input files, allocating memory to each section based on its length and location as specified by the MEMORY and SECTIONS commands in the linker command file. The linker command file describes the physical hardware memory and specifies where the sections are placed in the memory. The file created during the link process is a .out file. This is the file that will be loaded into the microcontroller. As an option, we can generate a map file. This map file will provide a summary of the link process, such as the absolute address and size of each section.

Memory-Map Description

The MEMORY section describes the memory configuration of the target system to the linker. The format is:  

```
Name:  origin = 0x????,  length = 0x????
```

For example, if you placed a 64Kw FLASH starting at memory location 0x3E8000, it would read:

```
MEMORY
{
  FLASH:  origin = 0x3E8000 , length = 0x010000
}
```

Each memory segment is defined using the above format. If you added M0SARAM and M1SARAM, it would look like:
Remember that the MCU has two memory maps: *Program*, and *Data*. Therefore, the MEMORY description must describe each of these separately. The loader uses the following syntax to delineate each of these:

<table>
<thead>
<tr>
<th>Linker Page</th>
<th>TI Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Page 0</td>
<td>Program</td>
</tr>
<tr>
<td>Page 1</td>
<td>Data</td>
</tr>
</tbody>
</table>

### Linker Command File

```plaintext
MEMORY
{
  PAGE 0:     /* Program Memory */
  FLASH:   origin = 0x3E8000, length = 0x10000

  PAGE 1:     /* Data Memory */
  MOSARAM: origin = 0x000000, length = 0x400
  M1SARAM: origin = 0x000400, length = 0x400
}
SECTIONS
{
  .text:>     FLASH     PAGE = 0
  .ebss:>     MOSARAM  PAGE = 1
  .cinit:>    FLASH     PAGE = 0
  .stack:>    M1SARAM   PAGE = 1
}
```

A linker command file consists of two sections, a memory section and a sections section. In the memory section, page 0 defines the program memory space, and page 1 defines the data memory space. Each memory block is given a unique name, along with its origin and length. In the sections section, the section is directed to the appropriate memory block.

### Section Placement

The SECTIONS section will specify how you want the sections to be distributed through memory. The following code is used to link the sections into the memory specified in the previous example:
The linker will gather all the code sections from all the files being linked together. Similarly, it will combine all ‘like’ sections.

Beginning with the first section listed, the linker will place it into the specified memory segment.

**Summary: Linker Command File**

The linker command file (.cmd) contains the inputs — commands — for the linker. This information is summarized below:

<table>
<thead>
<tr>
<th>Memory Map Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
</tr>
<tr>
<td>Location</td>
</tr>
<tr>
<td>Size</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Sections Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Directs software sections into named memory regions</td>
</tr>
<tr>
<td>Allows per-file discrimination</td>
</tr>
<tr>
<td>Allows separate load/run locations</td>
</tr>
</tbody>
</table>
Lab File Directory Structure

Lab File Directory Structure

Supporting Files and Libraries
- Easier to make projects portable
- `${PROJECT_ROOT}` provides an anchor point for paths to files that travel with the project
- Easier to maintain and update supporting files and libraries

Original Source Files
Source Files are “Added” to the Project Folder
- All modified files are in the Project Folder
- Original source files are always available for reuse, if a file becomes corrupted

Note: CCSv6 will automatically add ALL files contained in the folder where the project is created
Lab 2: Linker Command File

Objective

Use a linker command file to link the C program file (Lab2.c) into the system described below.

Placement of Sections:
- `.text` into RAM Block L4SARAM on PAGE 0 (program memory)
- `.cinit` into RAM Block L4SARAM on PAGE 0 (program memory)
- `.ebss` into RAM Block M0SARAM on PAGE 1 (data memory)
- `.stack` into RAM Block M1SARAM on PAGE 1 (data memory)

Lab 2: Linker Command File

System Description:
- TMS320F28069
- All internal RAM blocks allocated

- Start Code Composer Studio (CCS) by double clicking the icon on the desktop or selecting it from the Windows Start menu. When CCS loads, a dialog box will prompt you for the location of a workspace folder. Use the default location for the workspace and click OK.

- Code Composer Studio must be installed in addition to the workshop files. A local copy of the required controlSUITE files is included with the lab files. This provides portability, making the workshop files self-contained and independent of other support files or resources. The lab directions for this workshop are based on all software installed in their default locations.

- Insert the F28069 controlCARD into the Docking Station connector slot. Using the supplied USB cable – plug the USB Standard Type A connector into the computer USB port and the USB Standard Type B connector into the Docking Station. On the Docking Station move switch SW1 to the “USB” position. This will power the Docking Station and controlCARD using the power supplied by the computer USB port. Additionally, this USB port will provide the JTAG communication link between the device and Code Composer Studio.

Initial Hardware Set Up

Initial Software Set Up

Procedure

Start Code Composer Studio and Open a Workspace

1. Insert the F28069 controlCARD into the Docking Station connector slot. Using the supplied USB cable – plug the USB Standard Type A connector into the computer USB port and the USB Standard Type B connector into the Docking Station. On the Docking Station move switch SW1 to the “USB” position. This will power the Docking Station and controlCARD using the power supplied by the computer USB port. Additionally, this USB port will provide the JTAG communication link between the device and Code Composer Studio.

2. Code Composer Studio must be installed in addition to the workshop files. A local copy of the required controlSUITE files is included with the lab files. This provides portability, making the workshop files self-contained and independent of other support files or resources. The lab directions for this workshop are based on all software installed in their default locations.

3. Procedure

Start Code Composer Studio and Open a Workspace

1. Start Code Composer Studio (CCS) by double clicking the icon on the desktop or selecting it from the Windows Start menu. When CCS loads, a dialog box will prompt you for the location of a workspace folder. Use the default location for the workspace and click OK.
This folder contains all CCS custom settings, which includes project settings and views when CCS is closed so that the same projects and settings will be available when CCS is opened again. The workspace is saved automatically when CCS is closed.

2. The first time CCS opens an introduction page appears. Close the page by clicking the X on the “Getting Started” tab. You should now have an empty workbench. The term workbench refers to the desktop development environment. Maximize CCS to fill your screen.

The workbench will open in the “CCS Edit Perspective” view. Notice the CCS Edit icon in the upper right-hand corner. A perspective defines the initial layout views of the workbench windows, toolbars, and menus which are appropriate for a specific type of task (i.e. code development or debugging). This minimizes clutter to the user interface. The “CCS Edit Perspective” is used to create or build projects. A “CCS Debug Perspective” view will automatically be enabled when the debug session is started. This perspective is used for debugging projects.

**Setup Target Configuration**

3. Open the emulator target configuration dialog box. On the menu bar click:

File → New → Target Configuration File

In the file name field type `F28069_ExpKit.ccxml`. This is just a descriptive name since multiple target configuration files can be created. Leave the “Use shared location” box checked and select Finish.

4. In the next window that appears, select the emulator using the “Connection” pull-down list and choose “Texas Instruments XDS100v1 USB Emulator”. In the “Board or Device” box type `F28069` to filter the options. In the box below, check the box to select “Experimenter’s Kit – Piccolo F28069”. Click Save to save the configuration, then close the “F28069_ExpKit.ccxml” setup window by clicking the X on the tabs.

5. To view the target configurations, click:

View → Target Configurations

and click the plus sign (+) to the left of User Defined. Notice that the `F28069_ExpKit.ccxml` file is listed and set as the default. If it is not set as the default, right-click on the .ccxml file and select “Set as Default”. Close the Target Configurations window by clicking the X on the tab.

**Create a New Project**

6. A project contains all the files you will need to develop an executable output file (.out) which can be run on the MCU hardware. To create a new project click:

File → New → CCS Project

A CCS Project window will open. At the top of this window, filter the “Target” options by using the pull-down list on the left and choose “2806x Piccolo”. In the pull-
down list immediately to the right, choose the “Experimenter’s Kit – F28069 Piccolo”.

Leave the “Connection” box blank. We have already set up the target configuration.

7. The next section selects the project settings. In the Project name field type Lab2. Uncheck the “Use default location” box. Click the Browse… button and navigate to:

   C:\C28x\Labs\Lab2\Project

   Click OK.

8. Next, open the “Advanced setting” section and set the “Linker command file” to “<none>”. We will be using our own linker command file rather than the one supplied by CCS. Leave the “Runtime Support Library” set to “<automatic>”. This will automatically select the “rts2800_fpu32.lib” runtime support library for floating-point devices.

9. Then, open the “Project templates and examples” section and select the “Empty Project” template. Click Finish.

10. A new project has now been created. Notice the Project Explorer window contains Lab2. The project is set Active and the output files will be located in the Debug folder. At this point, the project does not include any source files. The next step is to add the source files to the project.

11. To add the source files to the project, right-click on Lab2 in the Project Explorer window and select:

   Add Files…

   or click: Project  Add Files…

   and make sure you’re looking in C:\C28x\Labs\Lab2\Files. With the “files of type” set to view all files (*.*) select Lab2.c and Lab2.cmd then click OPEN. A “File Operation” window will open, choose “Copy files” and click OK. This will add the files to the project.

12. In the Project Explorer window, click the plus sign (+) to the left of Lab2 and notice that the files are listed.

**Project Build Options**

13. There are numerous build options in the project. Most default option settings are sufficient for getting started. We will inspect a couple of the default options at this time. Right-click on Lab2 in the Project Explorer window and select Properties or click:

   Project  Properties

14. A “Properties” window will open and in the section on the left under “Build” be sure that the “C2000 Compiler” and “C2000 Linker” options are visible. Next, under “C2000 Linker” select the “Basic Options”. Notice that .out and .map files are being specified. The .out file is the executable code that will be loaded into the MCU. The .map file will contain a linker report showing memory usage and section addresses in memory. Also notice the stack size is set to 0x300.
15. Under “C2000 Compiler” select the “Processor Options”. Notice the “Use large memory model” and “Unified memory” boxes are checked. Next, notice the “Specify CLA support” is set to `cla0`, the “Specify floating point support” is set to `fpu32`, and the “Specify VCU support” is set to `vcu0`. Select `OK` to close the Properties window.

**Linker Command File – Lab2.cmd**

16. Open and inspect `Lab2.cmd` by double clicking on the filename in the Project Explorer window. Notice that the `Memory{}` declaration describes the system memory shown on the “Lab2: Linker Command File” slide in the objective section of this lab exercise. Memory blocks `L3DPSARAM` and `L4SARAM` have been placed in program memory on page 0, and the other memory blocks have been placed in data memory on page 1.

17. In the `Sections{}` area notice that the sections defined on the slide have been “linked” into the appropriate memories. Also, notice that a section called `.reset` has been allocated. The `.reset` section is part of the `rts2800_fpu32.lib` and is not needed. By putting the `TYPE = DSECT` modifier after its allocation the linker will ignore this section and not allocate it. Close the inspected file.

**Build and Load the Project**

18. Two buttons on the horizontal toolbar control code generation. Hover your mouse over each button as you read the following descriptions:

<table>
<thead>
<tr>
<th>Button</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Build</td>
<td>Full build and link of all source files</td>
</tr>
<tr>
<td>2</td>
<td>Debug</td>
<td>Automatically build, link, load and launch debug-session</td>
</tr>
</tbody>
</table>

19. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window (we have deliberately put an error in `Lab2.c`). When you get an error, you will see the error message in the Problems window. Expand the error by clicking on the plus sign (+) to the left of the “Errors”. Then simply double-click the error message. The editor will automatically open to the source file containing the error, with the code line highlighted with a question mark (?).

20. Fix the error by adding a semicolon at the end of the “z = x + y” statement. For future knowledge, realize that a single code error can sometimes generate multiple error messages at build time. This was not the case here.

21. Build the project again. There should be no errors this time.

22. CCS can automatically save modified source files, build the program, open the debug perspective view, connect and download it to the target, and then run the program to the beginning of the main function.

Click on the “Debug” button (green bug) or click `RUN` → `Debug`

Notice the CCS Debug icon in the upper right-hand corner indicating that we are now in the “CCS Debug Perspective” view. The program ran through the C-environment initialization routine in the `rts2800_fpu32.lib` and stopped at `main()` in `Lab2.c`. 

---

**Lab 2: Linker Command File**

2 - 22

**C2000 Microcontroller Workshop - Programming Development Environment**
Debug Environment Windows

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in Code Composer Studio. We will examine two of them here: memory browser, and expressions.

23. Open a “Memory Browser” to view the global variable “z”.

   Click: View → Memory Browser on the menu bar.

   Type \&z into the address field, select “Data” memory page, and then select Go. Note that you must use the ampersand (meaning “address of”) when using a symbol in a memory browser address box. Also note that CCS is case sensitive.

   Set the properties format to “Hex 16 Bit – TI Style Hex” in the browser. This will give you more viewable data in the browser. You can change the contents of any address in the memory browser by double-clicking on its value. This is useful during debug.

24. Notice the “Variables” window automatically opened and the local variables x and y are present. The variables window will always contain the local variables for the code function currently being executed.

   (Note that local variables actually live on the stack. You can also view local variables in a memory browser by setting the address to “SP” after the code function has been entered).

25. We can also add global variables to the “Expressions” window if desired. Let's add the global variable “z”.

   Click the “Expressions” tab at the top of the window. In the empty box in the “Expression” column (Add new expression), type z and then enter. An ampersand is not used here. The expressions window knows you are specifying a symbol. (Note that the expressions window can be manually opened by clicking: View → Expressions on the menu bar).

   Check that the expressions window and memory browser both report the same value for “z”. Try changing the value in one window, and notice that the value also changes in the other window.

Single-stepping the Code

26. Click the “Variables” tab at the top of the window to watch the local variables. Single-step through main() by using the <F5> key (or you can use the Step Into button on the horizontal toolbar). Check to see if the program is working as expected. What is the value for “z” when you get to the end of the program?

Terminate Debug Session and Close Project

27. The Terminate button will terminate the active debug session, close the debugger and return CCS to the “CCS Edit Perspective” view.

   Click: Run → Terminate or use the Terminate icon:
28. Next, close the project by right-clicking on Lab2 in the Project Explorer window and select Close Project.

End of Exercise
Introduction

The purpose of the F2806x C-code header files is to simplify the programming of the many peripherals on the F28x device. Typically, to program a peripheral the programmer needs to write the appropriate values to the different fields within a control register. In its simplest form, the process consists of writing a hex value (or masking a bit field) to the correct address in memory. But, since this can be a burdensome and repetitive task, the C-code header files were created to make this a less complicated task.

The F2806x C-code header files are part of a library consisting of C functions, macros, peripheral structures, and variable definitions. Together, this set of files is known as the ‘header files.’

Registers and the bit-fields are represented by structures. C functions and macros are used to initialize or modify the structures (registers).

In this module, you will learn how to use the header files and C programs to facilitate programming the peripherals.

Module Objectives

- Understand the usage of the F2806x C-Code Header Files
- Be able to program peripheral registers
- Understand how the structures are mapped with the linker command file
Module Topics

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Naming Conventions ....................................................................................... 3-7

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Summary ........................................................................................................ 3-14
Traditional and Structure Approach to C Coding

Traditional Approach to C Coding

```c
#define ADCCTL1 (volatile unsigned int *)0x00007100
... 
void main(void)
{
  *ADCCTL1 = 0x1234; //write entire register
  *ADCCTL1 |= 0x4000; //enable ADC module
}
```

Advantages
- Simple, fast and easy to type
- Variable names exactly match register names (easy to remember)

Disadvantages
- Requires individual masks to be generated to manipulate individual bits
- Cannot easily display bit fields in debugger window
- Will generate less efficient code in many cases

In the traditional approach to C coding, we used a #define to assign the address of the register and referenced it with a pointer. The first line of code on this slide we are writing to the entire register with a 16-bit value. The second line, we are ORing a bit field.

Advantages? Simple, fast, and easy to type. The variable names can exactly match the register names, so it's easy to remember. Disadvantages? Requires individual masks to be generated to manipulate individual bits, it cannot easily display bit fields in the debugger window, and it will generate less efficient code in many cases.
### Structure Approach to C Coding

```c
void main(void)
{
    AdcRegs.ADCCTL1.all = 0x1234; //write entire register
    AdcRegs.ADCCTL1.bit.ADCENABLE = 1; //enable ADC module
}
```

<table>
<thead>
<tr>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Easy to manipulate individual bits</td>
<td></td>
</tr>
<tr>
<td>- Watch window is amazing! (next slide)</td>
<td></td>
</tr>
<tr>
<td>- Generates most efficient code (on C28x)</td>
<td></td>
</tr>
<tr>
<td>- Can be difficult to remember the structure names (Editor Auto Complete feature to the rescue!)</td>
<td></td>
</tr>
<tr>
<td>- More to type (again, Editor Auto Complete feature to the rescue)</td>
<td></td>
</tr>
</tbody>
</table>

The structure approach to C coding uses the peripheral register header files. First, a peripheral is specified, followed by a control register. Then you can modify the complete register or selected bits. This is almost self-commented code.

The first line of code on this slide we are writing to the entire register. The second line of code we are modifying a bit field. Advantages? Easy to manipulate individual bits, it works great with our tools, and will generate the most efficient code. Disadvantages? Can be difficult to remember the structure names and more to type; however, the edit auto complete feature of Code Composer Studio will eliminate these disadvantages.
With the traditional approach to coding using #define, we can only view the complete register values. As an example, notice the control register ADCCTL1 has a value of 0x40E4. We would need to refer to the reference guide to know the settings of the individual bit fields.

With the structure approach, we can add the peripheral to an expressions window, allowing us to
view, as well as modify individual bit fields in a register. No need for a reference guide to identify the bit fields.

**Is the Structure Approach Efficient?**

The structure approach enables efficient compiler use of DP addressing mode and C28x atomic operations

<table>
<thead>
<tr>
<th>C Source Code</th>
<th>Generated Assembly Code*</th>
</tr>
</thead>
<tbody>
<tr>
<td>// Stop CPU Timer0</td>
<td>MOV  DP, #0030</td>
</tr>
<tr>
<td>CpuTimer0Regs.TCR.bit.TSS = 1;</td>
<td>OR  @4, #0x0010</td>
</tr>
<tr>
<td>// Load new 32-bit period value</td>
<td>MOV  XAR4, #0x010000</td>
</tr>
<tr>
<td>CpuTimer0Regs.PRD.all = 0x000100000;</td>
<td>MOV  @2, XAR4</td>
</tr>
<tr>
<td>// Start CPU Timer0</td>
<td>AND  @4, #0xFFEF</td>
</tr>
</tbody>
</table>

- Easy to read the code w/o comments
- Bit mask built-in to structure

You could not have coded this example any more efficiently with hand assembly!

* C28x Compiler v5.0.1 with -g and either -o1, -o2, or -o3 optimization level

**Compare with the #define Approach**

The #define approach relies heavily on less-efficient pointers for random memory access, and often does not take advantage of C28x atomic operations

<table>
<thead>
<tr>
<th>C Source Code</th>
<th>Generated Assembly Code*</th>
</tr>
</thead>
<tbody>
<tr>
<td>// Stop CPU Timer0</td>
<td>MOV  @AL,*(0:0x0C04)</td>
</tr>
<tr>
<td>*TIMER0TCR</td>
<td>= 0x0010;</td>
</tr>
<tr>
<td>// Load new 32-bit period value</td>
<td>MOV  *(0:0x0C04), @AL</td>
</tr>
<tr>
<td>*TIMER0TPRD32 = 0x00010000;</td>
<td>MOVL  XAR5, #0x010000</td>
</tr>
<tr>
<td>// Start CPU Timer0</td>
<td>MOVL  XAR4, #0x000C0A</td>
</tr>
<tr>
<td>*TIMER0TCR &amp;= 0xFFEF;</td>
<td>MOVL  *[XAR4[0]], XAR5</td>
</tr>
</tbody>
</table>

- Hard to read the code w/o comments
- User had to determine the bit mask

9 words, 9 cycles

* C28x Compiler v5.0.1 with -g and either -o1, -o2, or -o3 optimization level
Naming Conventions

The header files use a familiar set of naming conventions. They are consistent with the Code Composer Studio configuration tool, and generated file naming conventions.

<table>
<thead>
<tr>
<th>Structure Naming Conventions</th>
</tr>
</thead>
<tbody>
<tr>
<td>✦ The F2806x header files define:</td>
</tr>
<tr>
<td>✦ All of the peripheral structures</td>
</tr>
<tr>
<td>✦ All of the register names</td>
</tr>
<tr>
<td>✦ All of the bit field names</td>
</tr>
<tr>
<td>✦ All of the register addresses</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.all // Access full 16 or 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.half.LSW // Access low 16-bits of 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.half.MSW // Access high 16-bits of 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.bit.FieldName // Access specified bit fields of register</td>
</tr>
</tbody>
</table>

Notes:
[1] “PeripheralName” are assigned by TI and found in the F2806x header files. They are a combination of capital and small letters (i.e. CpuTimer0Regs).
[2] “RegisterName” are the same names as used in the data sheet. They are always in capital letters (i.e. TCR, TIM, TPR,...).
[3] “FieldName” are the same names as used in the data sheet. They are always in capital letters (i.e. POL, TOG, TSS,...).

The header files define all of the peripheral structures, all of the register names, all of the bit field names, and all of the register addresses. The most common naming conventions used are PeripheralName.RegisterName.all, which will access the full 16 or 32-bit register; and PeripheralName.RegisterName.bit.FieldName, which will access the specified bit fields of a register.
Editor Auto Complete to the Rescue!

The editor auto complete feature works as follows. First, you type AdcRegs. Then, when you type a “.” a window opens up, allowing you to select a control register. In this example ADCCTL1 is selected. Then, when you type the “.” a window opens up, allowing you to select “all” or “bit”. In this example “bit” is selected. Then, when you type the “.” a window opens up, allowing you to select a bit field. In this example RESET is selected. And now, the structure is completed.
F2806x C-Code Header Files

The F2806x header file package contains everything needed to use the structure approach. It defines all the peripheral register bits and register addresses. The header file package includes the header files, linker command files, code examples, and documentation. The header file package is available from controlSUITE.

<table>
<thead>
<tr>
<th>F2806x Header File Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>(<a href="http://www.ti.com">http://www.ti.com</a>, controlSUITE)</td>
</tr>
<tr>
<td>Contains everything needed to use the structure approach</td>
</tr>
<tr>
<td>Defines all peripheral register bits and register addresses</td>
</tr>
<tr>
<td>Header file package includes:</td>
</tr>
<tr>
<td>\F2806x_headers\include \rightarrow .h files</td>
</tr>
<tr>
<td>\F2806x_headers\cmd \rightarrow linker .cmd files</td>
</tr>
<tr>
<td>\F2806x_examples \rightarrow CCS examples</td>
</tr>
<tr>
<td>\doc \rightarrow documentation</td>
</tr>
</tbody>
</table>

controlSUITE Header File Package located at C:\TI\controlSUITE\device_support\ |

A peripheral is programmed by writing values to a set of registers. Sometimes, individual fields are written to as bits, or as bytes, or as entire words. Unions are used to overlap memory (register) so the contents can be accessed in different ways. The header files group all the registers belonging to a specific peripheral.

Peripheral data structures can be added to the watch window by right-clicking on the structure and selecting the option to add to watch window. This will allow viewing of the individual register fields.

Peripheral Structure .h File

The F2806x_Device.h header file is the main include file. By including this file in the .c source code, all of the peripheral specific .h header files are automatically included. Of course, each specific .h header file can be included individually in an application that does not use all the header files, or you can comment out the ones you do not need. (Also includes typedef statements).
Peripheral Structure .h files (1 of 2)

- Contain bits field structure definitions for each peripheral register

**F2806x_Adc.h**

```c
#include "F2806x_Device.h"

Void InitAdc(void)
{
    /* Reset the ADC module */
    AdcRegs.ADCCTL1.bit.RESET = 1;
    /* configure the ADC register */
    AdcRegs.ADCCTL1.all = 0x00E4;
};
```

Your C-source file (e.g., Adc.c)

```c
// ADC Individual Register Bit Definitions:
struct ADCCTL1_BITS {        // bits description
    Uint16  TEMPCONV:1;       // 0 Temperature sensor connection
    Uint16  VREFLOCONV:1;   // 1 VSSA connection
    Uint16  INTPULSEPOS:1;   // 2 INT pulse generation control
    Uint16  ADCREFSEL:1;      // 3 Internal/external reference select
    Uint16  rsvd1:1;                  // 4 reserved
    Uint16  ADCREFPWD:1;     // 5 Reference buffers powerdown
    Uint16  ADCBGPWD:1;       // 6 ADC bandgap powerdown
    Uint16  ADCPWDN:1;          // 7 ADC powerdown
    Uint16  ADCBSYCHN:5;      // 12:8 ADC busy on a channel
    Uint16  ADCBSY:1;              // 13 ADC busy signal
    Uint16  ADCENABLE:1;       // 14 ADC enable
    Uint16  RESET:1;                 // 15 ADC master reset
};

// Allow access to the bit fields or entire register:
union ADCCTL1_REG {
    Uint16                all;
    struct ADCCTL1_BITS   bit;
};

// ADC External References & Function Declarations:
extern volatile struct ADC_REGS AdcRegs;
```

Next, we will discuss the steps needed to use the header files with your project. The .h files contain the bit field structure definitions for each peripheral register.

Peripheral Structure .h files (2 of 2)

- The header file package contains a .h file for each peripheral in the device

<table>
<thead>
<tr>
<th>F2806x_Adc.h</th>
<th>F2806x_BootVars.h</th>
<th>F2806x_Cla.h</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2806x_Comp.h</td>
<td>F2806x_CpuTimers.h</td>
<td>F2806x_DevEmu.h</td>
</tr>
<tr>
<td>F2806x_Device.h</td>
<td>F2806x_Dma.h</td>
<td>F2806x_ECan.h</td>
</tr>
<tr>
<td>F2806x_ECap.h</td>
<td>F2806x_EPwm.h</td>
<td>F2806x_EQep.h</td>
</tr>
<tr>
<td>F2806x_Gpio.h</td>
<td>F2806x_I2c.h</td>
<td>F2806x_Mcbsp.h</td>
</tr>
<tr>
<td>F2806x_NmiIntrupt.h</td>
<td>F2806x_PieCtrl.h</td>
<td>F2806x_PieVect.h</td>
</tr>
<tr>
<td>F2806x_Sci.h</td>
<td>F2806x_Spi.h</td>
<td>F2806x_SysCtrl.h</td>
</tr>
<tr>
<td>F2806x_Usb.h</td>
<td>F2806x_XIntrupt.h</td>
<td></td>
</tr>
</tbody>
</table>

- **F2806x_Device.h**
  - Main include file
  - Will include all other .h files
  - Include this file (directly or indirectly) in each source file:
    ```c
    #include "F2806x_Device.h"
    ```

The header file package contains a .h file for each peripheral in the device. The F2806x_Device.h file is the main include file. It will include all of the other .h files. There are
three steps needed to use the header files. The first step is to include this file directly or indirectly in each source files.

Global Variable Definitions File

With F2806x_GlobalVariableDefs.c included in the project all the needed variable definitions are globally defined.

<table>
<thead>
<tr>
<th>Global Variable Definitions File</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2806x_GlobalVariableDefs.c</td>
</tr>
</tbody>
</table>

- Declares a global instantiation of the structure for each peripheral
- Each structure is placed in its own section using a DATA_SECTION pragma to allow linking to the correct memory (see next slide)

```c
F2806x_GlobalVariableDefs.c
#include "F2806x_Device.h"
...
#pragma DATA_SECTION(AdcRegs,"AdcRegsFile");
volatile struct ADC_REGS AdcRegs;
...
```

- Add this file to your CCS project:
  F2806x_GlobalVariableDefs.c

The global variable definition file declares a global instantiation of the structure for each peripheral. Each structure is placed in its own section using a DATA_SECTION pragma to allow linking to the correct memory. The second step for using the header files is to add F2806x_GlobalVariableDefs.c file to your project.
Mapping Structures to Memory

The data structures describe the register set in detail. And, each instance of the data type (i.e., register set) is unique. Each structure is associated with an address in memory. This is done by (1) creating a new section name via a DATA_SECTION pragma, and (2) linking the new section name to a specific memory in the linker command file.

### Linker Command Files for the Structures

**F2806x_nonBIOS.cmd** and **F2806x_BIOS.cmd**

- Links each structure to the address of the peripheral using the structures named section
- non-BIOS and BIOS versions of the .cmd file
- Add one of these files to your CCS project:
  - F2806x_nonBIOS.cmd
  - F2806x_BIOS.cmd

The header file package has two linker command file versions; one for non-BIOS projects and one for BIOS projects. This linker command file is used to link each structure to the address of the peripheral using the structures named section. The third and final step for using the header files is to add the appropriate linker command file to your project.

### Linker Command File

When using the header files, the user adds the MEMORY regions that correspond to the CODE_SECTION and DATA_SECTION pragmas found in the .h and global-definitons.c file.

The user can modify their own linker command file, or use a pre-configured linker command file such as F28069.cmd. This file has the peripheral memory regions defined and tied to the individual peripheral.
Peripheral Specific Routines

Peripheral Specific C functions are used to initialize the peripherals. They are used by adding the appropriate .c file to the project.

Peripheral Specific Examples

♦ Example projects for each peripheral
♦ Helpful to get you started

The peripheral register header file package includes example projects for each peripheral. This can be very helpful to getting you started.
Summary

Peripheral Register Header Files

- Easier code development
- Easy to use
- Generates most efficient code
- Increases effectiveness of CCS watch window
- TI has already done all the work!
  - Use the correct header file package for your device:
    - F2806x
    - F2803x
    - F2802x
    - F2833x and F2823x
    - F280x and F2801x
    - F2804x
    - F281x

Go to http://www.ti.com and enter "controlSUITE" in the keyword search box

In summary, the peripheral register header files allow for easier code development, they are easy to use, generates the most efficient code, works great with Code Composer Studio, and TI has already done the work for you. Just make sure to use the correct header file package for your device.
Reset and Interrupts

Introduction

This module describes the interrupt process and explains how the Peripheral Interrupt Expansion (PIE) works.

Module Objectives

- Describe the F28x reset process
- List the event sequence during an interrupt
- Describe the F28x interrupt structure
Module Topics

Reset and Interrupts ..........................................................................................................................4-1

Module Topics ..................................................................................................................................4-2

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  Emulation Boot Mode .....................................................................................................................4-5
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  Interrupt Enable Register (IER) ......................................................................................................4-11
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  Interrupt Signal Flow – Summary ..................................................................................................4-16
  Interrupt Response and Latency ....................................................................................................4-17
There are various reset sources available for this device: an external reset pin, watchdog timer reset, power-on reset which generates a device reset during power-up conditions, brownout reset which generates a device reset if the power supply drops below specifications for the device, as well as a missing clock detect reset. Additionally, the device incorporates an on-chip voltage regulator to generate the core voltage.
Reset - Bootloader

After reset, the PIE block is disabled and the global interrupt line is disabled. The reset vector is fetched from the boot ROM and the bootloader process begins.

Then the bootloader determines if the emulator is connected by checking the JTAG test reset line. If the emulator is connected, we are in emulation boot mode. The boot is then determined by two RAM locations named EMU_KEY and EMU_BMODE, which are located in the PIE block. If the emulator is not connected, we are in stand-alone boot mode. The boot is then determined by two GPIO pins and two OTP locations named OTP_KEY and OTP_BMODE, which are located in the OTP.
Emulation Boot Mode

If either EMU_KEY or EMU_BMODE are invalid, the “wait” boot mode is used. These values can then be modified using the debugger and a reset issued to restart the boot process.

In emulation boot mode, first the EMU_KEY register is checked to see if it has a value of 0x55AA. If either EMU_KEY or EMU_BMODE are invalid, the wait boot mode is used. These values can then be modified using the debugger and a reset issued to restart the boot process. This can be considered the default on power-up. At this point, you would like the device to wait until given a boot mode.

If EMU_KEY register has a value of 0x55AA, then the hex value in the EMU_BMODE register determines the boot mode. The boot modes are parallel I/O, SCI, SPI, I2C, OTP, CAN, M0SARAM, FLASH, and Wait. In addition, there is a GetMode, which emulates the stand-alone boot mode.
Stand-Alone Boot Mode

In stand-alone boot mode, GPIO pins 37 and 34 determine if the boot mode is parallel I/O, SCI, or wait. The default unconnected pins would set the boot mode to GetMode. In GetMode, first the OTP_KEY register is checked to see if it has a value of 0x005A. An unprogrammed OTP is set to the FLASH boot mode, as expected.

If the OTP_KEY register has a value of 0x005A, then the hex value in the OTP_BMODE register determines the boot mode. The boot modes are SCI, SPI, I2C, OTP, CAN, and FLASH.

Reset Code Flow – Summary

In summary, the reset code flow is as follows: The reset vector is fetched from the boot ROM. Then, the execution entry is determined by emulation boot mode or stand-alone boot mode. The boot mode options are M0SARAM, OTP, FLASH, and boot loading routines.
Emulation Boot Mode using Code Composer Studio GEL

The CCS GEL file can be used to setup the boot mode for the device during debug. The “OnReset()” GEL function is called each time the device is reset. This function can be modified to include a call to set the device to “Boot to SARAM” emulation mode automatically, if desired.

```c
OnReset(int nErrorCode)
{
    C28x_Mode();
    Unlock_CSM();
    Device_Cal();
    CLA_Clock_Enable(); /* Enable CLA clock */
    // EMU_BOOT_SARAM(); /* Set EMU Boot Variables - Boot to SARAM */
    // EMU_BOOT_FLASH(); /* Set EMU Boot Variables - Boot to flash */
}
```

The GEL file also provides a function to set the device to “Boot to Flash”:

```c
/* EMU Boot Mode - Set Boot Mode During Debug */
/*********************************************************************/
menuitem "EMU Boot Mode Select"
hotmenu EMU_BOOT_SARAM()
{
    *0xD00 = 0x55AA; /* EMU_KEY = 0x55AA */
    *0xD01 = 0x000A; /* Boot to SARAM */
}
hotmenu EMU_BOOT_FLASH()
{
    *0xD00 = 0x55AA; /* EMU_KEY = 0x55AA */
    *0xD01 = 0x000B; /* Boot to FLASH */
}
```

To access the GEL file use: Tools → Debugger Options → Generic Debugger Options
Getting to main()

After reset how do we get to main()?

- At the code entry point, branch to _c_int00()
  - Part of compiler runtime support library
  - Sets up compiler environment
  - Calls main()

Note: the above example is for boot mode set to M0 SARAM; to run out of Flash, the "codestart" section would be linked to the entry point of the Flash memory block.

After reset how do we get to main? When the bootloader process is completed, a branch to the compiler runtime support library is located at the code entry point. This branch to _c_int00 is executed, then the compiler environment is set up, and finally main is called.
The internal interrupt sources include the general purpose timers 0, 1, and 2, and all of the peripherals on the device. External interrupt sources include the three external interrupt lines, the trip zones, and the external reset pin. The core has 14 interrupt lines. As you can see, the number of interrupt sources exceeds the number of interrupt lines on the core. The PIE, or Peripheral Interrupt Expansion block, is connected to the core interrupt lines 1 through 12. This block manages and expands the 12 core interrupt lines, allowing up to 96 possible interrupt sources.
Interrupt Processing

Maskable Interrupt Processing

Conceptual Core Overview

- A valid signal on a specific interrupt line causes the latch to display a “1” in the appropriate bit
- If the individual and global switches are turned “on” the interrupt reaches the core

It is easier to explain the interrupt processing flow from the core back out to the interrupt sources. The INTM is the master interrupt switch. This switch must be closed for any interrupts to propagate into the core. The next layer out is the interrupt enable register. The appropriate interrupt line switch must be closed to allow an interrupt through. The interrupt flag register gets set when an interrupt occurs. Once the core starts processing an interrupt, the INTM switch opens to avoid nested interrupts and the flag is cleared.

The core interrupt registers consists of the interrupt flag register, interrupt enable register, and interrupt global mask bit. Notice that the interrupt global mask bit is zero when enabled and one when disabled. The interrupt enable register is managed by ORing and ANDing mask values. The interrupt global mask bit is managed using inline assembly.
Interrupts

Interrupt Flag Register (IFR)

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTOSINT</td>
<td>DLOGINT</td>
<td>INT14</td>
<td>INT13</td>
<td>INT12</td>
<td>INT11</td>
<td>INT10</td>
<td>INT9</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>INT8</td>
<td>INT7</td>
<td>INT6</td>
<td>INT5</td>
<td>INT4</td>
<td>INT3</td>
<td>INT2</td>
<td>INT1</td>
</tr>
</tbody>
</table>

Pending : IFR Bit = 1
Absent : IFR Bit = 0

/*** Manual setting/clearing IFR/*** 
extern cregister volatile unsigned int IFR;
IFR |= 0x0008; //set INT4 in IFR
IFR &= 0xFFF7; //clear INT4 in IFR

- Compiler generates atomic instructions (non-interruptible) for setting/clearing IFR
- If interrupt occurs when writing IFR, interrupt has priority
- IFR(bit) cleared when interrupt is acknowledged by CPU
- Register cleared on reset

Interrupt Enable Register (IER)

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
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<td>INT10</td>
<td>INT9</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>INT8</td>
<td>INT7</td>
<td>INT6</td>
<td>INT5</td>
<td>INT4</td>
<td>INT3</td>
<td>INT2</td>
<td>INT1</td>
</tr>
</tbody>
</table>

Enable: Set IER Bit = 1
Disable: Clear IER Bit = 0

/*** Interrupt Enable Register/*** 
extern cregister volatile unsigned int IER;
IER |= 0x0008; //enable INT4 in IER
IER &= 0xFFF7; //disable INT4 in IER

- Compiler generates atomic instructions (non-interruptible) for setting/clearing IER
- Register cleared on reset
Interrupt Global Mask Bit (INTM)

Interrupt Global Mask Bit

- INTM used to globally enable/disable interrupts:
  - Enable: INTM = 0
  - Disable: INTM = 1 (reset value)
- INTM modified from assembly code only:

```c
/**/ Global Interrupts /**/
asm("  CLRC  INTM"); //enable global interrupts
asm("  SETC  INTM"); //disable global interrupts
```

Peripheral Interrupt Expansion (PIE)

Peripheral Interrupt Expansion - PIE

We have already discussed the interrupt process in the core. Now we need to look at the
Peripheral interrupt expansion block. This block is connected to the core interrupt lines 1 through 12. The PIE block consists of 12 groups. Within each group, there are eight interrupt sources. Each group has a PIE interrupt enable register and a PIE interrupt flag register.

As you can see, the interrupts are numbered from 1.1 through 12.8, giving us a maximum of 96 interrupt sources. Interrupt lines 13, 14, and NMI bypass the PIE block.

**F2806x PIE Interrupt Assignment Table**

<table>
<thead>
<tr>
<th>INTx.8</th>
<th>INTx.7</th>
<th>INTx.6</th>
<th>INTx.5</th>
<th>INTx.4</th>
<th>INTx.3</th>
<th>INTx.2</th>
<th>INTx.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT1</td>
<td>WAKEINT</td>
<td>INTINT0</td>
<td>ADCINT9</td>
<td>XINT2</td>
<td>XINT1</td>
<td>ADCINT2</td>
<td>ADCINT1</td>
</tr>
<tr>
<td>INT2</td>
<td>EPWM8 _TZINT</td>
<td>EPWM7 _TZINT</td>
<td>EPWM6 _TZINT</td>
<td>EPWM5 _TZINT</td>
<td>EPWM4 _TZINT</td>
<td>EPWM3 _TZINT</td>
<td>EPWM2 _TZINT</td>
</tr>
<tr>
<td>INT3</td>
<td>EPWM8 _INT</td>
<td>EPWM7 _INT</td>
<td>EPWM6 _INT</td>
<td>EPWM5 _INT</td>
<td>EPWM4 _INT</td>
<td>EPWM3 _INT</td>
<td>EPWM2 _INT</td>
</tr>
<tr>
<td>INT4</td>
<td>HRCAPI2 _INT</td>
<td>HRCAPI1 _INT</td>
<td>ECAPI3 _INT</td>
<td>ECAPI2 _INT</td>
<td>ECAPI1 _INT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT5</td>
<td>HRCAPT2 _INT</td>
<td>HRCAPT1 _INT</td>
<td>ECAPI3 _INT</td>
<td>ECAPI2 _INT</td>
<td>ECAPI1 _INT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT6</td>
<td>MXINTA</td>
<td>MRINTA</td>
<td>SPIRTX INTB</td>
<td>SPIRX INTB</td>
<td>SPIRTX INTA</td>
<td>SPIRX INTA</td>
<td></td>
</tr>
<tr>
<td>INT7</td>
<td>DINTCH6</td>
<td>DINTCH5</td>
<td>DINTCH4</td>
<td>DINTCH3</td>
<td>DINTCH2</td>
<td>DINTCH1</td>
<td></td>
</tr>
<tr>
<td>INT8</td>
<td>I2CINT2A</td>
<td>I2CINT1A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT9</td>
<td>ECAN1 _INTA</td>
<td>ECAN0 _INTA</td>
<td>SCITX INTB</td>
<td>SCIRX INTA</td>
<td>SCITX INTA</td>
<td>SCIRX INTA</td>
<td></td>
</tr>
<tr>
<td>INT10</td>
<td>ADCINT8</td>
<td>ADCINT7</td>
<td>ADCINT6</td>
<td>ADCINT5</td>
<td>ADCINT4</td>
<td>ADCINT3</td>
<td>ADCINT2</td>
</tr>
<tr>
<td>INT11</td>
<td>CLA1 _INT8</td>
<td>CLA1 _INT7</td>
<td>CLA1 _INT6</td>
<td>CLA1 _INT5</td>
<td>CLA1 _INT4</td>
<td>CLA1 _INT3</td>
<td>CLA1 _INT2</td>
</tr>
<tr>
<td>INT12</td>
<td>LUF</td>
<td>LVF</td>
<td>XINT3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The interrupt assignment table tells us the location for each interrupt source within the PIE block. Notice the table is numbered from 1.1 through 12.8, perfectly matching the PIE block.

The PIE registers consist of 12 PIE interrupt flag registers, 12 PIE interrupt enable registers, a PIE interrupt acknowledge register, and a PIE control register. The enable PIE bit in the PIE control register must be set during initialization for the PIE block to be enabled.
The interrupt vector table, as mapped in the PIE interrupt assignment table, is located in the PieVect.c file. During initialization in main, we have a function call to PieCtrl.c. In this file, a
memory copy function copies the interrupt vector table to the PIE RAM and then sets ENPIE to 1, enabling the PIE block. This process is done to set up the vectors for interrupts.

In summary, the PIE initialization code flow is as follows. After the device is reset and executes the boot code, the selected boot option determines the code entry point. This figure shows two different entry points. The one on the left is for memory block M0, and the one on the right is for flash.

In either case, CodeStartBranch.asm has a “Long Branch” to the entry point of the runtime support library. After the runtime support library completes execution, it calls main. In main, we have a function call to initialize the interrupt process and enable the PIE block. When an interrupt occurs, the PIE block contains a vector to the interrupt service routine located in DefaultIsr.c.
In summary, the following steps occur during an interrupt process. First, a peripheral interrupt is generated and the PIE interrupt flag register is set. If the PIE interrupt enable register is enabled, then the core interrupt flag register will be set. Next, if the core interrupt enable register and global interrupt mask is enabled, the PIE vector table will redirect the code to the interrupt service routine.
Interrupt Response and Latency

Interrupt Response - Hardware Sequence

<table>
<thead>
<tr>
<th>CPU Action</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers → stack</td>
<td>14 Register words auto saved</td>
</tr>
<tr>
<td>0 → IFR (bit)</td>
<td>Clear corresponding IFR bit</td>
</tr>
<tr>
<td>0 → IER (bit)</td>
<td>Clear corresponding IER bit</td>
</tr>
<tr>
<td>1 → INTM/DBGM</td>
<td>Disable global ints/debug events</td>
</tr>
<tr>
<td>Vector → PC</td>
<td>Loads PC with int vector address</td>
</tr>
<tr>
<td>Clear other status bits</td>
<td>Clear LOOP, EALLOW, IDLESTAT</td>
</tr>
</tbody>
</table>

Note: some actions occur simultaneously, none are interruptible

<table>
<thead>
<tr>
<th>T</th>
<th>ST0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AH</td>
<td>AL</td>
</tr>
<tr>
<td>PH</td>
<td>PL</td>
</tr>
<tr>
<td>AR1</td>
<td>AR0</td>
</tr>
<tr>
<td>DP</td>
<td>ST1</td>
</tr>
<tr>
<td>DBSTAT</td>
<td>IER</td>
</tr>
<tr>
<td>PC(msw)</td>
<td>PC(lsw)</td>
</tr>
</tbody>
</table>

Interrupt Latency

- Minimum latency (to when real work occurs in the ISR):
  - Internal interrupts: 14 cycles
  - External interrupts: 16 cycles
- Maximum latency: Depends on wait states, INTM, etc.
Introduction

This module discusses the operation of the OSC/PLL-based clock module and watchdog timer. Also, the general-purpose digital I/O ports, external interrupts, various low power modes and the EALLOW protected registers will be covered.

Module Objectives

- OSC/PLL Clock Module
- Watchdog Timer
- General Purpose Digital I/O
- External Interrupts
- Low Power Modes
- Register Protection
Module Topics

System Initialization ................................................................................................................................... 5-1
  Module Topics ........................................................................................................................................ 5-2
  Oscillator/PLL Clock Module ........................................................................................................... 5-3
  Watchdog Timer ................................................................................................................................. 5-7
  General-Purpose Digital I/O ............................................................................................................ 5-12
  External Interrupts ............................................................................................................................. 5-16
  Low Power Modes .............................................................................................................................. 5-17
  Register Protection ............................................................................................................................. 5-19
  Lab 5: System Initialization .............................................................................................................. 5-21
The oscillator/PLL clock module has two internal, 10 MHz oscillators, and the availability of an external oscillator or crystal. This provides redundancy in case an oscillator fails, as well as the ability to use multiple oscillators. The asterisks in the multiplexers show the default settings. This module has the capability to clock the watchdog, core, and CPU timer 2 from independent clock sources, if needed.

The on-chip oscillator and phase-locked loop (PLL) block provide all the necessary clocking signals for the F2806x devices. The two internal oscillators (INTOSC1 and INTOSC2) need no external components.
A clock source can be fed directly into the core or multiplied using the PLL. The PLL gives us the capability to use the internal 10 MHz oscillator multiplied by 18/2, and run the device at the full 90 MHz clock frequency. If the input clock is removed after the PLL is locked, the input clock failed detect circuitry will issue a limp mode clock of 1 to 4 MHz. Additionally, an internal device reset will be issued. The low-speed peripheral clock prescaler is used to clock some of the communication peripherals.

The PLL has a 4-bit ratio control to select different CPU clock rates. In addition to the on-chip oscillators, two external modes of operation are supported – crystal operation, and external clock source operation. Crystal operation allows the use of an external crystal/resonator to provide the time base to the device. External clock source operation allows the internal (crystal) oscillator to be bypassed, and the device clocks are generated from an external clock source input on the XCLKIN pin. The C28x core provides a SYSCLKOUT clock signal. This signal is prescaled to provide a clock source for some of the on-chip communication peripherals through the low-speed peripheral clock prescaler. Other peripherals are clocked by SYSCLKOUT and use their own clock prescalers for operation.
Oscillator/PLL Clock Module

Clock Control Register
SysCtrlRegs.CLKCTL (lab file: SysCtrl.c)

Upper Register:

- **Watchdog HALT Mode Ignore**
  - 0 = automatic turn on/off
  - 1 = ignores HALT Mode

- **Internal Oscillator 1 HALT Mode Ignore**
  - 0 = automatic turn on/off
  - 1 = ignores HALT Mode

- **Internal Oscillator 1 Off**
  - 0 = on
  - 1 = off

- **Nmireset**
  - 0 = default

- **XTAL Oscillator OFF**
  - 0 = on
  - 1 = off

- **INTOSC2 HALT1**
  - 0 = on
  - 1 = off

- **INTOSC1 HALT1**
  - 0 = on
  - 1 = off

- **INTOSC2 OFF**
  - 0 = on
  - 1 = off

- **INTOSC1 OFF**
  - 0 = on
  - 1 = off

- **XCLKIN Off**
  - 0 = on
  - 1 = off

- **Crystal Oscillator Off**
  - 0 = on
  - 1 = off

- **Watchdog HALT Mode Ignore**
  - 0 = automatic turn on/off
  - 1 = ignores HALT Mode

- **CPU Timer 2 Clock Prescale**
  - 000 = /1
  - 001 = /2
  - 010 = /4
  - 011 = /8
  - 100 = /16
  - 1xx = reserved

- **CPU Timer 2 Clock Source**
  - 00 = SYSCLKOUT
  - 01 = external
  - 10 = internal OSC1
  - 11 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = external
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

Clock Control Register
SysCtrlRegs.CLKCTL (lab file: SysCtrl.c)

Lower Register:

- **Watchdog Clock Source**
  - 0 = internal OSC1
  - 1 = external or internal OSC2

- **Oscillator Clock Source**
  - 0 = internal OSC1
  - 1 = external or internal OSC2

- **CPU Timer 2 Clock Prescale**
  - 000 = /1
  - 001 = /2
  - 010 = /4
  - 011 = /8
  - 100 = /16
  - 1xx = reserved

- **CPU Timer 2 Clock Source**
  - 00 = SYSCLKOUT
  - 01 = external
  - 10 = internal OSC1
  - 11 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = external
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2

- **Oscillator 2 Clock Source**
  - 0 = internal OSC1
  - 1 = internal OSC2
The peripheral clock control register allows individual peripheral clock signals to be enabled or disabled. If a peripheral is not being used, its clock signal could be disabled, thus reducing power consumption.
Watchdog Timer

The watchdog timer is a safety feature, which resets the device if the program runs away or gets trapped in an unintended infinite loop. The watchdog counter runs independent of the CPU. If the counter overflows, a reset or interrupt is triggered. The CPU must write the correct data key sequence to reset the counter before it overflows.

The watchdog timer provides a safeguard against CPU crashes by automatically initiating a reset if it is not serviced by the CPU at regular intervals. In motor control applications, this helps protect the motor and drive electronics when control is lost due to a CPU lockup. Any CPU reset will revert the PWM outputs to a high-impedance state, which should turn off the power converters in a properly designed system.

The watchdog timer is running immediately after system power-up/reset, and must be dealt with by software soon after. Specifically, you have 13.11 ms (with a 10 MHz watchdog clock) after any reset before a watchdog initiated reset will occur. This translates into 131,072 WDCLK cycles, which is a seemingly tremendous amount! Indeed, this is plenty of time to get the watchdog configured as desired and serviced. A failure of your software to properly handle the watchdog after reset could cause an endless cycle of watchdog initiated resets to occur.
The watchdog clock is divided by 512 and prescaled, if desired. The watchdog disable switch allows the watchdog to be enabled and disabled. The watchdog override switch is a safety mechanism, and once closed, it can only be open by resetting the device.

During initialization, “101” is written into the watchdog check bit fields. Any other values will cause a reset or interrupt. During run time, the correct keys must be written into the watchdog key register before the watchdog counter overflows and issues a reset or interrupt. Issuing a reset or interrupt is user-selectable.
Watchdog Timer

Watchdog Period Selection

<table>
<thead>
<tr>
<th>WDPS Bits</th>
<th>FRC rollover</th>
<th>WD timeout period @ 10 MHz WDCLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>00x:</td>
<td>1</td>
<td>13.11 ms *</td>
</tr>
<tr>
<td>010:</td>
<td>2</td>
<td>26.22 ms</td>
</tr>
<tr>
<td>011:</td>
<td>4</td>
<td>52.44 ms</td>
</tr>
<tr>
<td>100:</td>
<td>8</td>
<td>104.88 ms</td>
</tr>
<tr>
<td>101:</td>
<td>16</td>
<td>209.76 ms</td>
</tr>
<tr>
<td>110:</td>
<td>32</td>
<td>419.52 ms</td>
</tr>
<tr>
<td>111:</td>
<td>64</td>
<td>839.04 ms</td>
</tr>
</tbody>
</table>

* reset default

- Remember: Watchdog starts counting immediately after reset is released!
- Reset default with WDCLK = 10 MHz computed as 
  \((1/10 \text{ MHz}) \times 512 \times 256 = 13.11 \text{ ms}\)

Watchdog Timer Control Register

SysCtrlRegs.WDCR (lab file: Watchdog.c)

- WD Flag Bit
  - Gets set when the WD causes a reset
  - Writing a 1 clears this bit
  - Writing a 0 has no effect

- WD Flag Bit
- WDDIS
- WDCHK
- WDPS

Watchdog Disable Bit
- Write 1 to disable
  - (Functions only if WD OVERRIDE bit in SCSR is equal to 1)
Resetting the Watchdog
SysCtrlRegs.WDKEY (lab file: Watchdog.c)

- WDKEY write values:
  - 55h - counter enabled for reset on next AAh write
  - AAh - counter set to zero if reset enabled
- Writing any other value has no effect
- Watchdog should not be serviced solely in an ISR
  - If main code crashes, but interrupt continues to execute, the watchdog will not catch the crash
  - Could put the 55h WDKEY in the main code, and the AAh WDKEY in an ISR; this catches main code crashes and also ISR crashes

<table>
<thead>
<tr>
<th>Sequential Step</th>
<th>Value Written to WDKEY</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AAh</td>
<td>No action</td>
</tr>
<tr>
<td>2</td>
<td>AAh</td>
<td>No action</td>
</tr>
<tr>
<td>3</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>4</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>5</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>6</td>
<td>AAh</td>
<td>WD counter is reset</td>
</tr>
<tr>
<td>7</td>
<td>AAh</td>
<td>No action</td>
</tr>
<tr>
<td>8</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>9</td>
<td>AAh</td>
<td>WD counter is reset</td>
</tr>
<tr>
<td>10</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>11</td>
<td>23h</td>
<td>No effect; WD counter not reset on next AAh write</td>
</tr>
<tr>
<td>12</td>
<td>AAh</td>
<td>No action due to previous invalid value</td>
</tr>
<tr>
<td>13</td>
<td>55h</td>
<td>WD counter enabled for reset on next AAh write</td>
</tr>
<tr>
<td>14</td>
<td>AAh</td>
<td>WD counter is reset</td>
</tr>
</tbody>
</table>
**System Control and Status Register**

SysCtrlRegs.SCSR (lab file: Watchdog.c)

**WD Override (protect bit)**
Protects WD from being disabled

- 0 = WDDIS bit in WDCR has no effect (WD cannot be disabled)
- 1 = WDDIS bit in WDCR can disable the watchdog

- This bit is a *clear-only* bit (write 1 to clear)
- The reset default of this bit is a 1

<table>
<thead>
<tr>
<th>15 - 3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>WDINTS</td>
<td>WDENINT</td>
<td>WDOVERRIDE</td>
</tr>
</tbody>
</table>

**WD Interrupt Status (read only)**

- 0 = active
- 1 = not active

**WD Enable Interrupt**

- 0 = WD generates a MCU reset
- 1 = WD generates a WDINT interrupt
Each general-purpose I/O pin has a maximum of four options, either general-purpose I/O or up to three possible peripheral pin assignments. This is selected using the GPIO port multiplexer. If the pin is set to GPIO, the direction register sets it as an input or an output. The input qualification will be explained shortly.

* See device datasheet for pin function selection matrices
The GPIO pin block diagram shows a single GPIO pin. If the pin is set as a GPIO by the GPIO multiplexer, the direction will be set by the GPIO direction register. The GPIO data register will have the value of the pin if set as an input or write the value of the data register to the pin if set as an output.

The data register can be quickly and easily modified using set, clear, or toggle registers. As you can see, the GPIO multiplexer can be set to select up to three other possible peripheral pin assignments. Also, the pin has an option for an internal pull-up.

The GPIO input qualification feature allows filtering out noise on a pin. The user would select the number of samples and qualification period. Qualification is available on ports A and B only and is individually selectable per pin.
F2806x GPIO Input Qual Registers

GpioCtrlRegs.register (lab file: Gpio.c)

GPAQSEL1 / GPAQSEL2 / GPBQSEL1

<table>
<thead>
<tr>
<th>31</th>
<th>16 pins configured per register</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>sync to SYSCLKOUT only *</td>
</tr>
<tr>
<td>01</td>
<td>qual to 3 samples</td>
</tr>
<tr>
<td>10</td>
<td>qual to 6 samples</td>
</tr>
<tr>
<td>11</td>
<td>no sync or qual (for peripheral only; GPIO same as 00)</td>
</tr>
</tbody>
</table>

GPACTRL / GPBCTRL

<table>
<thead>
<tr>
<th>31</th>
<th>24</th>
<th>16</th>
<th>8</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>QUALPRD3</td>
<td>QUALPRD2</td>
<td>QUALPRD1</td>
<td>QUALPRD0</td>
<td></td>
</tr>
<tr>
<td>B: GPIO56-63</td>
<td>GPIO48-55</td>
<td>GPIO47-40</td>
<td>GPIO39-32</td>
<td></td>
</tr>
<tr>
<td>A: GPIO31-24</td>
<td>GPIO23-16</td>
<td>GPIO15-8</td>
<td>GPIO7-0</td>
<td></td>
</tr>
</tbody>
</table>

| 00h | no qualification (SYNC to SYSCLKOUT) * |
| 01h | QUALPRD = SYSCLKOUT/2 |
| 02h | QUALPRD = SYSCLKOUT/4 |
| ... | ... |
| FFh | QUALPRD = SYSCLKOUT/510 |

* reset default

F2806x GPIO Control Registers

GpioCtrlRegs.register (lab file: Gpio.c)

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPACTRL</td>
<td>GPIO A Control Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPAQSEL1</td>
<td>GPIO A Qualifier Select 1 Register [GPIO 0 – 15]</td>
</tr>
<tr>
<td>GPAQSEL2</td>
<td>GPIO A Qualifier Select 2 Register [GPIO 16 – 31]</td>
</tr>
<tr>
<td>GPAMUX1</td>
<td>GPIO A Mux1 Register [GPIO 0 – 15]</td>
</tr>
<tr>
<td>GPAMUX2</td>
<td>GPIO A Mux2 Register [GPIO 16 – 31]</td>
</tr>
<tr>
<td>GPADIR</td>
<td>GPIO A Direction Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPPAUDP</td>
<td>GPIO A Pull-Up Disable Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPBCTRL</td>
<td>GPIO B Control Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>GPBQSEL1</td>
<td>GPIO B Qualifier Select 1 Register [GPIO 32 – 47]</td>
</tr>
<tr>
<td>GPBQSEL2</td>
<td>GPIO B Qualifier Select 2 Register [GPIO 48 – 63]</td>
</tr>
<tr>
<td>GPBMUX1</td>
<td>GPIO B Mux1 Register [GPIO 32 – 47]</td>
</tr>
<tr>
<td>GPBMUX2</td>
<td>GPIO B Mux2 Register [GPIO 48 – 63]</td>
</tr>
<tr>
<td>GPBDIR</td>
<td>GPIO B Direction Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>GPBPUD</td>
<td>GPIO B Pull-Up Disable Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>AIOMUX1</td>
<td>ANALOG I/O Mux1 Register [AIO 0 – 15]</td>
</tr>
<tr>
<td>AIODIR</td>
<td>ANALOG I/O Direction Register [AIO 0 – 15]</td>
</tr>
</tbody>
</table>
## F2806x GPIO Data Registers

GpioDataRegs.register (lab file: Gpio.c)

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPADAT</td>
<td>GPIO A Data Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPASET</td>
<td>GPIO A Data Set Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPACLEAR</td>
<td>GPIO A Data Clear Register [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPATOGGLE</td>
<td>GPIO A Data Toggle [GPIO 0 – 31]</td>
</tr>
<tr>
<td>GPBDAT</td>
<td>GPIO B Data Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>GPBSET</td>
<td>GPIO B Data Set Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>GPBCLEAR</td>
<td>GPIO B Data Clear Register [GPIO 32 – 63]</td>
</tr>
<tr>
<td>GPBToggle</td>
<td>GPIO B Data Toggle [GPIO 32 – 63]</td>
</tr>
<tr>
<td>AIODAT</td>
<td>ANALOG I/O Data Register [AIO 0 – 15]</td>
</tr>
<tr>
<td>AIOSET</td>
<td>ANALOG I/O Data Set Register [AIO 0 – 15]</td>
</tr>
<tr>
<td>AIOCLEAR</td>
<td>ANALOG I/O Data Clear Register [AIO 0 – 15]</td>
</tr>
<tr>
<td>AIOTOGGLE</td>
<td>ANALOG I/O Data Toggle [AIO 0 – 15]</td>
</tr>
</tbody>
</table>
External Interrupts

- 3 external interrupt signals: XINT1, XINT2 and XINT3
- XINT1, XINT2 and XINT3 can be mapped to any of GPIO0-31
- XINT1, XINT2 and XINT3 also each have a free-running 16-bit counter that measures the elapsed time between interrupts
  - The counter resets to zero each time the interrupt occurs

External Interrupt Registers

- Pin Selection Register chooses which pin the signal comes out on
  - Only one pin can be assigned to each interrupt signal
- Configuration Register controls the enable/disable and polarity
- Counter Register holds the interrupt counter
Low Power Modes

<table>
<thead>
<tr>
<th>Low Power Mode</th>
<th>CPU Logic Clock</th>
<th>Peripheral Logic Clock</th>
<th>Watchdog Clock</th>
<th>PLL / OSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Run</td>
<td>on</td>
<td>on</td>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>IDLE</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>STANDBY</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>HALT</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
</tr>
</tbody>
</table>

See device datasheet for power consumption in each mode

Low Power Mode Control Register 0
SysCtrlRegs.LPMCR0 (lab file: SysCtrl.c)

Watchdog Interrupt
- wake device from STANDBY
- 0 = disable (default)
- 1 = enable

WAKE from STANDBY
- GPIO signal qualification *
- 000000 = 2 OSCCLKs
- 000001 = 3 OSCCLKs
- 111111 = 65 OSCCLKs (default)

Low Power Mode Entering
1. Set LPM bits
2. Enable desired exit interrupt(s)
3. Execute IDLE instruction
4. The power down sequence of the hardware depends on LP mode

Low Power Mode Selection
- 00 = Idle (default)
- 01 = Standby
- 1x = Halt

* QUALSTDBY will qualify the GPIO wakeup signal in series with the GPIO port qualification.
This is useful when GPIO port qualification is not available or insufficient for wake-up purposes.
### Low Power Mode Exit

<table>
<thead>
<tr>
<th>Low Power Mode</th>
<th>Exit Interrupt</th>
<th>RESET</th>
<th>GPIO Port A Signal</th>
<th>Watchdog Interrupt</th>
<th>Any Enabled Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLE</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>STANDBY</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>HALT</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
</tbody>
</table>

### GPIO Low Power Wakeup Select

```
<table>
<thead>
<tr>
<th>GPIO31</th>
<th>GPIO30</th>
<th>GPIO29</th>
<th>GPIO28</th>
<th>GPIO27</th>
<th>GPIO26</th>
<th>GPIO25</th>
<th>GPIO24</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO23</td>
<td>GPIO22</td>
<td>GPIO21</td>
<td>GPIO20</td>
<td>GPIO19</td>
<td>GPIO18</td>
<td>GPIO17</td>
<td>GPIO16</td>
</tr>
<tr>
<td>GPIO15</td>
<td>GPIO14</td>
<td>GPIO13</td>
<td>GPIO12</td>
<td>GPIO11</td>
<td>GPIO10</td>
<td>GPIO09</td>
<td>GPIO08</td>
</tr>
<tr>
<td>GPIO07</td>
<td>GPIO06</td>
<td>GPIO05</td>
<td>GPIO04</td>
<td>GPIO03</td>
<td>GPIO02</td>
<td>GPIO01</td>
<td>GPIO00</td>
</tr>
</tbody>
</table>
```

Wake device from HALT and STANDBY mode (GPIO Port A)
- 0 = disable (default)
- 1 = enable
Register Protection

**Write-Read Protection**

Suppose you need to write to a peripheral register and then read a different register for the same peripheral (e.g., write to control, read from status register)?

- CPU pipeline protects W-R order for the same address
- Write-Read protection mechanism protects W-R order for different addresses
  - Peripheral Frame 0 and Peripheral Frame 1 zones protected
  - Write-read protection mode bit ENPROT located in the DEVICECNF register is enabled by default

### Peripheral Frame Registers

<table>
<thead>
<tr>
<th>PF0</th>
<th>PF1</th>
</tr>
</thead>
<tbody>
<tr>
<td>eCAN</td>
<td>System Control</td>
</tr>
<tr>
<td>COMP</td>
<td>SPI</td>
</tr>
<tr>
<td>ePWM</td>
<td>SCI</td>
</tr>
<tr>
<td>eCAP</td>
<td>Watchdog</td>
</tr>
<tr>
<td>eQEP</td>
<td>XINT</td>
</tr>
<tr>
<td>LIN</td>
<td>ADC</td>
</tr>
<tr>
<td>GPIO</td>
<td>I2C</td>
</tr>
</tbody>
</table>

**Protected address:** 0x4000 - 0x7FFF

### EALLOW Protection (1 of 2)

- **EALLOW stands for Emulation Allow**
- Code access to protected registers allowed only when EALLOW = 1 in the ST1 register
- The emulator can always access protected registers
- EALLOW bit controlled by assembly level instructions
  - ‘EALLOW’ sets the bit (register access enabled)
  - ‘EDIS’ clears the bit (register access disabled)
- EALLOW bit cleared upon ISR entry, restored upon exit
EALLOW Protection (2 of 2)

The following registers are protected:

- Device Emulation
- Flash
- Code Security Module
- PIE Vector Table
- LIN (some registers)
- eCAN A/B (control registers only; mailbox RAM not protected)
- ePWM1-7 and COMP1-3 (some registers)
- GPIO (control registers only)
- System Control

See device datasheet and peripheral users guides for detailed listings

EALLOW register access C-code example:

```c
asm(" EALLOW"); // enable protected register access
SysCtrlRegs.WDKEY=0x55; // write to the register
asm(" EDIS"); // disable protected register access
```
Lab 5: System Initialization

Objective

The objective of this lab is to perform the processor system initialization. Additionally, the peripheral interrupt expansion (PIE) vectors will be initialized and tested using the information discussed in the previous module. This initialization process will be used again in all of the lab exercises throughout this workshop. The system initialization for this lab will consist of the following:

- Setup the clock module – PLL, LOSPCP = /4, low-power modes to default values, enable all module clocks
- Disable the watchdog – clear WD flag, disable watchdog, WD prescale = 1
- Setup the watchdog and system control registers – DO NOT clear WD OVERRIDE bit, configure WD to generate a CPU reset
- Setup the shared I/O pins – set all GPIO pins to GPIO function (e.g. a "00" setting for GPIO function, and a “01”, “10”, or “11” setting for a peripheral function)

The first part of the lab exercise will setup the system initialization and test the watchdog operation by having the watchdog cause a reset. In the second part of the lab exercise the PIE vectors will be added and tested by using the watchdog to generate an interrupt. This lab will make use of the F2806x C-code header files to simplify the programming of the device, as well as take care of the register definitions and addresses. Please review these files, and make use of them in the future, as needed.

Procedure

Create a New Project

1. Create a new project (File → New → CCS Project) for this lab exercise. The top section should default to the options previously selected (setting the “Target” to “Experimenter’s Kit – Piccolo F28069”, and leaving the “Connection” box blank). Name the project Lab5. Uncheck the “Use default location” box. Using the Browse… button navigate to: C:\C28x\Labs\Lab5\Project then click OK. Set the “Linker Command File” to <none>, and be sure to set the “Project templates and examples” to “Empty Project”. Then click Finish.

2. Right-click on Lab5 in the Project Explorer window and add (copy) the following files to the project (Add Files…) from C:\C28x\Labs\Lab5\Files:

   CodeStartBranch.asm
   DelayUs.asm
   F2806x_DefaultIsr.h
   F2806x_GlobalVariableDefs.c
   F2806x_Headers_nonBIOS.cmd
   Gpio.c
   Lab.h
   Lab_5_6_7.cmd
   Main_5.c
   SysCtrl1.c
   Watchdog.c
Do not add DefaultIsr_5.c, PieCtrl.c, and PieVect.c. These files will be added and used with the interrupts in the second part of this lab exercise.

Project Build Options

3. Setup the build options by right-clicking on Lab5 in the Project Explorer window and select Properties. We need to setup the include search path to include the peripheral register header files. Under “C2000 Compiler” select “Include Options”. In the lower box that opens (“Add dir to #include search path”) click the Add icon (first icon with green plus sign). Then in the “Add directory path” window type:

$\{PROJECT_ROOT\}/../../F2806x_headers/include

Click OK to include the search path. Finally, click OK to save and close the Properties window.

Modify Memory Configuration

4. Open and inspect the linker command file Lab_5_6_7.cmd. Notice that the user defined section “codestart” is being linked to a memory block named BEGIN_M0. The codestart section contains code that branches to the code entry point of the project. The bootloader must branch to the codestart section at the end of the boot process. Recall that the emulation boot mode "M0 SARAM" branches to address 0x000000 upon bootloader completion.

Modify the linker command file Lab_5_6_7.cmd to create a new memory block named BEGIN_M0: origin = 0x000000, length = 0x0002, in program memory. You will also need to modify the existing memory block M0SARAM in data memory to avoid any overlaps with this new memory block.

5. In the linker command file, notice that RESET in the MEMORY section has been defined using the “(R)” qualifier. This qualifier indicates read-only memory, and is optional. It will cause the linker to flag a warning if any uninitialized sections are linked to this memory. The (R) qualifier can be used with all non-volatile memories (e.g., flash, ROM, OTP), as you will see in later lab exercises.

Setup System Initialization

6. Modify SysCtrl.c and Watchdog.c to implement the system initialization as described in the objective for this lab.

7. Open and inspect Gpio.c. Notice that the shared I/O pins have been set to the GPIO function. Save your work and close the modified files.

Build and Load

8. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.
9. Click the “Debug” button (green bug). The “CCS Debug Perspective” view should open, the program will load automatically, and you should now be at the start of main().

10. After CCS loaded the program in the previous step, it set the program counter (PC) to point to _c_int00. It then ran through the C-environment initialization routine in the rts2800_fpu32.lib and stopped at the start of main(). CCS did not do a device reset, and as a result the bootloader was bypassed.

In the remaining parts of this lab exercise, the device will be undergoing a reset due to the watchdog timer. Therefore, we must configure the device by loading values into EMU_KEY and EMU_BMODE so the bootloader will jump to “M0 SARAM” at address 0x000000. Set the bootloader mode using the menu bar by clicking:

Scripts → EMU Boot Mode Select → EMU_BOOT_SARAM

If the device is power cycled between lab exercises, or within a lab exercise, be sure to re-configure the boot mode to EMU_BOOT_SARAM.

Run the Code – Watchdog Reset

11. Place the cursor in the “main loop” section (on the asm(" NOP"); instruction line) and right click the mouse key and select Run To Line. This is the same as setting a breakpoint on the selected line, running to that breakpoint, and then removing the breakpoint.

12. Place the cursor on the first line of code in main() and set a breakpoint by double clicking in the line number field to the left of the code line. Notice that line is highlighted with a blue dot indicating that the breakpoint has been set. (Alternately, you can set a breakpoint on the line by right-clicking the mouse and selecting Breakpoint (Code Composer Studio) → Breakpoint). The breakpoint is set to prove that the watchdog is disabled. If the watchdog causes a reset, code execution will stop at this breakpoint.

13. Run your code for a few seconds by using the “Resume” button on the toolbar, or by using Run → Resume on the menu bar (or F8 key). After a few seconds halt your code by using the “Suspend” button on the toolbar, or by using Run → Suspend on the menu bar (or Alt-F8 key). Where did your code stop? Are the results as expected? If things went as expected, your code should be in the “main loop”.

14. Switch to the “CCS Edit Perspective” view by clicking the CCS Edit icon in the upper right-hand corner. Modify the InitWatchdog() function to enable the watchdog (WDCR). This will enable the watchdog to function and cause a reset. Save the file.

15. Click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.

16. Like before, place the cursor in the “main loop” section (on the asm(" NOP"); instruction line) and right click the mouse key and select Run To Line.

17. Run your code. Where did your code stop? Are the results as expected? If things went as expected, your code should have stopped at the breakpoint. What happened is as
follows. While the code was running, the watchdog timed out and reset the processor. The reset vector was then fetched and the ROM bootloader began execution. Since the device is in emulation boot mode (i.e. the emulator is connected) the bootloader read the EMU_KEY and EMU_BMODE values from the PIE RAM. These values were previously set for boot to M0 SARAM boot mode by CCS. Since these values did not change and are not affected by reset, the bootloader transferred execution to the beginning of our code at address 0x000000 in the M0SARAM, and execution continued until the breakpoint was hit in main().

Setup PIE Vector for Watchdog Interrupt

The first part of this lab exercise used the watchdog to generate a CPU reset. This was tested using a breakpoint set at the beginning of main(). Next, we are going to use the watchdog to generate an interrupt. This part will demonstrate the interrupt concepts learned in the previous module.

18. In the “CCS Edit Perspective” view add (copy) the following files to the project from C:\C28x\Labs\Lab5\Files:
   - DefaultIsr_5.c
   - PieCtrl.c
   - PieVect.c

   Check your files list to make sure the files are there.

19. In Main_5.c, add code to call the InitPieCtrl() function. There are no passed parameters or return values, so the call code is simply:

   InitPieCtrl();

20. Using the “PIE Interrupt Assignment Table” shown in the previous module find the location for the watchdog interrupt, “WAKEINT”. This will be used in the next step.

   PIE group #:__________  # within group:__________

21. Modify main() to do the following:
   - Enable global interrupts (INTM bit)

   Then modify InitWatchdog() to do the following:
   - Enable the “WAKEINT” interrupt in the PIE (Hint: use the PieCtrlRegs structure)
   - Enable the appropriate core interrupt in the IER register

22. In Watchdog.c modify the system control and status register (SCSR) to cause the watchdog to generate a WAKEINT rather than a reset. Save all changes to the files.

23. Open and inspect DefaultIsr_5.c. This file contains interrupt service routines. The ISR for WAKEINT has been trapped by an emulation breakpoint contained in an inline assembly statement using “ESTOP0”. This gives the same results as placing a breakpoint in the ISR. We will run the lab exercise as before, except this time the watchdog will generate an interrupt. If the registers have been configured properly, the code will be trapped in the ISR.
24. Open and inspect PieCtrl.c. This file is used to initialize the PIE RAM and enable the PIE. The interrupt vector table located in PieVect.c is copied to the PIE RAM to setup the vectors for the interrupts. Close the modified and inspected files.

**Build and Load**

25. Click the “Build” button and select Yes to “Reload the program automatically”. Switch to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.

**Run the Code – Watchdog Interrupt**

26. Place the cursor in the “main loop” section, right click the mouse key and select Run To Line.

27. Run your code. Where did your code stop? Are the results as expected? If things went as expected, your code should stop at the “ESTOP0” instruction in the WAKEINT ISR.

**Terminate Debug Session and Close Project**

28. Terminate the active debug session using the Terminate button. This will close the debugger and return CCS to the “CCS Edit Perspective” view.

29. Next, close the project by right-clicking on Lab5 in the Project Explorer window and select Close Project.

**End of Exercise**

**Note:** By default, the watchdog timer is enabled out of reset. Code in the file CodeStartBranch.asm has been configured to disable the watchdog. This can be important for large C code projects (ask your instructor if this has not already been explained). During this lab exercise, the watchdog was actually re-enabled (or disabled again) in the file Watchdog.c.
Analog-to-Digital Converter and Comparator

Introduction

This module explains the operation of the analog-to-digital converter and comparator. The ADC system consists of a 12-bit analog-to-digital converter with up to 16 analog input channels. The analog input channels have a full range analog input of 0 to 3.3 volts or VREFHI/VREFLO ratiometric. Two input analog multiplexers are available, each supporting up to 8 analog input channels. Each multiplexer has its own dedicated sample and hold circuit. Therefore, sequential, as well as simultaneous sampling is supported. The ADC system is start-of-conversion (SOC) based where each independent SOCx (where x = 0 to 15) register configures the trigger source that starts the conversion, the channel to convert, and the acquisition (sample) window size. Up to 16 results registers are used to store the conversion values. Conversion triggers can be performed by an external trigger pin, software, an ePWM or CPU timer interrupt event, or a generated ADCINT1/2 interrupt.

Module Objectives

- Understand the operation of the Analog-to-Digital converter (ADC) and Comparator
- Use the ADC to perform data acquisition
Module Topics

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Module Topics .................................................................................................................. 6-2

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Comparator ...................................................................................................................... 6-17
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Analog-to-Digital Converter

ADC Block and Functional Diagrams

The ADC module is based around a 12-bit converter. There are 16 input channels and 16 result registers. The SOC configuration registers select the trigger source, channel to convert, and the acquisition prescale window size. The triggers include software by selecting a bit, CPU timers 0, 1 and 2, EPWMA and EPWMB 1 through 8, and an external pin. Additionally, ADCINT 1 and 2 can be fed back for continuous conversions.

The ADC module can operate in sequential sampling mode or simultaneous sampling mode. In simultaneous sampling mode, the channel selected on the A multiplexer will be the same channel on the B multiplexer. The ADC interrupt logic can generate up to nine interrupts. The results for SOC 0 through 15 will appear in result registers 0 through 15.
ADC Triggering

Example – ADC Triggering

(sequential sampling)

Sample A2 → B3 → A7 when ePWM1 SOCB is generated and then generate ADCINT1:

Then after above, sample A0 → B0 → A5 continuously and generate ADCINT2:

The top example on this slide shows channels A2, B3, and A7 being converted with a trigger from EPWM1SO CB. After A7 is converted, ADCINT1 is generated.
The bottom examples extends this with channels A0, B0, and A5 being converted initially with a software trigger. After A5 is converted, ADCINT2 is generated, which is fed back as a trigger to start the process again.

The example on this slide shows channels A/B 0 through 7 being converted in simultaneous sampling mode, triggered initially by software. After channel A/B three is converted, ADCINT1 is generated. After channel A/B seven is converted, ADCINT2 is generated and fed back to start the process again. ADCINT1 and ADCINT2 are being used as ping-pong interrupts.
ADC Conversion Priority

**When multiple SOC flags are set at the same time – priority determines the order in which they are converted**

- Round Robin Priority (default)
  - No SOC has an inherent higher priority than another
  - Priority depends on the round robin pointer

- High Priority
  - High priority SOC will interrupt the round robin wheel after current conversion completes and insert itself as the next conversion
  - After its conversion completes, the round robin wheel will continue where it was interrupted

**Conversion Priority Functional Diagram**

- **SOC Priority**
  - Determines cutoff point for high priority and round robin mode

- **Round Robin Pointer**
  - Points to the last converted round robin SOCx and determines order of conversions
**Round Robin Priority Example**

SOC0 is highest RR priority

SOC7 trigger received

SOC7 is converted; RRPOINTER now points to SOC7; SOC8 is now highest RR priority

SOC2 & SOC12 triggers received simultaneously

SOC12 is converted; RRPOINTER points to SOC12; SOC13 is now highest RR priority

SOC2 is converted; RRPOINTER points to SOC2; SOC3 is now highest RR priority

**High Priority Example**

SOC0 is highest RR priority

SOC7 trigger received

SOC7 is converted; RRPOINTER points to SOC7; SOC8 is now highest RR priority

SOC2 & SOC12 triggers received simultaneously

SOC2 is converted; RRPOINTER stays pointing to SOC7

SOC12 is converted; RRPOINTER points to SOC12; SOC13 is now highest RR priority
ADC Clock and Timing

ADC Clocking Flow

ADC Timing – Sequential Sampling

Max Continuous Sampling:

\[
\text{45 MHz} \div \frac{13 \text{ cycles}}{1 \text{ sample}} = 3.46 \text{ MSPS}
\]

Note: Sampling window of 7 cycles is minimum and it can be larger
### ADC Timing – Simultaneous Sampling

- **Latch**: 2 Clocks
- **Sample**: 7 Clocks
- **Convert “A” Channel**: 13 Clocks
- **Write**: 2 Clocks
- **Convert “B” Channel**: 6 Clocks
- **Write**: 7 Clocks
- **Generate Early Interrupt “A” Channel**: 2 Clocks
- **Generate Early Interrupt “B” Channel**: 2 Clocks
- **Generate Late Interrupt “A” Channel & Generate Early Interrupt “B” Channel**: 2 Clocks
- **Start Sampling Next Channel**: 2 Clocks

---

#### Max Continuous Sampling:

\[
\text{Sampling Window} = \frac{26 \text{ cycles}}{2 \text{ sample}} = 3.46 \text{ MSPS}
\]

Note: Sampling window of 7 cycles is minimum and it can be larger

### ADC Converter Registers

**Analog-to-Digital Converter Registers**

*AdcRegs.register (lab file: Adc.c)*

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCCTL1</td>
<td>Control 1 Register</td>
</tr>
<tr>
<td>ADCCTL2</td>
<td>Control 2 Register</td>
</tr>
<tr>
<td>ADCSOCxCTL</td>
<td>SOC0 to SOC15 Control Registers</td>
</tr>
<tr>
<td>ADCINTSOCSELx</td>
<td>Interrupt SOC Selection 1 and 2 Registers</td>
</tr>
<tr>
<td>ADCSAMPLEMODE</td>
<td>Sampling Mode Register</td>
</tr>
<tr>
<td>ADCSOCTRLG1</td>
<td>SOC Flag 1 Register</td>
</tr>
<tr>
<td>ADCSOCFRC1</td>
<td>SOC Force 1 Register</td>
</tr>
<tr>
<td>ADCSOCOVF1</td>
<td>SOC Overflow 1 Register</td>
</tr>
<tr>
<td>ADCSOCOVFCLR1</td>
<td>SOC Overflow Clear 1 Register</td>
</tr>
<tr>
<td>INTSELxNy</td>
<td>Interrupt x and y Selection Registers</td>
</tr>
<tr>
<td>ADCINTFLG</td>
<td>Interrupt Flag Register</td>
</tr>
<tr>
<td>ADCINTFLGCLR</td>
<td>Interrupt Flag Clear Register</td>
</tr>
<tr>
<td>ADCINTOVF</td>
<td>Interrupt Overflow Register</td>
</tr>
<tr>
<td>ADCINTOVFCLR</td>
<td>Interrupt Overflow Clear Register</td>
</tr>
<tr>
<td>SOCPRICTL</td>
<td>SOC Priority Control Register</td>
</tr>
<tr>
<td>ADCREFTRIM</td>
<td>Reference Trim Register</td>
</tr>
<tr>
<td>ADCOFFTRIM</td>
<td>Offset Trim Register</td>
</tr>
<tr>
<td>ACREV</td>
<td>Revision Register – reserved</td>
</tr>
<tr>
<td>ADCRESULTx</td>
<td>ADC Result 0 to 15 Registers</td>
</tr>
</tbody>
</table>

Note: ADCRESULTx header file coding is AdcResult.ADCRESULTx (not in AdcRegs)
### ADC Control Register 1

**Upper Register:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ADC Module Reset</td>
</tr>
<tr>
<td>14</td>
<td>ADC Enable</td>
</tr>
<tr>
<td>13</td>
<td>ADC Busy</td>
</tr>
<tr>
<td>12-8</td>
<td>ADC Busy Channel</td>
</tr>
</tbody>
</table>

#### ADC Enable

- **0** = ADC disable
- **1** = ADC enable

#### ADC Busy Channel

When ADCBSY =

- **0** = last channel converted
- **1** = channel currently processing

<table>
<thead>
<tr>
<th>Value</th>
<th>Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>ADCINA0</td>
</tr>
<tr>
<td>01h</td>
<td>ADCINA1</td>
</tr>
<tr>
<td>02h</td>
<td>ADCINA2</td>
</tr>
<tr>
<td>03h</td>
<td>ADCINA3</td>
</tr>
<tr>
<td>04h</td>
<td>ADCINA4</td>
</tr>
<tr>
<td>05h</td>
<td>ADCINA5</td>
</tr>
<tr>
<td>06h</td>
<td>ADCINA6</td>
</tr>
<tr>
<td>07h</td>
<td>ADCINA7</td>
</tr>
<tr>
<td>08h</td>
<td>ADCINB0</td>
</tr>
<tr>
<td>09h</td>
<td>ADCINB1</td>
</tr>
<tr>
<td>0Ah</td>
<td>ADCINB2</td>
</tr>
<tr>
<td>0Bh</td>
<td>ADCINB3</td>
</tr>
<tr>
<td>0Ch</td>
<td>ADCINB4</td>
</tr>
<tr>
<td>0Dh</td>
<td>ADCINB5</td>
</tr>
<tr>
<td>0Eh</td>
<td>ADCINB6</td>
</tr>
<tr>
<td>0Fh</td>
<td>ADCINB7</td>
</tr>
</tbody>
</table>

### ADC Control Register 1

**Lower Register:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADC Power Down</td>
</tr>
<tr>
<td>6</td>
<td>ADC Reference Power Down</td>
</tr>
<tr>
<td>5</td>
<td>ADC Reference Select</td>
</tr>
<tr>
<td>4</td>
<td>Temperature Sensor Convert</td>
</tr>
<tr>
<td>3</td>
<td>ADCREFSEL</td>
</tr>
<tr>
<td>2</td>
<td>INTPULSEPOS</td>
</tr>
<tr>
<td>1</td>
<td>VREFLOCONV</td>
</tr>
<tr>
<td>0</td>
<td>VREFLOSEL</td>
</tr>
<tr>
<td></td>
<td>reserved</td>
</tr>
</tbody>
</table>

#### ADC Power Down

- **0** = analog circuitry powered down
- **1** = analog circuitry powered up

#### ADC Reference Power Down

- **0** = reference circuitry powered down
- **1** = reference circuitry powered up

#### ADC Reference Select

- **0** = internal
- **1** = external

#### Temperature Sensor Convert

- **0** = not connected
- **1** = connected (A5)

#### VREFLO Convert

- **0** = not connected
- **1** = connected (B5)

#### INT Pulse Generation Control

- **0** = beginning of conversion
- **1** = one cycle prior to result

#### ADC Bandgap Power Down

- **0** = bandgap circuitry powered down
- **1** = bandgap circuitry powered up
ADC Control Register 2
AdcRegs.ADCCTL2

ADC Overlap Bit
0 = overlap of sample and conversion is allowed
1 = overlap of sample is not allowed

ADC Clock Divider

<table>
<thead>
<tr>
<th>CLKDIV4EN</th>
<th>CLKDIV2EN</th>
<th>ADCCLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>0</td>
<td>SYSCLK</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>SYSCLK / 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>SYSCLK / 4</td>
</tr>
</tbody>
</table>

ADC SOC0 – SOC15 Control Registers
AdcRegs.ADCSOCxCTL

SOCx Trigger Source Select

<table>
<thead>
<tr>
<th>TRIGSEL</th>
<th>15 - 11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential S/M (SIMULEN=0)</td>
<td>Simultaneous S/M (SIMULEN=1)</td>
<td></td>
</tr>
<tr>
<td>0h = ADCINA0</td>
<td>0h = ADCINA0/B0</td>
<td></td>
</tr>
<tr>
<td>1h = ADCINA1</td>
<td>1h = ADCINA1/B1</td>
<td></td>
</tr>
<tr>
<td>2h = ADCINA2</td>
<td>2h = ADCINA2/B2</td>
<td></td>
</tr>
<tr>
<td>3h = ADCINA3</td>
<td>3h = ADCINA3/B3</td>
<td></td>
</tr>
<tr>
<td>4h = ADCINA4</td>
<td>4h = ADCINA4/B4</td>
<td></td>
</tr>
<tr>
<td>5h = ADCINA5</td>
<td>5h = ADCINA5/B5</td>
<td></td>
</tr>
<tr>
<td>6h = ADCINA6</td>
<td>6h = ADCINA6/B6</td>
<td></td>
</tr>
<tr>
<td>7h = ADCINA7</td>
<td>7h = ADCINA7/B7</td>
<td></td>
</tr>
</tbody>
</table>

SOCx Channel Select

<table>
<thead>
<tr>
<th>CHSEL</th>
<th>9 - 6</th>
<th>5 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h = ADCINB0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1h = ADCINB1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2h = ADCINB2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3h = ADCINB3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4h = ADCINB4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5h = ADCINB5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6h = ADCINB6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7h = ADCINB7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SOCx Acquisition Prescale (S/H window)

<table>
<thead>
<tr>
<th>ACQPS</th>
<th>10h - Fh</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h - 05h = invalid</td>
<td></td>
</tr>
<tr>
<td>06h = 7 cycles long</td>
<td></td>
</tr>
<tr>
<td>07h = 8 cycles long</td>
<td></td>
</tr>
<tr>
<td>08h = 9 cycles long</td>
<td></td>
</tr>
<tr>
<td>09h = 10 cycles long</td>
<td></td>
</tr>
<tr>
<td>3Fh = 64 cycles long</td>
<td></td>
</tr>
</tbody>
</table>

Sampling Window
00h – 05h = invalid
06h = 7 cycles long
07h = 8 cycles long
08h = 9 cycles long
09h = 10 cycles long
3Fh = 64 cycles long
**ADC Interrupt Trigger SOC Select**

**Registors 1 & 2**

AdcRegs.ADCINTSOCSELx

<table>
<thead>
<tr>
<th>ADCINTSOCSEL2</th>
<th>15 - 14</th>
<th>13 - 12</th>
<th>11 - 10</th>
<th>9 - 8</th>
<th>7 - 6</th>
<th>5 - 4</th>
<th>3 - 2</th>
<th>1 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOC15</td>
<td>SOC14</td>
<td>SOC13</td>
<td>SOC12</td>
<td>SOC11</td>
<td>SOC10</td>
<td>SOC9</td>
<td>SOC8</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ADCINTSOCSEL1</th>
<th>15 - 14</th>
<th>13 - 12</th>
<th>11 - 10</th>
<th>9 - 8</th>
<th>7 - 6</th>
<th>5 - 4</th>
<th>3 - 2</th>
<th>1 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOC7</td>
<td>SOC6</td>
<td>SOC5</td>
<td>SOC4</td>
<td>SOC3</td>
<td>SOC2</td>
<td>SOC1</td>
<td>SOC0</td>
<td></td>
</tr>
</tbody>
</table>

**SOCx ADC Interrupt Select**

- Selects which, if any, ADCINT triggers SOCx
- 00 = no ADCINT will trigger SOCx (TRIGSEL field determines SOCx trigger)
- 01 = ADCINT1 will trigger SOCx (TRIGSEL field ignored)
- 10 = ADCINT2 will trigger SOCx (TRIGSEL field ignored)
- 11 = invalid selection

**ADC Sample Mode Register**

AdcRegs.ADCSAMPLEMODE

<table>
<thead>
<tr>
<th>15 - 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
</tr>
<tr>
<td>7</td>
</tr>
</tbody>
</table>

**Simultaneous Sampling Enable**

- Couples SOCx and SOCx+1 in simultaneous sampling mode
- 0 = single sample mode for SOCx and SOCx+1
- 1 = simultaneous sample mode for SOCx and SOCx+1
### SOC Priority Control Register

**AdcRegs.SOCPRICRTL**

<table>
<thead>
<tr>
<th>15 - 11</th>
<th>10 - 5</th>
<th>4 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>RRPOINTER</td>
<td>SOCPRIORITY</td>
</tr>
</tbody>
</table>

**Round Robin Pointer**
Points to the last converted round robin SOCx and determines order of conversions

00h = SOC0 last converted, SOC1 highest priority
01h = SOC1 last converted, SOC2 highest priority
02h = SOC2 last converted, SOC3 highest priority
03h = SOC3 last converted, SOC4 highest priority
04h = SOC4 last converted, SOC5 highest priority
05h = SOC5 last converted, SOC6 highest priority
06h = SOC6 last converted, SOC7 highest priority
07h = SOC7 last converted, SOC8 highest priority
08h = SOC8 last converted, SOC9 highest priority
09h = SOC9 last converted, SOC10 highest priority
0Ah = SOC10 last converted, SOC11 highest priority
0Bh = SOC11 last converted, SOC12 highest priority
0Ch = SOC12 last converted, SOC13 highest priority
0Dh = SOC13 last converted, SOC14 highest priority
0Eh = SOC14 last converted, SOC15 highest priority
0Fh = SOC15 last converted, SOC0 highest priority
10h = reset value (no SOC has been converted)
11h - 15h = invalid selection

00h = round robin mode for all channels
01h = SOC0 high priority, SOC1-15 round robin
02h = SOC0-1 high priority, SOC2-15 round robin
03h = SOC0-2 high priority, SOC3-15 round robin
04h = SOC0-3 high priority, SOC4-15 round robin
05h = SOC0-4 high priority, SOC5-15 round robin
06h = SOC0-5 high priority, SOC6-15 round robin
07h = SOC0-6 high priority, SOC7-15 round robin
08h = SOC0-7 high priority, SOC8-15 round robin
09h = SOC0-8 high priority, SOC9-15 round robin
0Ah = SOC0-9 high priority, SOC10-15 round robin
0Bh = SOC0-10 high priority, SOC11-15 round robin
0Ch = SOC0-11 high priority, SOC12-15 round robin
0Dh = SOC0-12 high priority, SOC13-15 round robin
0Eh = SOC0-13 high priority, SOC14-15 round robin
0Fh = SOC0-14 high priority, SOC15 round robin
10h = all SOCs high priority (arbitrated by SOC #)
11h - 15h = invalid selection

### Interrupt Select x and y Register

**AdcRegs.INTSELxNy**

Where x/y = 1/2, 3/4, 5/6, 7/8, 9/10 and 10 is reserved

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12 - 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>INTyCONT</td>
<td>INTyE</td>
<td>INTySEL</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4 - 0</td>
</tr>
<tr>
<td>reserved</td>
<td>INTxCONT</td>
<td>INTxE</td>
<td>INTxSEL</td>
</tr>
</tbody>
</table>

**ADCINTx/y Continuous Mode Enable**
0 = one-shot pulse generated (until flag cleared by user)
1 = pulse generated for each EOC

**ADCINTx/y Interrupt Enable**
0 = disable
1 = enable

**ADCINTx/y EOC Source Select**
00h = EOC0 is trigger for ADCINTx/y
01h = EOC1 is trigger for ADCINTx/y
02h = EOC2 is trigger for ADCINTx/y
03h = EOC3 is trigger for ADCINTx/y
04h = EOC4 is trigger for ADCINTx/y
05h = EOC5 is trigger for ADCINTx/y
06h = EOC6 is trigger for ADCINTx/y
07h = EOC7 is trigger for ADCINTx/y
08h = EOC8 is trigger for ADCINTx/y
09h = EOC9 is trigger for ADCINTx/y
0Ah = EOC10 is trigger for ADCINTx/y
0Bh = EOC11 is trigger for ADCINTx/y
0Ch = EOC12 is trigger for ADCINTx/y
0Dh = EOC13 is trigger for ADCINTx/y
0 Eh = EOC14 is trigger for ADCINTx/y
0Fh = EOC15 is trigger for ADCINTx/y
10h = invalid value
Analog-to-Digital Converter

ADC Conversion Result Registers

AdcResult.ADCRESULTx, x = 0 - 15

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>Digital Result</th>
<th>AdcResult. ADCRESULTx</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>FFFh</td>
<td>0000</td>
</tr>
<tr>
<td>1.65</td>
<td>7FFh</td>
<td>0000</td>
</tr>
<tr>
<td>0.00081</td>
<td>1h</td>
<td>0000</td>
</tr>
<tr>
<td>0</td>
<td>0h</td>
<td>0000</td>
</tr>
</tbody>
</table>

- Sequential Sampling Mode (SIMULENx = 0)
  - After ADC completes a conversion of an SOCx, the digital result is placed in the corresponding ADCRESULTx register
- Simultaneous Sampling Mode (SIMULENx = 1)
  - After ADC completes a conversion of a channel pair, the digital results are found in the corresponding ADCRESULTx and ADCRESULTx+1 registers

Signed Input Voltages

How Can We Handle Signed Input Voltages?

Example: \(-1.65\) V \(\leq V_{\text{in}} \leq +1.65\) V

1) Add 1.65 volts to the analog input

2) Subtract “1.65” from the digital result

```c
#include "F2806x_Device.h"
#define offset 0x07FF
void main(void)
{
  int16 value; // signed

  value = AdcResult.ADCRESULT0 - offset;
}
```
ADC Calibration and Reference

**Built-In ADC Calibration**
- TI reserved OTP contains device specific calibration data for the ADC and internal oscillators
- The Boot ROM contains a Device_cal() routine that copies the calibration data to their respective registers
- Device_cal() must be run to meet the ADC and oscillator specs in the datasheet
  - The Bootloader automatically calls Device_cal() such that no action is normally required by the user
  - If the Bootloader is bypassed (e.g., during development) Device_cal() should be called by the application:

```c
#define Device_cal (void (*)(void))0x3D7C80
void main(void)
{
    (*Device_cal)();       // call Device_cal()
}
```
- A GEL function using CCS is also available as part of the Peripheral Register Header Files to accomplish this

**Manual ADC Calibration**
- If the offset and gain errors in the datasheet* are unacceptable for your application, or you want to also compensate for board level errors (e.g., sensor or amplifier offset), you can manually calibrate
  - **Offset error**
    - Compensated in analog with the ADCOFFTRIM register
    - No reduction in full-scale range
    - Configure input B5 to VREFLO, ADCOFFTRIM to maximum error, and take a reading
    - Re-adjust ADCOFFTRIM to make result zero
  - **Gain error**
    - Compensated in software
    - Some loss in full-scale range
    - Requires use of a second ADC input pin and an upper-range reference voltage on that pin; see “TMS320280x and TMS320F2801x ADC Calibration” appnote #SPRAAD8 for more information
- **Tip:** To minimize mux-to-mux variation effects, put your most critical signals on a single mux and use that mux for calibration inputs

* +/-15 LSB offset, +/-30 LSB gain. See device datasheet for exact specifications
The internal reference has temperature stability of ~50 PPM/°C*

The internal reference (default) will convert an applied input voltage to a fixed scale of 0 to 3.3 V range

If this is not sufficient for your application, there is the option to use an external reference*

External reference will scale an input voltage range from VREFLO to VREFHI (ratiometric)

The reference value changes the 0 - 3.3 V full-scale range of the ADC

The ADCREFSEL in ADCCTL1 controls the reference choice

<table>
<thead>
<tr>
<th>15 - 5</th>
<th>4</th>
<th>3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>ADCREFSEL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ADC Reference Selection
0 = internal (default)
1 = external VREFHI/VREFLO pins used for reference generation

* See device datasheet for exact specifications and ADC reference hardware connections
This device has three analog comparators that share the input pins with the analog-to-digital converter module. If neither the ADC or comparator input pins are needed, the input pins can be used as analog I/O pins. As you can see, one of the inputs to the comparator comes directly from the input pin, and the other input can be taken from the input pin or the 10-bit digital-to-analog converter. The output of the comparator is fed into the ePWM digital compare sub-module.
Comparator

Comparator Block Diagram

DAC Reference

\[ V = \frac{\text{DACVAL} \times (V_{\text{DDA}} - V_{\text{SSA}})}{1023} \]

Comparator Truth Table

<table>
<thead>
<tr>
<th>Voltages</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage A &lt; Voltage B</td>
<td>0</td>
</tr>
<tr>
<td>Voltage A &gt; Voltage B</td>
<td>1</td>
</tr>
</tbody>
</table>

Comparator Registers

**AdcRegs.COMPCTL – Compare Control Register**

- **SYNCSEL**: Synchronization Select
- **QUALSEL**: Output before being feed to ETPWM/GPIO blocks
- **CMPINV**: Qualification Period
- **COMPSOURCE**: Comparator Source
- **COMPDACE**: Comparator/DAC Enable

**AdcRegs.DACCTL – DAC Control Register**

- **FREE:SOFT**: DAC source (DACVAL or RAMP Generator) and RAMP source sync select
- **RAMPSOURCE**: DAC VAL
- **DACSOURCE**: DAC source

**AdcRegs.DACVAL – DAC Value Register**

- **DACVAL**: Scales output of DAC from 0 – 1023
- **Value**: 0 – 3FFh

**AdcRegs.COMPSTS – Compare Output Status Register**

- **COMPSTS**: Logical latched value of the comparator
Lab 6: Analog-to-Digital Converter

- **Objective**

The objective of this lab is to become familiar with the programming and operation of the on-chip analog-to-digital converter. The MCU will be setup to sample a single ADC input channel at a prescribed sampling rate and store the conversion result in a circular memory buffer.

Recall that there are three basic ways to initiate an ADC start of conversion (SOC):

1. **Using software**
   a. SOCx bit (where x = 0 to 15) in the ADC SOC Force 1 Register (ADCSOCFRC1) causes a software initiated conversion

2. **Automatically triggered on user selectable conditions**
   a. CPU Timer 0/1/2 interrupt
   b. ePWMxSOCA / ePWMxSOCB (where x = 1 to 7)
      - ePWM underflow (CTR = 0)
      - ePWM period match (CTR = PRD)
      - ePWM underflow or period match (CTR = 0 or PRD)
      - ePWM compare match (CTRU/D = CMPA/B)
   c. ADC interrupt ADCINT1 or ADCINT2
      - triggers SOCx (where x = 0 to 15) selected by the ADC Interrupt Trigger SOC Select1/2 Register (ADCSOCSEL1/2)

3. **Externally triggered using a pin**
   a. ADCSOC pin (GPIO/XINT2_ADCSOC)

One or more of these methods may be applicable to a particular application. In this lab, we will be using the ADC for data acquisition. Therefore, one of the ePWMs (ePWM2) will be configured to automatically trigger the SOCA signal at the desired sampling rate (ePWM period match CTR = PRD SOC method 2b above). The ADC end-of-conversion interrupt will be used to prompt the CPU to copy the results of the ADC conversion into a results buffer in memory.
This buffer pointer will be managed in a circular fashion, such that new conversion results will continuously overwrite older conversion results in the buffer. In order to generate an interesting input signal, the code also alternately toggles a GPIO pin (GPIO18) high and low in the ADC interrupt service routine. The ADC ISR will also toggle LED LD3 on the controlCARD as a visual indication that the ISR is running. This pin will be connected to the ADC input pin, and sampled. After taking some data, Code Composer Studio will be used to plot the results. A flow chart of the code is shown in the following slide.

### Lab 6: Code Flow Diagram

**Start**

- **General Initialization**
  - PLL and clocks
  - watchdog configure
  - GPIO setup
  - PIE initialization

- **ADC Initialization**
  - convert channel A0 on ePWM2 period match
  - send interrupt on EOC to trigger ADC ISR
  - setup a results buffer in memory

- **ePWM2 Initialization**
  - clear counter
  - set period register
  - set to trigger ADC on period match
  - set the clock prescaler
  - enable the timer

**Main Loop**

```c
while(1) {
    // Main Loop Code
}
```

**ADC ISR**

- read the ADC result
- write to result buffer
- adjust the buffer pointer
- toggle the GPIO pin
- return from interrupt

**return**

### Notes

- Program performs conversion on ADC channel A0 (ADCINA0 pin)
- ADC conversion is set at a 50 kHz sampling rate
- ePWM2 is triggering the ADC on period match using SOCA trigger
- Data is continuously stored in a circular buffer
- GPIO18 pin is also toggled in the ADC ISR
- ADC ISR will also toggle the controlCARD LED LD3 as a visual indication that it is running
Procedure

Open the Project

1. A project named Lab6 has been created for this lab. Open the project by clicking on Project ➔ Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab6\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:

- Adc.c
- CodeStartBranch.asm
- DefaultIsr_6.c
- DelayUs.asm
- EPwm_6.c
- F2806x_DefaultIsr.h
- F2806x_GlobalVariableDefs.c
- F2806x_Headers_nonBIOS.cmd
- Gpio.c
- Lab.h
- Lab_5_6_7.cmd
- Main_6.c
- PieCtrl.c
- PieVect.c
- SysCtrl.c
- Watchdog.c

Setup ADC Initialization and Enable Core/PIE Interrupts

2. In Main_6.c add code to call InitAdc() and InitEPwm() functions. The InitEPwm() function is used to configure ePWM2 to trigger the ADC at a 50 kHz rate. Details about the ePWM and control peripherals will be discussed in the next module.

3. Edit Adc.c to configure SOC0 in the ADC as follows:
   - SOC0 converts input ADCINA0 in single-sample mode
   - SOC0 has a 7 cycle acquisition window
   - SOC0 is triggered by the ePWM2 SOCA
   - SOC0 triggers ADCINT1 on end-of-conversion
   - All SOCs run round-robin

4. Using the “PIE Interrupt Assignment Table” find the location for the ADC interrupt “ADCINT1” (high-priority) and fill in the following information:

   PIE group #:__________ # within group:__________

   This information will be used in the next step.

5. Modify the end of Adc.c to do the following:
   - Enable the “ADCINT1” interrupt in the PIE (Hint: use the PieCtrlRegs structure)
   - Enable the appropriate core interrupt in the IER register

6. Open and inspect DefaultIsr_6.c. This file contains the ADC interrupt service routine. Save your work and close the modified files.

Build and Load

7. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.
8. Click the “Debug” button (green bug). The “Debug Perspective” view should open, the program will load automatically, and you should now be at the start of main(). If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to EMU_BOOT_SARAM using the Scripts menu.

Run the Code

9. In Main_6.c place the cursor in the “main loop” section, right click on the mouse key and select Run To Line.

10. Open a memory browser to view some of the contents of the ADC results buffer. The address label for the ADC results buffer is AdcBuf (type &AdcBuf) in the “Data” memory page. Select GO to view the contents of the ADC result buffer.

Note: Exercise care when connecting any wires, as the power to the USB Docking Station is on, and we do not want to damage the controlCARD!

11. Using a connector wire provided, connect the ADCINA0 (pin # ADC-A0) to “GND” (pin # GND) on the Docking Station. Then run the code again, and halt it after a few seconds. Verify that the ADC results buffer contains the expected value of ~0x0000. Note that you may not get exactly 0x0000 if the device you are using has positive offset error.

12. Adjust the connector wire to connect the ADCINA0 (pin # ADC-A0) to “+3.3V” (pin # GPIO-20) on the Docking Station. (Note: pin # GPIO-20 has been set to “1” in Gpio.c). Then run the code again, and halt it after a few seconds. Verify that the ADC results buffer contains the expected value of ~0x0FFF. Note that you may not get exactly 0x0FFF if the device you are using has negative offset error.

13. Adjust the connector wire to connect the ADCINA0 (pin # ADC-A0) to GPIO18 (pin # GPIO-18) on the Docking Station. Then run the code again, and halt it after a few seconds. Examine the contents of the ADC results buffer (the contents should be alternating ~0x0000 and ~0x0FFF values). Are the contents what you expected?

14. Open and setup a graph to plot a 50-point window of the ADC results buffer. Click: Tools → Graph → Single Time and set the following values:

<table>
<thead>
<tr>
<th>Acquisition Buffer Size</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Data Type</td>
<td>16-bit unsigned integer</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address</td>
<td>AdcBuf</td>
</tr>
<tr>
<td>Display Data Size</td>
<td>50</td>
</tr>
<tr>
<td>Time Display Unit</td>
<td>µs</td>
</tr>
</tbody>
</table>

Select OK to save the graph options.
15. Recall that the code toggled the GPIO18 pin alternately high and low. (Also, the ADC ISR is toggling the LED LD3 on the controlCARD as a visual indication that the ISR is running). If you had an oscilloscope available to display GPIO18, you would expect to see a square-wave. Why does Code Composer Studio plot resemble a triangle wave? What is the signal processing term for what is happening here?

16. Recall that the program toggled the GPIO18 pin at a 50 kHz rate. Therefore, a complete cycle (toggle high, then toggle low) occurs at half this rate, or 25 kHz. We therefore expect the period of the waveform to be 40 µs. Confirm this by measuring the period of the triangle wave using the “measurement marker mode” graph feature. In the graph window toolbar, left-click on the ruler icon with the red arrow. Note when you hover your mouse over the icon, it will show “Toggle Measurement Marker Mode”. Move the mouse to the first measurement position and left-click. Again, left-click on the Toggle Measurement Marker Mode icon. Move the mouse to the second measurement position and left-click. The graph will automatically calculate the difference between the two values taken over a complete waveform period. When done, clear the measurement points by right-clicking on the graph and select Remove All Measurement Marks (or Ctrl+Alt+M).

Using Real-time Emulation

Real-time emulation is a special emulation feature that offers two valuable capabilities:

A. Windows within Code Composer Studio can be updated at up to a 10 Hz rate while the MCU is running. This not only allows graphs and watch windows to update, but also allows the user to change values in watch or memory windows, and have those changes affect the MCU behavior. This is very useful when tuning control law parameters on-the-fly, for example.

B. It allows the user to halt the MCU and step through foreground tasks, while specified interrupts continue to get serviced in the background. This is useful when debugging portions of a realtime system (e.g., serial port receive code) while keeping critical parts of your system operating (e.g., commutation and current loops in motor control).

We will only be utilizing capability “A” above during the workshop. Capability “B” is a particularly advanced feature, and will not be covered in the workshop.

17. The memory and graph windows displaying AdcBuf should still be open. The connector wire between ADCINA0 (pin # ADC-A0) and GPIO18 (pin # GPIO-18) should still be connected. In real-time mode, we will have our window continuously refresh at the default rate. To view the refresh rate click:

Window → Preferences...

and in the section on the left select the “Code Composer Studio” category. Click the plus sign (+) to the left of “Code Composer Studio” and select “Debug”. In the section on the right notice the default setting:

- “Continuous refresh interval (milliseconds)” = 500

Click OK.
Note: Decreasing the “Continuous refresh interval” causes all enabled continuous refresh windows to refresh at a faster rate. This can be problematic when a large number of windows are enabled, as bandwidth over the emulation link is limited. Updating too many windows can cause the refresh frequency to bog down. In this case you can just selectively enable continuous refresh for the individual windows of interest.

18. Next we need to enable the graph window for continuous refresh. Select the “Single Time” graph. In the graph window toolbar, left-click on the yellow icon with the arrows rotating in a circle over a pause sign. Note when you hover your mouse over the icon, it will show “Enable Continuous Refresh”. This will allow the graph to continuously refresh in real-time while the program is running.

19. Enable the Memory Browser for continuous refresh using the same procedure as the previous step.

20. Code Composer Studio includes Scripts that are functions which automate entering and exiting real-time mode. Four functions are available:
   - Run_Realtime_with_Reset (reset CPU, enter real-time mode, run CPU)
   - Run_Realtime_with_Restart (restart CPU, enter real-time mode, run CPU)
   - Full_Halt (exit real-time mode, halt CPU)
   - Full_Halt_with_Reset (exit real-time mode, halt CPU, reset CPU)

   These Script functions are executed by clicking:
   Scripts → Realtime Emulation Control → Function

   In the remaining lab exercises we will be using the first and third above Script functions to run and halt the code in real-time mode.

21. Run the code and watch the windows update in real-time mode. Click:
   Scripts → Realtime Emulation Control → Run_Realtime_with_Reset

22. Carefully remove and replace the connector wire from GPIO18. Are the values updating in the Memory Browser and Single Time graph as expected?

23. Fully halt the CPU in real-time mode. Click:
   Scripts → Realtime Emulation Control → Full_Halt

24. So far, we have seen data flowing from the MCU to the debugger in realtime. In this step, we will flow data from the debugger to the MCU.
   - Open and inspect Main_6.c. Notice that the global variable DEBUG_TOGGLE is used to control the toggling of the GPIO18 pin. This is the pin being read with the ADC.
   - Highlight DEBUG_TOGGLE with the mouse, right click and select “Add Watch Expression...” and then select OK. The global variable DEBUG_TOGGLE should now be in the “Expressions” window with a value of “1”.
   - Enable the “Expressions” window for continuous refresh
• Run the code in real-time mode and change the value to “0”. Are the results shown in the memory and graph window as expected? Change the value back to “1”. As you can see, we are modifying data memory contents while the processor is running in real-time (i.e., we are not halting the MCU nor interfering with its operation in any way)! When done, fully halt the CPU.

**Terminate Debug Session and Close Project**

25. Terminate the active debug session using the Terminate button. This will close the debugger and return CCS to the “CCS Edit Perspective” view.

26. Next, close the project by right-clicking on Lab6 in the Project Explorer window and select Close Project.

**Optional Exercise**

If you finish early, you might want to experiment with the code by observing the effects of changing the OFFTRIM value. Open a watch window to the AdcRegs.ADCOFFTRIM register and change the OFFTRIM value. If you did not get 0x0000 in step 11, you can calibrate out the offset of your device. If you did get 0x0000, you can determine if you actually had zero offset, or if the offset error of your device was negative. (If you do not have time to work on this optional exercise, you may want to try this after the class).

**End of Exercise**
Introduction

This module explains how to generate PWM waveforms using the ePWM unit. Also, the eCAP unit, and eQEP unit will be discussed.

Module Objectives

- Pulse Width Modulation (PWM) review
- Generate a PWM waveform with the Pulse Width Modulator Module (ePWM)
- Use the Capture Module (eCAP) to measure the width of a waveform
- Explain the function of Quadrature Encoder Pulse Module (eQEP)

Note: Different numbers of ePWM, eCAP, and eQEP modules are available on F2806x devices. See the device datasheet for more information.
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Module Topics...................................................................................................................................7-2

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ePWM .............................................................................................................................................7-4

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ePWM Compare Sub-Module .........................................................................................................7-7

ePWM Action Qualifier Sub-Module .............................................................................................7-11

Asymmetric and Symmetric Waveform Generation using the ePWM ........................................7-13

PWM Computation Example...........................................................................................................7-19

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PWM Review

What is Pulse Width Modulation?

- PWM is a scheme to represent a signal as a sequence of pulses
  - fixed carrier frequency
  - fixed pulse amplitude
  - pulse width proportional to instantaneous signal amplitude
- PWM energy ≈ original signal energy

Pulse width modulation (PWM) is a method for representing an analog signal with a digital approximation. The PWM signal consists of a sequence of variable width, constant amplitude pulses which contain the same total energy as the original analog signal. This property is valuable in digital motor control as sinusoidal current (energy) can be delivered to the motor using PWM signals applied to the power converter. Although energy is input to the motor in discrete packets, the mechanical inertia of the rotor acts as a smoothing filter. Dynamic motor motion is therefore similar to having applied the sinusoidal currents directly.
Why use PWM with Power Switching Devices?

- Desired output currents or voltages are known
- Power switching devices are transistors
  - Difficult to control in proportional region
  - Easy to control in saturated region
- PWM is a digital signal $\Rightarrow$ easy for MCU to output

Power-switching devices are difficult to control in the proportional region but are easy to control in the saturation and cutoff region. Since PWM is a digital signal and easy for microcontrollers to generate, it is ideal for use with power-switching devices.
An ePWM module can be synchronized with adjacent ePWM modules. The generated PWM waveforms are available as outputs on the GPIO pins. Additionally, the EPWM module can generate ADC starter conversion signals and generate interrupts to the PIE block. External trip zone signals can trip the output and generate interrupts, too. The outputs of the comparators are used as inputs to the digital compare sub-module. Next, we will look at the internal details of the ePWM module.
The ePWM, or enhanced PWM block diagram, consists of a series of sub-modules. In this section, we will learn about the operation and details of each sub-module.
In the time-base sub-module, the clock prescaler divides down the device core system clock and clocks the 16-bit time-base counter. The time-base counter is used to generate asymmetrical and symmetrical waveforms using three different count modes: count-up mode, countdown mode, and count up and down mode. A period register is used to control the maximum count value. Additionally, the time-base counter has the capability to be synchronized and phase-shifted with other ePWM units.
The upper two figures show the time-base counter in the count-up mode and countdown mode. These modes are used to generate asymmetrical waveforms. The lower figure shows the time-base counter in the count up and down mode. This mode is used to generate symmetrical waveforms.
If needed, an ePWM module can be synchronized with adjacent ePWM modules. Synchronization is based on a synch-in signal, time-base counter equals zero, or time-base counter equals compare B register. Additionally, the waveform can be phase-shifted.

### ePWM Time-Base Sub-Module Registers

*(lab file: EPwm.c)*

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBCTL</td>
<td>Time-Base Control</td>
<td>EPwmXRegs.TBCTL.all =</td>
</tr>
<tr>
<td>TBSTS</td>
<td>Time-Base Status</td>
<td>EPwmXRegs.TBSTS.all =</td>
</tr>
<tr>
<td>TBPHS</td>
<td>Time-Base Phase</td>
<td>EPwmXRegs.TBPHS =</td>
</tr>
<tr>
<td>TBCTR</td>
<td>Time-Base Counter</td>
<td>EPwmXRegs.TBCTR =</td>
</tr>
<tr>
<td>TBPRD</td>
<td>Time-Base Period</td>
<td>EPwmXRegs.TBPRD =</td>
</tr>
</tbody>
</table>
### Upper Register:

**Phase Direction**
- **0** = count down after sync
- **1** = count up after sync

**Emulation Halt Behavior**
- **00** = stop after next CTR inc/dec
- **01** = stop when:  
  - Up Mode; CTR = PRD
  - Down Mode; CTR = 0
  - Up/Down Mode; CTR = 0
- **1x** = free run (do not stop)

**TB Clock Prescale**
- **000** = /1 (default)
- **001** = /2
- **010** = /4
- **011** = /8
- **100** = /16
- **101** = /32
- **110** = /64
- **111** = /128

**High Speed TB Clock Prescale**
- **000** = /1
- **001** = /2 (default)
- **010** = /4
- **011** = /6
- **100** = /8
- **101** = /10
- **110** = /12
- **111** = /14

(HSPCLKDIV is for legacy compatibility)

### Lower Register:

**Software Force Sync Pulse**
- **0** = no action
- **1** = force one-time sync

**Counter Mode**
- **00** = count up
- **01** = count down
- **10** = count up and down
- **11** = stop – freeze (default)

**Sync Output Select**
(source of EPWMxSYNC0 signal)
- **00** = EPWMxSYNCI
- **01** = CTR = 0
- **10** = CTR = CMPB
- **11** = disable SyncOut

**Period Shadow Load**
- **0** = load on CTR = 0
- **1** = load immediately

**Phase Reg. Enable**
- **0** = disable
- **1** = CTR = TBPHS on EPWMxSYNCI signal
The compare sub-module uses two compare registers to detect time-base count matches. These compare match events are fed into the action qualifier sub-module. Notice that the output of this block feeds two signals into the action qualifier.

**ePWM Compare Event Waveforms**

- **Count Up Mode**
  - Asymmetrical Waveform

- **Count Down Mode**
  - Asymmetrical Waveform

- **Count Up and Down Mode**
  - Symmetrical Waveform

---

**ePWM Compare Sub-Module**

- **Clock Prescaler**
- **16-Bit Time-Base Counter**
- **Compare Logic**
- **Action Qualifier**
- **Dead Band**
- **Period Register**
- **Chopper**
- **Trip Zone**
- **PWM**
- **Digital Compare**
- **Shadowed Compare Register**
- **Shadowed Compare Register**
- **EPWMxA**
- **EPWMxB**
- **EPWMxSYNCI**
- **EPWMxSYNCO**
- **TBCLK**
- **TBPRD**
- **CMPA**
- **CMPB**
- **COMPxOUT**
The ePWM Compare Event Waveforms figures shows the compare matches that are fed into the action qualifier. Notice that with the count up and countdown mode, there are matches on the up-count and down-count.

### ePWM Compare Sub-Module Registers
*(lab file: EPwm.c)*

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPCTL</td>
<td>Compare Control</td>
<td><code>EPwmRegs.CMPCTL.all =</code></td>
</tr>
<tr>
<td>CMPA</td>
<td>Compare A</td>
<td><code>EPwmRegs.CMPA =</code></td>
</tr>
<tr>
<td>CMPB</td>
<td>Compare B</td>
<td><code>EPwmRegs.CMPB =</code></td>
</tr>
</tbody>
</table>

### ePWM Compare Control Register
`EPwmRegs.CMPCTL`

**CMPA and CMPB Shadow Full Flag**
*bit automatically clears on load*
- 0 = shadow not full
- 1 = shadow full

- **SHDWBFULL**
  - 15 - 10: reserved
  - 9: SHDWBFULL
  - 8: SHDWFULL
  - 7: reserved

**CMPA and CMPB Operating Mode**
- 0 = shadow mode; double buffer w/ shadow register
- 1 = immediate mode; shadow register not used

**CMPA and CMPB Shadow Load Mode**
- 00 = load on CTR = 0
- 01 = load on CTR = PRD
- 10 = load on CTR = 0 or PRD
- 11 = freeze (no load possible)

<table>
<thead>
<tr>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3 - 2</th>
<th>1 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SHDBMODE</strong></td>
<td>reserved</td>
<td><strong>SHDWAMODE</strong></td>
<td><strong>LOADBMODE</strong></td>
<td><strong>LOADAMODE</strong></td>
</tr>
</tbody>
</table>
ePWM Action Qualifier Sub-Module

The action qualifier sub-module uses the inputs from the compare logic and time-base counter to generate various actions on the output pins. These first few modules are the main components used to generate a basic PWM waveform.

**ePWM Action Qualifier Actions**

For EPWMA and EPWMB

<table>
<thead>
<tr>
<th>S/W Force</th>
<th>Time-Base Counter equals:</th>
<th>EPWM Output Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Zero CMPA CMPB TBPRD</td>
<td></td>
</tr>
<tr>
<td>SW X</td>
<td>Z X CA X CB X P X</td>
<td>Do Nothing</td>
</tr>
<tr>
<td>SW ↓</td>
<td>Z CA CB P</td>
<td>Clear Low</td>
</tr>
<tr>
<td>SW ↑</td>
<td>Z CA CB P</td>
<td>Set High</td>
</tr>
<tr>
<td>SW T</td>
<td>Z CA CB P</td>
<td>Toggle</td>
</tr>
</tbody>
</table>

The diagram and table provide a visual and tabular representation of the various actions that can be taken by the ePWM action qualifier sub-module, showing how different conditions on the time-base counter and compare registers result in specific actions on the output pins.
This table shows the various action qualifier compare-match options for when the time-base counter equals zero, compare A match, compare B match, and period match. Based on the selected match option, the output pins can be configured to do nothing, clear low, set high, or toggle. Also, the output pins can be forced to any action using software.

The next few figures show how the action qualifier uses the compare matches to modulate the output pins. Notice that the output pins for EPWMA and EPWMB are completely independent. Here, on the EPWMA output, the waveform will be set high on zero match and clear low on compare A match. On the EPWMB output, the waveform will be set high on zero match and clear low on compare B match.
This figure has the EPWMA output set high on compare A match and clear low on compare B match, while the EPWMB output is configured to toggle on zero match.

Here you can see that we can have different output actions on the up-count and down-count using a single compare register. So, for the EPWMA and EPWMB outputs, we are setting high on the
compare A and B up-count matches and clearing low on the compare A and B down-down matches.

And finally, again using different output actions on the up-count and down-count, we have the EPWMA output set high on the compare A up-count match and clear low on the compare B down-count match. The EPWMB output will clear low on zero match and set high on period match.
ePWM Action Qualifier Sub-Module
Registers
(lab file: EPwm.c)

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>AQCTLA</td>
<td>AQ Control Output A</td>
<td>EPwm__Regs.AQCTLA.all =</td>
</tr>
<tr>
<td>AQCTLB</td>
<td>AQ Control Output B</td>
<td>EPwm__Regs.AQCTLB.all =</td>
</tr>
<tr>
<td>AQSFRC</td>
<td>AQ S/W Force</td>
<td>EPwm__Regs.AQSFRC.all =</td>
</tr>
<tr>
<td>AQCSFRC</td>
<td>AQ Cont. S/W Force</td>
<td>EPwm__Regs.AQCSFRC.all =</td>
</tr>
</tbody>
</table>

**ePWM Action Qualifier Control Register**

EPwm\_\_Regs.AQCTLy \( y = A \) or B

<table>
<thead>
<tr>
<th>Action when CTR = CMPB on UP Count</th>
<th>Action when CTR = CMPA on UP Count</th>
<th>Action when CTR = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 - 12</td>
<td>9 - 8</td>
<td>1 - 0</td>
</tr>
<tr>
<td>11 - 10</td>
<td>7 - 6</td>
<td></td>
</tr>
<tr>
<td>reserved</td>
<td>CBD</td>
<td>ZRO</td>
</tr>
<tr>
<td></td>
<td>CBU</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CAD</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CAU</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PRD</td>
<td></td>
</tr>
</tbody>
</table>

Action when CTR = CMPB on DOWN Count
Action when CTR = CMPA on DOWN Count
Action when CTR = PRD

00 = do nothing (action disabled)
01 = clear (low)
10 = set (high)
11 = toggle (low → high; high → low)
### ePWM Action Qualifier S/W Force Register

**EPwmRegs.AQSFRC**

#### One-Time S/W Force on Output B / A
- 0 = no action
- 1 = single s/w force event

#### AQSFRC Shadow Reload Options
- 00 = load on event CTR = 0
- 01 = load on event CTR = PRD
- 10 = load on event CTR = 0 or CTR = PRD
- 11 = load immediately (from active reg.)

#### Action on One-Time S/W Force B / A
- 00 = do nothing (action disabled)
- 01 = clear (low)
- 10 = set (high)
- 11 = toggle (low → high; high → low)

---

### ePWM Action Qualifier Continuous S/W Force Register

**EPwmRegs.AQCSFRC**

#### Continuous S/W Force on Output B / A
- 00 = forcing disabled
- 01 = force continuous low on output
- 10 = force continuous high on output
- 11 = forcing disabled
Asymmetric and Symmetric Waveform Generation using the ePWM

PWM switching frequency:

The PWM carrier frequency is determined by the value contained in the time-base period register, and the frequency of the clocking signal. The value needed in the period register is:

\[
\text{Asymmetric PWM: } \text{period register} = \left(\frac{\text{switching period}}{\text{timer period}}\right) - 1
\]

\[
\text{Symmetric PWM: } \text{period register} = \frac{\text{switching period}}{2(\text{timer period})}
\]

Notice that in the symmetric case, the period value is half that of the asymmetric case. This is because for up/down counting, the actual timer period is twice that specified in the period register (i.e. the timer counts up to the period register value, and then counts back down).

PWM resolution:

The PWM compare function resolution can be computed once the period register value is determined. The largest power of 2 is determined that is less than (or close to) the period value. As an example, if asymmetric was 1000, and symmetric was 500, then:

\[
\text{Asymmetric PWM: approx. 10 bit resolution since } 2^{10} = 1024 \approx 1000
\]

\[
\text{Symmetric PWM: approx. 9 bit resolution since } 2^9 = 512 \approx 500
\]

PWM duty cycle:

Duty cycle calculations are simple provided one remembers that the PWM signal is initially inactive during any particular timer period, and becomes active after the (first) compare match occurs. The timer compare register should be loaded with the value as follows:

\[
\text{Asymmetric PWM: } \text{TxCMPR} = (100\% - \text{duty cycle}) \times \text{TxPR}
\]

\[
\text{Symmetric PWM: } \text{TxCMPR} = (100\% - \text{duty cycle}) \times \text{TxPR}
\]

Note that for symmetric PWM, the desired duty cycle is only achieved if the compare registers contain the computed value for both the up-count compare and down-count compare portions of the time-base period.
PWM Computation Example

**Symmetric PWM Computation Example**

- Determine TBPRD and CMPA for 90 kHz, 25% duty symmetric PWM from a 90 MHz time base clock

\[
\text{TBPRD} = \frac{1}{2} \cdot \frac{f_{\text{TBCLK}}}{f_{\text{PWM}}} = \frac{1}{2} \cdot \frac{90 \text{ MHz}}{90 \text{ kHz}} = 500
\]

\[
\text{CMPA} = (100\% - \text{duty cycle}) \cdot \text{TBPRD} = 0.75 \cdot 500 = 375
\]

**Asymmetric PWM Computation Example**

- Determine TBPRD and CMPA for 90 kHz, 25% duty asymmetric PWM from a 90 MHz time base clock

\[
\text{TBPRD} = \frac{f_{\text{TBCLK}}}{f_{\text{PWM}}} - 1 = \frac{90 \text{ MHz}}{90 \text{ kHz}} - 1 = 999
\]

\[
\text{CMPA} = (100\% - \text{duty cycle}) \cdot (\text{TBPRD}+1) - 1 = 0.75 \cdot (999+1) - 1 = 749
\]
The dead-band sub-module provides a means to delay the switching of a gate signal, thereby allowing time for gates to turn off and preventing a short circuit.

Motivation for Dead-Band

- Transistor gates turn on faster than they shut off
- Short circuit if both gates are on at the same time!
To explain further, power-switching devices turn on faster than they shut off. This issue would momentarily provide a path from supply rail to ground, giving us a short circuit. The dead-band sub-module alleviates this issue.

Dead-band control provides a convenient means of combating current shoot-through problems in a power converter. Shoot-through occurs when both the upper and lower gates in the same phase of a power converter are open simultaneously. This condition shorts the power supply and results in a large current draw. Shoot-through problems occur because transistors open faster than they close, and because high-side and low-side power converter gates are typically switched in a complimentary fashion. Although the duration of the shoot-through current path is finite during PWM cycling, (i.e. the closing gate will eventually shut), even brief periods of a short circuit condition can produce excessive heating and over stress in the power converter and power supply.

Two basic approaches exist for controlling shoot-through: modify the transistors, or modify the PWM gate signals controlling the transistors. In the first case, the opening time of the transistor gate must be increased so that it (slightly) exceeds the closing time. One way to accomplish this is by adding a cluster of passive components such as resistors and diodes in series with the transistor gate, as shown in the next figure.

The resistor acts to limit the current rise rate towards the gate during transistor opening, thus increasing the opening time. When closing the transistor however, current flows unimpeded from...
the gate via the by-pass diode and closing time is therefore not affected. While this passive approach offers an inexpensive solution that is independent of the control microprocessor, it is imprecise, the component parameters must be individually tailored to the power converter, and it cannot adapt to changing system conditions.

The second approach to shoot-through control separates transitions on complimentary PWM signals with a fixed period of time. This is called dead-band. While it is possible to perform software implementation of dead-band, the C28x offers on-chip hardware for this purpose that requires no additional CPU overhead. Compared to the passive approach, dead-band offers more precise control of gate timing requirements. In addition, the dead time is typically specified with a single program variable that is easily changed for different power converters or adapted on-line.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBCTL</td>
<td>Dead-Band Control</td>
<td>EPwmxRegs.DBCNT.all =</td>
</tr>
<tr>
<td>DBRED</td>
<td>10-bit Rising Edge Delay</td>
<td>EPwmxRegs.DBRED =</td>
</tr>
<tr>
<td>DBFED</td>
<td>10-bit Falling Edge Delay</td>
<td>EPwmxRegs.DBFED =</td>
</tr>
</tbody>
</table>

**Rising Edge Delay** $= T_{TBCLK} \times DBRED$

**Falling Edge Delay** $= T_{TBCLK} \times DBFED$
**ePWM Dead Band Control Register**

EPwmRegs.DBCTL

**Half Cycle Clocking**
- 0 = full cycle clocking (TBCLK rate)
- 1 = half cycle clocking (TBCLK*2 rate)

**Polarity Select**
- 00 = active high
- 01 = active low complementary (RED)
- 10 = active high complementary (FED)
- 11 = active low

**Out-Mode Control**
- 00 = disabled (DBM bypass)
- 01 = PWMxA = no delay, PWMxB = FED
- 10 = PWMxA = RED, PWMxB = no delay
- 11 = RED & FED (DBM fully enabled)

**In-Mode Control**
- 00 = PWMxA is source for RED and FED
- 01 = PWMxA is source for FED, PWMxB is source for RED
- 10 = PWMxA is source for RED, PWMxB is source for FED
- 11 = PWMxB is source for RED and FED

**ePWM Chopper Sub-Module**

- Clock Prescaler
- 16-Bit Time-Base Counter
- Compare Logic
- Action Qualifier
- Dead Band
- PWM Chopper
- Digital Compare

- Clock Prescaler
- EPWMxA
- EPWMxB
- TZ1-TZ3
- COMPxOUT
- SYSCLKOUT
- EPWMxSYNCO
- EPWMxSYNCI
- TBCLK
The PWM chopper sub-module uses a high-frequency carrier signal to modulate the PWM waveform. This is used with pulsed transformer-based gate drives to control power-switching elements.

**Purpose of the PWM Chopper**

- Allows a high frequency carrier signal to modulate the PWM waveform generated by the Action Qualifier and Dead-Band modules
- Used with pulse transformer-based gate drivers to control power switching elements

As you can see in this figure, a high-frequency carrier signal is ANDed with the ePWM outputs. Also, this circuit provides an option to include a larger, one-shot pulse width before the sustaining pulses.
ePWM Chopper Sub-Module Registers
(lab file: EPwm.c)

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCCTL</td>
<td>PWM-Chopper Control</td>
<td>EPwmRegs.PCCTL.all =</td>
</tr>
</tbody>
</table>

Chopper Enable
0 = disable (bypass)
1 = enable

One-Shot Pulse Width

<table>
<thead>
<tr>
<th>Chopper Ck Duty Cycle</th>
<th>Chopper Ck Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>000 = 1/8 (12.5%)</td>
<td>000 = SYSCLKOUT/8 ÷ 1</td>
</tr>
<tr>
<td>001 = 2/8 (25.0%)</td>
<td>001 = SYSCLKOUT/8 ÷ 2</td>
</tr>
<tr>
<td>010 = 3/8 (37.5%)</td>
<td>010 = SYSCLKOUT/8 ÷ 3</td>
</tr>
<tr>
<td>011 = 4/8 (50.0%)</td>
<td>011 = SYSCLKOUT/8 ÷ 4</td>
</tr>
<tr>
<td>100 = 5/8 (62.5%)</td>
<td>100 = SYSCLKOUT/8 ÷ 5</td>
</tr>
<tr>
<td>101 = 6/8 (75.0%)</td>
<td>101 = SYSCLKOUT/8 ÷ 6</td>
</tr>
<tr>
<td>110 = 7/8 (87.5%)</td>
<td>110 = SYSCLKOUT/8 ÷ 7</td>
</tr>
<tr>
<td>111 = reserved</td>
<td>111 = SYSCLKOUT/8 ÷ 8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15 - 11</th>
<th>10 - 8</th>
<th>7 - 5</th>
<th>4 - 1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>CHPDUTY</td>
<td>CHPFREQ</td>
<td>OSHTWTH</td>
<td>CHPEN</td>
</tr>
</tbody>
</table>

One-Shot Pulse Width

<table>
<thead>
<tr>
<th>Chopper Ck Duty Cycle</th>
<th>Chopper Ck Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 = 1 x SYSCLKOUT/8</td>
<td>1000 = 9 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0001 = 2 x SYSCLKOUT/8</td>
<td>1001 = 10 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0010 = 3 x SYSCLKOUT/8</td>
<td>1010 = 11 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0011 = 4 x SYSCLKOUT/8</td>
<td>1011 = 12 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0100 = 5 x SYSCLKOUT/8</td>
<td>1100 = 13 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0101 = 6 x SYSCLKOUT/8</td>
<td>1101 = 14 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0110 = 7 x SYSCLKOUT/8</td>
<td>1110 = 15 x SYSCLKOUT/8</td>
</tr>
<tr>
<td>0111 = 8 x SYSCLKOUT/8</td>
<td>1111 = 16 x SYSCLKOUT/8</td>
</tr>
</tbody>
</table>
The trip zone and digital compare sub-modules provide a protection mechanism to protect the output pins from abnormalities, such as over-voltage, over-current, and excessive temperature rise.

**Purpose of the Digital Compare Sub-Module**

- Generates ‘compare’ events that can:
  - Trip the ePWM
  - Generate a Trip interrupt
  - Sync the ePWM
  - Generate an ADC start of conversion

- The inputs to the digital compare module are:
  - Analog comparator outputs (COMP1, COMP2, COMP3)
  - Trip-zone input pins (TZ1, TZ2, TZ3)

- A compare event is generated when one or more of its selected inputs are either high or low *(shown on later slide)*

- Optional ‘Blanking’ can be used to temporarily disable the compare action in alignment with PWM switching to eliminate noise effects
The inputs to the digital compare sub-module are the trip zone pins and the analog comparator outputs. This module generates compare events that can generate a PWM sync, generate an ADC start of conversion, trip a PWM output, and generate a trip interrupt. Optional blinking can be used to temporarily disable the compare action in alignment with PWM switching to eliminate noise effects.

Digital Compare Events

- The user selects the input for each of DCAH, DCAL, DCBH, DCBL
- Each A and B compare uses its corresponding DCyH/L inputs (y = A or B)
- The user selects the signal state that triggers each compare from the following choices:

  i. DCxH → low  DCxL → don’t care
  ii. DCxH → high DCxL → don’t care
  iii. DCxL → low  DCxH → don’t care
  iv. DCxL → high  DCxH → don’t care
  v. DCxL → high  DCxH → low
The PWM trip zone has a fast, clock-independent logic path to the PWM output pins where the outputs can be forced to high impedance. Two actions are supported: One-shot trip for major short circuits or over-current conditions, and cycle-by-cycle trip for current limiting operation.

**Trip-Zone Features**

- Trip-Zone has a fast, clock independent logic path to high-impedance EPWMxA/B output pins
- Interrupt latency may not protect hardware when responding to over current conditions or short-circuits through ISR software
- Supports:  
  1. One-shot trip for major short circuits or over current conditions
  2. Cycle-by-cycle trip for current limiting operation

The power drive protection is a safety feature that is provided for the safe operation of systems such as power converters and motor drives. It can be used to inform the monitoring program of motor drive abnormalities such as over-voltage, over-current, and excessive temperature rise. If the power drive protection interrupt is unmasked, the PWM output pins will be put in the high-impedance state immediately after the pin is driven low. An interrupt will also be generated.
### ePWM Digital Compare and Trip-Zone Sub-Module Registers

*(lab file: EPwm.c)*

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCACTL</td>
<td>DC A Control</td>
<td>EPwm*Regs.DCACTL.all =</td>
</tr>
<tr>
<td>DCBCTL</td>
<td>DC B Control</td>
<td>EPwm*Regs.DCBCTL.all =</td>
</tr>
<tr>
<td>DCTRIPSEL</td>
<td>DC Trip Select</td>
<td>EPwm*Regs.DCTRIPSEL.all =</td>
</tr>
<tr>
<td>DCCAPCTL</td>
<td>Capture Control</td>
<td>EPWM*Regs.DCCAPCTL.all =</td>
</tr>
<tr>
<td>DCCAP</td>
<td>Counter Capture</td>
<td>EPwm*Regs.DCCAP =</td>
</tr>
<tr>
<td>DCFCTL</td>
<td>DC Filter Control</td>
<td>EPwm*Regs.DCFCTL.all =</td>
</tr>
<tr>
<td>DCOFFSETCNT</td>
<td>Filter Offset Ctr</td>
<td>EPwm*Regs.DCOFFSETCNT =</td>
</tr>
<tr>
<td>DCFWINDOW</td>
<td>Filter Window</td>
<td>EPwm*Regs.DCFWINDOW =</td>
</tr>
<tr>
<td>DCFWINDOWCNT</td>
<td>Filter Window Ctr</td>
<td>EPwm*Regs.DCFWINDOWCNT =</td>
</tr>
<tr>
<td>TZDCSEL</td>
<td>Digital Compare</td>
<td>EPwm*Regs.TZDCSEL.all =</td>
</tr>
<tr>
<td>TZCTL</td>
<td>Trip-Zone Control</td>
<td>EPwm*Regs.TZCTL.all =</td>
</tr>
<tr>
<td>TZSEL</td>
<td>Trip-Zone Select</td>
<td>EPwm*Regs.TZSEL.all =</td>
</tr>
<tr>
<td>TZEINT</td>
<td>Enable Interrupt</td>
<td>EPwm*Regs.TZEINT.all =</td>
</tr>
<tr>
<td>TZFLG</td>
<td>Trip-Zone Flag</td>
<td>EPwm*Regs.TZFLG.all =</td>
</tr>
<tr>
<td>TZCLR</td>
<td>Trip-Zone Clear</td>
<td>EPwm*Regs.TZCLR.all =</td>
</tr>
<tr>
<td>TZFRC</td>
<td>Trip-Zone Force</td>
<td>EPwm*Regs.TZFRC.all =</td>
</tr>
</tbody>
</table>

### ePWM Digital Compare Trip Select Register

EPwm\*Regs.DCTRIPSEL

<table>
<thead>
<tr>
<th>Digital Compare B</th>
<th>Digital Compare B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Input Source Select</td>
<td>High Input Source Select</td>
</tr>
<tr>
<td>15 - 12</td>
<td>11 - 8</td>
</tr>
<tr>
<td>DCBLCOMPSEL</td>
<td>DCBHCOMPSEL</td>
</tr>
<tr>
<td>7 - 4</td>
<td>3 - 0</td>
</tr>
<tr>
<td>DCALCOMPSEL</td>
<td>DCAHCOMPSEL</td>
</tr>
</tbody>
</table>

Digital Compare A

<table>
<thead>
<tr>
<th>Low Input Source Select</th>
<th>High Input Source Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 = TZ1 input</td>
<td>1000 = COMP1OUT input</td>
</tr>
<tr>
<td>0001 = TZ2 input</td>
<td>1001 = COMP2OUT input</td>
</tr>
<tr>
<td>0010 = TZ3 input</td>
<td>1010 = COMP3OUT input</td>
</tr>
<tr>
<td>other values reserved</td>
<td>other values reserved</td>
</tr>
</tbody>
</table>
**ePWM Trip-Zone Digital Compare Event Select Register**

EPwmxRegs.TZDCSEL

<table>
<thead>
<tr>
<th>15 - 12</th>
<th>11 - 9</th>
<th>8 - 6</th>
<th>5 - 3</th>
<th>2 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>DCBEVT2</td>
<td>DCBEVT1</td>
<td>DCAEVT2</td>
<td>DCAEVT1</td>
</tr>
</tbody>
</table>

- **Digital Compare Output B Event 2/1 Select**
- **Digital Compare Output A Event 2/1 Select**

000 = event disable
001 = DCBH → low, DCBL → don’t care
010 = DCBH → high, DCBL → don’t care
011 = DCBL → low, DCBH → don’t care
100 = DCBL → high, DCBH → don’t care
101 = DCBL → high, DCBH → low
11x = reserved

---

**ePWM Digital Compare Control Register**

EPwmxRegs.DCyCTL (y = A or B)

- **DCyEVT2 Source Force Sync Signal Select**
  - 0 = synchronous
  - 1 = asynchronous

- **DCyEVT1 SOC Generation**
  - 0 = disable
  - 1 = enable

- **DCyEVT1 Source Force Sync Signal Select**
  - 0 = synchronous
  - 1 = asynchronous

<table>
<thead>
<tr>
<th>15 - 10</th>
<th>9</th>
<th>8</th>
<th>7 - 4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>EVT2FRC SYNCSEL</td>
<td>EVT2SRC SEL</td>
<td>reserved</td>
<td>EVT1 SYNCE</td>
<td>EVT1 SOCE</td>
<td>EVT1FRC SYNCSEL</td>
<td>EVT1SRC SEL</td>
</tr>
</tbody>
</table>

- **DCyEVT2 Source Signal Select**
  - 0 = DCyEVT2 signal
  - 1 = DCEVTFILT signal

- **DCyEVT1 Source Signal Select**
  - 0 = DCyEVT1 signal
  - 1 = DCEVTFILT signal
**ePWM Trip-Zone Control Register**

EPwm\_x\_Regs.TZCTL

<table>
<thead>
<tr>
<th>Bit 15-12</th>
<th>Bit 11-10</th>
<th>Bit 9-8</th>
<th>Bit 7-6</th>
<th>Bit 5-4</th>
<th>Bit 3-2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>DCBEVT2</td>
<td>DCBEVT1</td>
<td>DCAEVT2</td>
<td>DCAEVT1</td>
<td>TZB</td>
<td>TZA</td>
</tr>
</tbody>
</table>

- **Digital Compare Output Event 2/1 Action on EPWMxB**
- **Digital Compare Output Event 2/1 Action on EPWMxA**
- **TZ1 to TZ6 Action on EPWMxB / EPWMxA**

| 00 | high impedance |
| 01 | force high     |
| 10 | force low      |
| 11 | do nothing (disable) |

**ePWM Trip-Zone Select Register**

EPwm\_x\_Regs.TZSEL

**One-Shot Trip Zone**
- (event only cleared under S/W control; remains latched)
- 0 = disable as trip source
- 1 = enable as trip source

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCBEVT1</td>
<td>DCAEVT1</td>
<td>OSHT6</td>
<td>OSHT5</td>
<td>OSHT4</td>
<td>OSHT3</td>
<td>OSHT2</td>
<td>OSHT1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCBEVT2</td>
<td>DCAEVT2</td>
<td>CBC6</td>
<td>CBC5</td>
<td>CBC4</td>
<td>CBC3</td>
<td>CBC2</td>
<td>CBC1</td>
</tr>
</tbody>
</table>

**Cycle-by-Cycle Trip Zone**
- (event cleared when CTR = 0; i.e. cleared every PWM cycle)
- 0 = disable as trip source
- 1 = enable as trip source
The event-trigger sub-module is used to provide a triggering signal for interrupts and the start of conversion for the ADC.
Event-trigger interrupts and start of conversions can be generated on counter equals zero, counter equal period, counter equal zero or period, counter up equal compare A, counter down equal compare A, counter up equal compare B, counter down equal compare B. Notice counter up and down are independent and separate.

### ePWM Event-Trigger Sub-Module Registers

*(lab file: EPwm.c)*

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>ETSEL</td>
<td>Event-Trigger Selection</td>
<td>EPwxRegs.ETSEL.all =</td>
</tr>
<tr>
<td>ETPS</td>
<td>Event-Trigger Pre-Scale</td>
<td>EPwxRegs.ETPS.all =</td>
</tr>
<tr>
<td>ETFLG</td>
<td>Event-Trigger Flag</td>
<td>EPwxRegs.ETFLG.all =</td>
</tr>
<tr>
<td>ETCLR</td>
<td>Event-Trigger Clear</td>
<td>EPwxRegs.ETCLR.all =</td>
</tr>
<tr>
<td>ETFRC</td>
<td>Event-Trigger Force</td>
<td>EPwxRegs.ETFRC.all =</td>
</tr>
</tbody>
</table>
### ePWM Event-Trigger Selection Register

**EPwm\*Regs.ETSEL**

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14-12</th>
<th>Bit 11</th>
<th>Bit 10-8</th>
<th>Bit 7-4</th>
<th>Bit 3</th>
<th>Bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOCBEN</td>
<td>SOCBSEL</td>
<td>SOCAEN</td>
<td>SOCASEL</td>
<td>reserved</td>
<td>INTE</td>
<td>INTSEL</td>
</tr>
</tbody>
</table>

**Enable SOCB / A**
- 0 = disable
- 1 = enable

**Enable EPWMxINT**
- 0 = disable
- 1 = enable

**EPWMxSOCB / A Select**
- 000 = DCBEVT1 / DCAEVT1
- 001 = CTR = 0
- 010 = CTR = PRD
- 011 = CTR = 0 or PRD
- 100 = CTRU = CMPA
- 101 = CTRD = CMPA
- 110 = CTRU = CMPB
- 111 = CTRD = CMPB

**EPWMxINT Select**
- 000 = reserved
- 001 = CTR = 0
- 010 = CTR = PRD
- 011 = CTR = 0 or PRD
- 100 = CTRU = CMPA
- 101 = CTRD = CMPA
- 110 = CTRU = CMPB
- 111 = CTRD = CMPB

### ePWM Event-Trigger Prescale Register

**EPwm\*Regs.ETPS**

<table>
<thead>
<tr>
<th>Bit 15 - 14</th>
<th>Bit 13-12</th>
<th>Bit 11-10</th>
<th>Bit 9-8</th>
<th>Bit 7-4</th>
<th>Bit 2-3</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOCBCNT</td>
<td>SOCBPRD</td>
<td>SOCACNT</td>
<td>SOCAPRD</td>
<td>reserved</td>
<td>INTCNT</td>
<td>INTPRD</td>
</tr>
</tbody>
</table>

**EPWMxSOCB / A Counter**
(number of events have occurred)
- 00 = no events
- 01 = 1 event
- 10 = 2 events
- 11 = 3 events

**EPWMxINT Counter**
(number of events have occurred)
- 00 = no events
- 01 = 1 event
- 10 = 2 events
- 11 = 3 events

**EPWMxSOCB / A Period**
(number of events before SOC)
- 00 = disabled
- 01 = SOC on first event
- 10 = SOC on second event
- 11 = SOC on third event

**EPWMxINT Period**
(number of events before INT)
- 00 = disabled
- 01 = INT on first event
- 10 = INT on second event
- 11 = INT on third event
Hi-Resolution PWM (HRPWM)

Hi-Resolution PWM (HRPWM) significantly increases the resolution of conventionally derived digital PWM. High-resolution PWM divides a clock cycle into smaller steps called micro steps. The step size is approximately 150 picoseconds. This is typically used when PWM resolution falls below approximately 9 or 10 bits, which occurs at frequencies greater than approximately 180 kHz with a system clock of 90 MHz.

Not all ePWM outputs support HRPWM feature (see device datasheet).
The eCAP module timestamps transitions on a capture input pin.

The capture units allow time-based logging of external TTL signal transitions on the capture input pins. The C28x has up to six capture units.

Capture units can be configured to trigger an A/D conversion that is synchronized with an external event. There are several potential advantages to using the capture for this function over the ADCSOC pin associated with the ADC module. First, the ADCSOC pin is level triggered, and therefore only low to high external signal transitions can start a conversion. The capture unit does not suffer from this limitation since it is edge triggered and can be configured to start a conversion on either rising edges or falling edges. Second, if the ADCSOC pin is held high longer than one conversion period, a second conversion will be immediately initiated upon completion of the first. This unwanted second conversion could still be in progress when a desired conversion is needed. In addition, if the end-of-conversion ADC interrupt is enabled, this second conversion will trigger an unwanted interrupt upon its completion. These two problems are not a concern with the capture unit. Finally, the capture unit can send an interrupt request to the CPU while it simultaneously initiates the A/D conversion. This can yield a time savings when computations are driven by an external event since the interrupt allows preliminary calculations to begin at the start-of-conversion, rather than at the end-of-conversion using the ADC end-of-conversion interrupt. The ADCSOC pin does not offer a start-of-conversion interrupt. Rather, polling of the ADCSOC bit in the control register would need to be performed to trap the externally initiated start of conversion.
Some Uses for the Capture Module

- **Measure the time width of a pulse**
- **Low speed velocity estimation from incr. encoder:**

  **Problem:** At low speeds, calculation of speed based on a measured position change at fixed time intervals produces large estimate errors

  \[ v_k \approx \frac{x_k - x_{k-1}}{\Delta t} \]

  **Alternative:** Estimate the speed using a measured time interval at fixed position intervals

  \[ v_k \approx \frac{\Delta x}{t_k - t_{k-1}} \]

- **Auxiliary PWM generation**

---

**eCAP Module Block Diagram – Capture Mode**

The capture module features a 32-bit time-stamp counter to minimize rollover. Each module has four capture registers. Polarity can be set to trigger on rising or falling edge, and trigger events.
can be pre-scaled. The capture module can operate in absolute time-stamp mode or difference mode where the counter resets on each capture.

If the capture module is not used, it can be configured as an asynchronous PWM module.

### eCAP Module Registers

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<th>Name</th>
<th>Description</th>
<th>Structure</th>
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<td>Capture Control 1</td>
<td>ECapRegs.ECCTL1.all =</td>
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<td>ECCTL2</td>
<td>Capture Control 2</td>
<td>ECapRegs.ECCTL2.all =</td>
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<td>Time-Stamp Counter</td>
<td>ECapRegs.TSCTR =</td>
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<td>CTRPHS</td>
<td>Counter Phase Offset</td>
<td>ECapRegs.CTRPHS =</td>
</tr>
<tr>
<td>CAP1</td>
<td>Capture 1</td>
<td>ECapRegs.CAP1 =</td>
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<td>Capture 2</td>
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</tr>
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<td>CAP3</td>
<td>Capture 3</td>
<td>ECapRegs.CAP3 =</td>
</tr>
<tr>
<td>CAP4</td>
<td>Capture 4</td>
<td>ECapRegs.CAP4 =</td>
</tr>
<tr>
<td>ECEINT</td>
<td>Enable Interrupt</td>
<td>ECapRegs.ECEINT.all =</td>
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<tr>
<td>ECFLG</td>
<td>Interrupt Flag</td>
<td>ECapRegs.ECFLG.all =</td>
</tr>
<tr>
<td>ECCLR</td>
<td>Interrupt Clear</td>
<td>ECapRegs.ECCLR.all =</td>
</tr>
<tr>
<td>ECFRC</td>
<td>Interrupt Force</td>
<td>ECapRegs.ECFRC.all =</td>
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eCAP Control Register 1
ECapRegs.ECCTL1

Upper Register:

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<tbody>
<tr>
<td>FREE_SOFT</td>
<td>PRESCALE</td>
<td>CAPLDEN</td>
</tr>
</tbody>
</table>

- **Emulation Control**
  - 00 = TSCTR stops immediately
  - 01 = TSCTR runs until equals 0
  - 1X = free run (do not stop)

- **Event Filter Prescale Counter**
  - 00000 = divide by 1 (bypass)
  - 00001 = divide by 2
  - 00010 = divide by 4
  - 00011 = divide by 6
  - 00100 = divide by 8
  - ... 
  - 11110 = divide by 60
  - 11111 = divide by 62

---

Counter Reset on Capture Event
- 0 = no reset (absolute time stamp mode)
- 1 = reset after capture (difference mode)

Capture Event Polarity
- 0 = trigger on rising edge
- 1 = trigger on falling edge
### eCAP Control Register 2

**ECapxRegs.ECCTL2**

#### Upper Register:

- **Capture / APWM mode**
  - 0 = capture mode
  - 1 = APWM mode

- **APWM Output Polarity**
  - (valid only in APWM mode)
  - 0 = active high output
  - 1 = active low output

- **Software Force Counter Synchronization**
  - 0 = no effect
  - 1 = TSCTR load of current module and other modules if SYNCO_SEL bits = 00

#### Lower Register:

- **Counter Sync-In**
  - (capture mode only)
  - 0 = disable
  - 1 = enable

- **Re-arm**
  - (capture mode only)
  - 0 = no effect
  - 1 = arm sequence

- **Continuous/One-Shot**
  - (capture mode only)
  - 0 = continuous mode
  - 1 = one-shot mode

- **Sync-Out Select**
  - 00 = sync-in to sync-out
  - 01 = CTR = PRD event generates sync-out
  - 1X = disable

- **Time Stamp Counter Stop**
  - 0 = stop
  - 1 = run

- **Stop Value for One-Shot Mode/ Wrap Value for Continuous Mode**
  - (capture mode only)
  - 00 = stop/wrap after capture event 1
  - 01 = stop/wrap after capture event 2
  - 10 = stop/wrap after capture event 3
  - 11 = stop/wrap after capture event 4
The capture unit interrupts offer immediate CPU notification of externally captured events. In situations where this is not required, the interrupts can be masked and flag testing/polling can be used instead. This offers increased flexibility for resource management. For example, consider a servo application where a capture unit is being used for low-speed velocity estimation via a pulsing sensor. The velocity estimate is not used until the next control law calculation is made, which is driven in real-time using a timer interrupt. Upon entering the timer interrupt service routine, software can test the capture interrupt flag bit. If sufficient servo motion has occurred since the last control law calculation, the capture interrupt flag will be set and software can proceed to compute a new velocity estimate. If the flag is not set, then sufficient motion has not occurred and some alternate action would be taken for updating the velocity estimate. As a second example, consider the case where two successive captures are needed before a computation proceeds (e.g. measuring the width of a pulse). If the width of the pulse is needed as soon as the pulse ends, then the capture interrupt is the best option. However, the capture interrupt will occur after each of the two captures, the first of which will waste a small number of cycles while the CPU is interrupted and then determines that it is indeed only the first capture. If the width of the pulse is not needed as soon as the pulse ends, the CPU can check, as needed, the capture registers to see if two captures have occurred, and proceed from there.
What is an Incremental Quadrature Encoder?

A digital (angular) position sensor

- Photo sensors spaced $\theta/4$ deg. apart
- Slots spaced $\theta$ deg. apart
- Light source (LED)

Incremental Optical Encoder

Quadrature Output from Photo Sensors

The eQEP circuit, when enabled, decodes and counts the quadrature encoded input pulses. The QEP circuit can be used to interface with an optical encoder to get position and speed information from a rotating machine.

How is Position Determined from Quadrature Signals?

Position resolution is $\theta/4$ degrees

$$(A,B) = (00, 01, 10, 11)$$

Quadrature Decoder

State Machine

Illegal Transitions; generate phase error interrupt

Increment counter

Decrement counter

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Using a quadrature decoder state machine, we can determine if the counter is incrementing or decrementing, and therefore know if the disc is moving clockwise or counterclockwise.

The QEP module features a direct interface to encoders. In addition to channels A and B being used for rotational directional information, the index can be used to determine rotational speed, and the strobe can be used for position from a homing sensor.
Lab 7: Control Peripherals

Objective

The objective of this lab is to become familiar with the programming and operation of the control peripherals and their interrupts. ePWM1A will be setup to generate a 2 kHz, 25% duty cycle symmetric PWM waveform. The waveform will then be sampled with the on-chip analog-to-digital converter and displayed using the graphing feature of Code Composer Studio. Next, eCAP1 will be setup to detect the rising and falling edges of the waveform. This information will be used to determine the width of the pulse and duty cycle of the waveform. The results of this step will be viewed numerically in a memory window.

Procedure

Open the Project

1. A project named Lab7 has been created for this lab. Open the project by clicking on Project ➔ Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab7\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:
Lab 7: Control Peripherals

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Note: The ECap_7_8_9_10_12.c file will be added and used with eCAP1 to detect the rising and falling edges of the waveform in the second part of this lab exercise.

**Setup Shared I/O and ePWM1**

2. Edit Gpio.c and adjust the shared I/O pin in GPIO0 for the PWM1A function.

3. In EPwm_7_8_9_10_12.c, setup ePWM1 to implement the PWM waveform as described in the objective for this lab. The following registers need to be modified: TBCTL (set clock prescales to divide-by-1, no software force, sync and phase disabled), TBPRD, CMPA, CMPCTL (load on 0 or PRD), and AQCTLA (set on up count and clear on down count for output A). Software force, deadband, PWM chopper and trip action has been disabled. (Hint – notice the last steps enable the timer count mode and enable the clock to the ePWM module). Either calculate the values for TBPRD and CMPA (as a challenge) or make use of the global variable names and values that have been set using #define in the beginning of Lab.h file. Notice that ePWM2 has been initialized earlier in the code for the ADC lab. Save your work and close the modified files.

**Build and Load**

4. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.

5. Click the “Debug” button (green bug). The “CCS Debug Perspective” view should open, the program will load automatically, and you should now be at the start of main(). If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to EMU_BOOT_SARAM using the Scripts menu.

**Run the Code – PWM Waveform**

6. Open a memory browser to view some of the contents of the ADC results buffer. The address label for the ADC results buffer is AdcBuf (type &AdcBuf) in the “Data” memory page. We will be running our code in real-time mode, and we will need to have the memory window continuously refresh.

7. Using a connector wire provided, connect the PWM1A (pin # GPIO-00) to ADCINA0 (pin # ADC-A0) on the Docking Station.

8. Run the code (real-time mode) using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset. Watch the window update. Verify that the ADC result buffer contains the updated values.
9. Open and setup a graph to plot a 50-point window of the ADC results buffer. Click: **Tools** → **Graph** → **Single Time** and set the following values:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Buffer Size</td>
<td>50</td>
</tr>
<tr>
<td>DSP Data Type</td>
<td>16-bit unsigned integer</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address</td>
<td>AdcBuf</td>
</tr>
<tr>
<td>Display Data Size</td>
<td>50</td>
</tr>
<tr>
<td>Time Display Unit</td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

Select **OK** to save the graph options.

10. The graphical display should show the generated 2 kHz, 25% duty cycle symmetric PWM waveform. The period of a 2 kHz signal is 500 \(\mu s\). You can confirm this by measuring the period of the waveform using the “measurement marker mode” graph feature. Disable continuous refresh for the graph before taking the measurements. In the graph window toolbar, left-click on the ruler icon with the red arrow. Note when you hover your mouse over the icon, it will show “Toggle Measurement Marker Mode”. Move the mouse to the first measurement position and left-click. Again, left-click on the Toggle Measurement Marker Mode icon. Move the mouse to the second measurement position and left-click. The graph will automatically calculate the difference between the two values taken over a complete waveform period. When done, clear the measurement points by right-clicking on the graph and select **Remove All Measurement Marks**. Then enable continuous refresh for the graph.

### Frequency Domain Graphing Feature of Code Composer Studio

11. Code Composer Studio also has the ability to make frequency domain plots. It does this by using the PC to perform a Fast Fourier Transform (FFT) of the DSP data. Let's make a frequency domain plot of the contents in the ADC results buffer (i.e. the PWM waveform).

Click: **Tools** → **Graph** → **FFT Magnitude** and set the following values:
Acquisition Buffer Size 50
DSP Data Type 16-bit unsigned integer
Sampling Rate (Hz) 50000
Start Address AdcBuf
Data Plot Style Bar
FFT Order 10

Select OK to save the graph options.

12. On the plot window, hold the mouse left-click key and move the marker line to observe the frequencies of the different magnitude peaks. Do the peaks occur at the expected frequencies?

13. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

Setup eCAP1 to Measure Width of Pulse

The first part of this lab exercise generated a 2 kHz, 25% duty cycle symmetric PWM waveform which was sampled with the on-chip analog-to-digital converter and displayed using the graphing feature of Code Composer Studio. Next, eCAP1 will be set up to detect the rising and falling edges of the waveform. This information will be used to determine the period and duty cycle of the waveform. The results of this step will be viewed numerically in a memory window and can be compared to the results obtained using the graphing features of Code Composer Studio.

14. Switch to the “CCS Edit Perspective” view by clicking the CCS Edit icon in the upper right-hand corner. Add the following file to the project from C:\C28x\Labs\Lab7\Files:

ECap_7_8_9_10_12.c

Check your files list to make sure the file is there.

15. In Main_7.c, add code to call the InitECap() function. There are no passed parameters or return values, so the call code is simply:

    InitECap();

16. Edit Gpio.c and adjust the shared I/O pin in GPIO5 for the ECAP1 function.

17. Open and inspect the eCAP1 interrupt service routine (ECAP1_INT_ISR) in the file DefaultIsr_7.c. Notice that PwmDuty is calculated by CAP2 – CAP1 (rising to falling edge) and that PwmPeriod is calculated by CAP3 – CAP1 (rising to rising edge).

18. In ECap_7_8_9_10_12.c, setup eCAP1 to calculate PWM_duty and PWM_period. The following registers need to be modified: ECCTL2 (continuous mode, re-arm disable, and sync disable), ECCTL1 (set prescale to divide-by-1, configure capture event polarity without resetting the counter), and ECEINT (enable desired eCAP interrupt).
19. Using the “PIE Interrupt Assignment Table” find the location for the eCAP1 interrupt “ECAP1_INT” and fill in the following information:

PIE group #:__________  # within group:__________

This information will be used in the next step.

20. Modify the end of ECap_7_8_9_10_12.c to do the following:
- Enable the “ECAP1_INT” interrupt in the PIE (Hint: use the PieCtrlRegs structure)
- Enable the appropriate core interrupt in the IER register

**Build and Load**

21. Save all changes to the files and click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.

**Run the Code – Pulse Width Measurement**

22. Open a memory browser to view the address label PwmPeriod. (Type &PwmPeriod in the address box). The address label PwmDuty (address &PwmDuty) should appear in the same memory browser window.

23. Set the memory browser properties format to “32-Bit Unsigned Integer”. We will be running our code in real-time mode, and we will need to have the memory browser continuously refresh.

24. Using the connector wire provided, connect the PWM1A (pin # GPIO-00) to ECAP1 (pin # GPIO-05) on the Docking Station.

25. Run the code (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset. Notice the values for PwmDuty and PwmPeriod.

26. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

**Questions:**

- How do the captured values for PwmDuty and PwmPeriod relate to the compare register CMPA and time-base period TBPRD settings for ePWM1A?
- What is the value of PwmDuty in memory?
- What is the value of PwmPeriod in memory?
- How does it compare with the expected value?
Terminate Debug Session and Close Project

27. Terminate the active debug session using the Terminate button. This will close the debugger and return CCS to the “CCS Edit Perspective” view.

28. Next, close the project by right-clicking on Lab7 in the Project Explorer window and select Close Project.

Optional Exercise

If you finish early, you might want to experiment with the code by observing the effects of changing the ePWM1 CMPA register using real-time emulation. Be sure that the jumper wire is connecting PWM1A (pin # GPIO-00) to ADCINA0 (pin # ADC-A0), and the Single Time graph is displayed. The graph must be enabled for continuous refresh. Run the code in real-time mode. Open an Expressions window to the EPwm1Regs.CMPA register – in EPwm.c highlight the “EPwm1Regs” structure and right click, then select Add Watch Expression… and then OK. In the Expressions window open “EPwm1Regs”, then open “CMPA” and open “half”. Under “half” change the “CMPA” value. The Expressions window must be enabled for continuous refresh. Notice the effect on the PWM waveform in the graph.

You have just modulated the PWM waveform by manually changing the CMPA value. Next, we will modulate the PWM automatically by having the ADC ISR change the CMPA value. In DefaultIsr.c notice the code in ADCINT1_ADC used to modulate the ePWM1A output between 10% and 90% duty cycle. In Main.c add “PWM_MODULATE” to the Expressions window using the same procedure above. Then with the code running in real-time mode, change the “PWM_MODULATE” from 0 to 1 and observe the PWM waveform in the graph. Also, in the Expressions window notice the CMPA value being updated. (If you do not have time to work on this optional exercise, you may want to try this after the class).

End of Exercise
Introduction

In this module, numerical concepts will be explored. One of the first considerations concerns multiplication – how does the user store the results of a multiplication, when the process of multiplication creates results larger than the inputs. A similar concern arises when considering accumulation – especially when long summations are performed. Next, floating-point concepts will be explored and IQmath will be described as a technique for implementing a “virtual floating-point” system to simplify the design process.

The IQmath Library is a collection of highly optimized and high precision mathematical functions used to seamlessly port floating-point algorithms into fixed-point code. These C/C++ routines are typically used in computationally intensive real-time applications where optimal execution speed and high accuracy is needed. By using these routines a user can achieve execution speeds considerable faster than equivalent code written in standard ANSI C language. In addition, by incorporating the ready-to-use high precision functions, the IQmath library can shorten significantly a DSP application development time. (The IQmath user's guide is included in the application zip file, and can be found in the /docs folder once the file is extracted and installed).

Module Objectives

- Integers and Fractions
- IEEE-754 Floating-Point
- IQmath
- Format Conversion of ADC Results
Module Topics

Numerical Concepts

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Numbering System Basics

Given the ability to perform arithmetic processes (addition and multiplication) with the C28x, it is important to understand the underlying mathematical issues which come into play. Therefore, we shall examine the numerical concepts which apply to the C28x and, to a large degree, most processors.

Binary Numbers

The binary numbering system is the simplest numbering scheme used in computers, and is the basis for other schemes. Some details about this system are:

- It uses only two values: 1 and 0
- Each binary digit, commonly referred to as a bit, is one “place” in a binary number and represents an increasing power of 2.
- The least significant bit (LSB) is to the right and has the value of 1.
- Values are represented by setting the appropriate 1's in the binary number.
- The number of bits used determines how large a number may be represented.

Examples:

0110₂ = (0 * 8) + (1 * 4) + (1 * 2) + (0 * 1) = 6₁₀
1111₀₂ = (1 * 16) + (1 * 8) + (1 * 4) + (1 * 2) + (0 * 1) = 30₁₀

Two's Complement Numbers

Notice that binary numbers can only represent positive numbers. Often it is desirable to be able to represent both positive and negative numbers. The two's complement numbering system modifies the binary system to include negative numbers by making the most significant bit (MSB) negative. Thus, two's complement numbers:

- Follow the binary progression of simple binary except that the MSB is negative — in addition to its magnitude
- Can have any number of bits — more bits allow larger numbers to be represented

Examples:

0110₂ = (0 * -8) + (1 * 4) + (1 * 2) + (0 * 1) = 6₁₀
1111₀₂ = (1 * -16) + (1 * 8) + (1 * 4) + (1 * 2) + (0 * 1) = -2₁₀

The same binary values are used in these examples for two's complement as were used above for binary. Notice that the decimal value is the same when the MSB is 0, but the decimal value is quite different when the MSB is 1.

Two operations are useful in working with two's complement numbers:

- The ability to obtain an additive inverse of a value
- The ability to load small numbers into larger registers (by sign extending)
To load small two's complement numbers into larger registers:

The MSB of the original number must carry to the MSB of the number when represented in the larger register.

1. Load the small number “right justified” into the larger register.
2. Copy the sign bit (the MSB) of the original number to all unfilled bits to the left in the register (sign extension).

Consider our two previous values, copied into an 8-bit register:

**Examples:**

<table>
<thead>
<tr>
<th>Original No.</th>
<th>0 1 1 0₂</th>
<th>= 6₁₀</th>
<th>1 1 1 1 0₂</th>
<th>= -2₁₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Load low</td>
<td>0 1 1 0</td>
<td></td>
<td>1 1 1 1 0</td>
<td></td>
</tr>
<tr>
<td>2. Sign Extend</td>
<td>0 0 0 0 0 1 1 0</td>
<td>= 4 + 2 = 6</td>
<td>1 1 1 1 1 1 0</td>
<td>= -128 + 64 + ... + 2 = -2</td>
</tr>
</tbody>
</table>

**Integer Basics**

- **Unsigned Binary Integers**
  
  \[ 0100b = (0 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (0 \times 2^0) = 4 \]
  
  \[ 1101b = (1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) = 13 \]

- **Signed Binary Integers (2’s Complement)**
  
  \[ 0100b = (0 \times -2^3) + (1 \times 2^2) + (0 \times 2^1) + (0 \times 2^0) = 4 \]
  
  \[ 1101b = (1 \times -2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) = -3 \]
Sign Extension Mode

The C28x can operate on either unsigned binary or two's complement operands. The “Sign Extension Mode” (SXM) bit, present within a status register of the C28x, identifies whether or not the sign extension process is used when a value is brought into the accumulator. It is good programming practice to always select the desired SXM at the beginning of a module to assure the proper mode.

What is Sign Extension?

- When moving a value from a narrowed width location to a wider width location, the sign bit is extended to fill the width of the destination
- Sign extension applies to signed numbers only
- It keeps negative numbers negative!
- Sign extension controlled by SXM bit in ST0 register; When SXM = 1, sign extension happens automatically

4 bit Example: Load a memory value into the ACC

```
memory 1101 = -2^3 + 2^2 + 2^0 = -3

Load and sign extend

ACC 1111 | 1101 = -2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^0

= -128 + 64 + 32 + 16 + 8 + 4 + 1
= -3
```
Binary Multiplication

Now that you understand two's complement numbers, consider the process of multiplying two two's complement values. As with “long hand” decimal multiplication, we can perform binary multiplication one “place” at a time, and sum the results together at the end to obtain the total product.

Note: This is not the method the C28x uses in multiplying numbers — it is merely a way of observing how binary numbers work in arithmetic processes.

The C28x uses 16-bit operands and a 32-bit accumulator. For the sake of clarity, consider the example below where we shall investigate the use of 4-bit values and an 8-bit accumulation:

<table>
<thead>
<tr>
<th>Integer Multiplication (signed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0100</td>
</tr>
<tr>
<td>x 1101</td>
</tr>
<tr>
<td>00000100</td>
</tr>
<tr>
<td>0000000</td>
</tr>
<tr>
<td>000100</td>
</tr>
<tr>
<td>11100</td>
</tr>
<tr>
<td>1110100</td>
</tr>
<tr>
<td><strong>Accumulator</strong> 1110100</td>
</tr>
<tr>
<td><strong>Data Memory</strong> ?</td>
</tr>
</tbody>
</table>

In this example, consider the following:
- What are the two input values, and the expected result?
- Why are the “partial products” shifted left as the calculation continues?
- Why is the final partial product “different” than the others?
- What is the result obtained when adding the partial products?
- How shall this result be loaded into the accumulator?
- How shall we fill the remaining bit? Is this value still the expected one?
- How can the result be stored back to memory? What problems arise?

Note: With two’s complement multiplication, the leading “1” in the second multiplicand is a sign bit. If the sign bit is “1”, then take the 2’s complement of the first multiplicand. Additionally, each partial product must be sign-extended for correct computation.
Note: All of the above questions except the final one are addressed in this module. The last question may have several answers:

- Store the lower accumulator to memory. What problem is apparent using this method in this example?
- Store the upper accumulator back to memory. Wouldn't this create a loss of precision, and a problem in how to interpret the results later?
- Store both the upper and lower accumulator to memory. This solves the above problems, but creates some new ones:
  - Extra code space, memory space, and cycle time are used
  - How can the result be used as the input to a subsequent calculation? Is such a condition likely (consider any “feedback” system)?

From this analysis, it is clear that integers do not behave well when multiplied. Might some other type of number system behave better? Is there a number system where the results of a multiplication are bounded?
Binary Fractions

Given the problems associated with integers and multiplication, consider the possibilities of using **fractional** values. Fractions do not grow when multiplied, therefore, they remain representable within a given word size and solve the problem. Given the benefit of fractional multiplication, consider the issues involved with using fractions:

- How are fractions represented in two's complement?
- What issues are involved when multiplying two fractions?

**Representing Fractions in Binary**

In order to represent both positive and negative values, the two's complement process will again be used. However, in the case of fractions, we will not set the LSB to 1 (as was the case for integers). When one considers that the range of fractions is from -1 to ~+1, and that the only bit which conveys negative information is the MSB, it seems that the MSB must be the “negative ones position.” Since binary representation is based on powers of two, it follows that the next bit would be the “one-halves” position, and that each following bit would have half the magnitude again. Considering, as before, a 4-bit model, we have the representation shown in the following example.

\[
\begin{array}{cccc}
1 & 0 & 1 & 1 \\
\hline
-1 & 1/2 & 1/4 & 1/8 \\
\end{array}
\]

\[-1 + 1/4 + 1/8 = -5/8\]

**Fraction Basics**

\[
\begin{array}{cccc}
-2^0 & 2^{-1} & 2^{-2} & 2^{-3} & \cdots & 2^{-(n-1)} \\
\hline
1101b &= (1*2^0) + (1*2^{-1}) + (0*2^{-2}) + (1*2^{-3}) \\
&= -1 + 1/2 + 1/8 \\
&= -3/8 \\
\end{array}
\]

*Fractions have the nice property that fraction x fraction = fraction*
Multiplying Binary Fractions

When the C28x performs multiplication, the process is identical for all operands, integers or fractions. Therefore, the user must determine how to interpret the results. As before, consider the 4-bit multiply example:

```
Fraction Multiplication

\[
\begin{array}{c|c}
0100 & 1/2 \\
\times 1101 & x -3/8 \\
\hline
00000100 & \\
000000 & \\
000100 & \\
1110 & \\
11110100 & -3/16 \\
\hline
\end{array}
\]

Accumulator 11101010

Data Memory 1110

As before, consider the following:

- What are the two input values and the expected result?
- As before, “partial products” are shifted left and the final is negative.
- How is the result (obtained when adding the partial products) read?
- How shall this result be loaded into the accumulator?
- How shall we fill the remaining bit? Is this value still the expected one?
- How can the result be stored back to memory? What problems arise?

To “read” the results of the fractional multiply, it is necessary to locate the binary point (the base 2 equivalent of the base 10 decimal point). Start by identifying the location of the binary point in the input values. The MSB is an integer and the next bit is 1/2, therefore, the binary point would be located between them. In our example, therefore, we would have three bits to the right of the binary point in each input value. For ease of description, we can refer to these as “Q3” numbers, where Q refers to the number of places to the right of the point.

When multiplying numbers, the Q values add. Thus, we would (mentally) place a binary point above the sixth LSB. We can now calculate the “Q6” result more readily.
As with integers, the results are loaded low and the MSB is a sign extension of the seventh bit. If this value were loaded into the accumulator, we could store the results back to memory in a variety of ways:

- Store both low and high accumulator values back to memory. This offers maximum detail, but has the same problems as with integer multiply.
- Store only the high (or low) accumulator back to memory. This creates a potential for a memory littered with varying Q-types.
- Store the upper accumulator shifted to the left by 1. This would store values back to memory in the same Q format as the input values, and with equal precision to the inputs. How shall the left shift be performed? Here’s three methods:
  - Explicit shift (C or assembly code)
  - Shift on store (assembly code)
  - Use Product Mode shifter (assembly code)
Fraction Coding

Although COFF tools recognize values in integer, hex, binary, and other forms, they understand only integer, or non-fractional values. To use fractions within the C28x, it is necessary to describe them as though they were integers. This turns out to be a very simple trick. Consider the following number lines:

### Coding Traditional 16-bit Q15 Fractions

-1  32767  0xFFFF
  1/2  16384  0x4000
   0  0  0x0000
-1/2 * 32768 (2^15) -16384  0xC000
  -1 -32768  0x8000

**Fraction**  **Integer**

- C-code example: \( y = 0.707 \times x \)

```c
void main(void)
{
  int16 coef = 32768*707/1000;  // 0.707 in Q15
  int16 x, y;
  y = (int16)((int32)coef * (int32)x) >> 15;
}
```

By multiplying a fraction by 32K (32768), a normalized fraction is created, which can be passed through the COFF tools as an integer. Once in the C28x, the normalized fraction looks and behaves exactly as a fraction. Thus, when using fractional constants in a C28x program, the coder first multiplies the fraction by 32768, and uses the resulting integer (rounded to the nearest whole value) to represent the fraction.

The following is a simple, but effective method for getting fractions past the assembler:

1. Express the fraction as a decimal number (drop the decimal point).
2. Multiply by 32768.
3. Divide by the proper multiple of 10 to restore the decimal position.

**Examples:**

- To represent 0.62: \( 32768 \times 62 / 100 \)
- To represent 0.1405: \( 32768 \times 1405 / 10000 \)

This method produces a valid number accurate to 16 bits. You will not need to do the math yourself, and changing values in your code becomes rather simple.
Fractional vs. Integer Representation

**Integer vs. Fractions**

<table>
<thead>
<tr>
<th></th>
<th>Range</th>
<th>Precision</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integer</td>
<td>determined by # of bits</td>
<td>1</td>
</tr>
<tr>
<td>Fraction</td>
<td>~+1 to -1</td>
<td>determined by # of bits</td>
</tr>
</tbody>
</table>

- Integers grow when you multiply them
- Fractions have limited range
  - Fractions can still grow when you add them
  - Scaling an application is time consuming

*Are there any other alternatives?*

The C28x accumulator, a 32-bit register, adds extra range to integer calculations, but this becomes a problem in storing the results back to 16-bit memory.

Conversely, when using fractions, the extra accumulator bits increase precision, which helps minimize accumulative errors. Since any number is accurate (at best) to ± one-half of a LSB, summing two of these values together would yield a worst case result of 1 LSB error. Four summations produce two LSBs of error. By 256 summations, eight LSBs are “noisy.” Since the accumulator holds 32 bits of information, and fractional results are stored from the high accumulator, the extra range of the accumulator is a major benefit in noise reduction for long sum-of-products type calculations.
Floating-Point

IEEE-754 Single Precision Floating-Point

Case 1: if \( e = 255 \) and \( f \neq 0 \), then \( v = \text{NaN} \)

Case 2: if \( e = 255 \) and \( f = 0 \), then \( v = [(-1)^s] \times \text{infinity} \)

Case 3: if \( 0 < e < 255 \), then \( v = [(-1)^s] \times 2^{(e-127)} \times (1.f) \)

Case 4: if \( e = 0 \) and \( f \neq 0 \), then \( v = [(-1)^s] \times 2^{(-126)} \times (0.f) \)

Case 5: if \( e = 0 \) and \( f = 0 \), then \( v = [(-1)^s] \times 0 \)

Example: \( 0x41200000 = 0 \ 100 \ 0001 \ 0 \ 010 \ 0000 \ 0000 \ 0000 \ b \)

\( e = 130 \)

\( f = 2^{-1} = 0.25 \)

\( \Rightarrow \) Case 3

\( v = (-1)^s \times 2^{(130-127)} \times 1.25 = 10.0 \)

Advantage \( \Rightarrow \) Exponent gives large dynamic range

Disadvantage \( \Rightarrow \) Precision of a number depends on its exponent

Number Line Insight

Non-uniform distribution
- Precision greatest near zero
- Less precision the further you get from zero
Using Floating-Point

- Set the “Specify floating point support” project option to ‘fpu32’
- When creating a new CCS project, choosing a device variant that has the FPU will automatically select this option, so normally no user action is required

- Adds the floating-point RTS library(s) to the CCS project
  - standard RTS lib (required)
    - rts2800_fpu32.lib
      - comes with compiler
    - fast RTS lib (optional)
      - C28x_FPU_FastRTS.lib
      - on TI web, #SPRC664
      - improved performance
      - Strongly Recommended
  - Selects ‘fpu32’ support in CCS build configuration settings

Getting the ADC Result into Floating-Point Format

```
#define AdcFsVoltage float(3.3) // ADC full scale voltage
float Result;               // ADC result
void main(void)
{
    // Convert unsigned 16-bit result to 32-bit float. Gives value of 0 to 4095.
    // Scale result by 1/4096. Gives value of 0 to -1.
    // Scale result by AdcFsVoltage. Gives value of 0 to ~3.3.
    Result = (AdcFsVoltage/4096.0)*(float)AdcResult.ADCRESULT0;
}
```

Compiler will pre-compute at build-time.
No runtime division!
Floating-Point Pros and Cons

◆ Advantages
  ◆ Easy to write code
  ◆ No scaling required

◆ Disadvantages
  ◆ Somewhat higher device cost
  ◆ May offer insufficient precision for some calculations due to 23 bit mantissa and the influence of the exponent

What if you don’t have the luxury of using a floating-point C28x device?
IQmath

Implementing complex digital control algorithms on a Digital Signal Processor (DSP), or any other DSP capable processor, typically come across the following issues:

- Algorithms are typically developed using floating-point math
- Floating-point devices are more expensive than fixed-point devices
- Converting floating-point algorithms to a fixed-point device is very time consuming
- Conversion process is one way and therefore backward simulation is not always possible

The design may initially start with a simulation (i.e. MatLab) of a control algorithm, which typically would be written in floating-point math (C or C++). This algorithm can be easily ported to a floating-point device, however because of cost reasons most likely a 16-bit or 32-bit fixed-point device would be used in many target systems.

The effort and skill involved in converting a floating-point algorithm to function using a 16-bit or 32-bit fixed-point device is quite significant. A great deal of time (many days or weeks) would be needed for reformatting, scaling and coding the problem. Additionally, the final implementation typically has little resemblance to the original algorithm. Debugging is not an easy task and the code is not easy to maintain or document.

IQ Fractional Representation

A new approach to fixed-point algorithm development, termed “IQmath”, can greatly simplify the design development task. This approach can also be termed “virtual floating-point” since it looks like floating-point, but it is implemented using fixed-point techniques.

| Advantage | Precision same for all numbers in an IQ format |
| Disadvantage | Limited dynamic range compared to floating-point |

\[-2^I + 2^{I-1} + \ldots + 2^1 + 2^0 \cdot 2^{-1} + 2^{-2} + \ldots + 2^{-Q}\]

I8Q24 Example: 0x41200000

\[= 0100 0001 . 0010 0000 0000 0000 0000 0000\ b\]

\[= 2^6 + 2^0 + 2^{-3} = 65.125\]
The IQmath approach enables the seamless portability of code between fixed and floating-point devices. This approach is applicable to many problems that do not require a large dynamic range, such as motor or digital control applications.

Number Line Insight

Distributions

- Floating-Point: non-uniform distribution (variable precision)
- IQ Fractions: uniform distribution (same precision everywhere)

- Both floating-point and IQ formats have $2^{32}$ possible values on the number line
- It’s how each distributes these values that differs

Traditional “Q” Math Approach

Traditional 32-bit “Q” Math Approach

$y = mx + b$

in C:

```c
Y = ((int64) M * (int64) X + (int64) B << Q) >> Q;
```

Note: Requires support for 64-bit integer data type in compiler.
The traditional approach to performing math operations, using fixed-point numerical techniques can be demonstrated using a simple linear equation example. The floating-point code for a linear equation would be:

```c
float Y, M, X, B;
Y = M * X + B;
```

For the fixed-point implementation, assume all data is 32-bits, and that the "Q" value, or location of the binary point, is set to 24 fractional bits (Q24). The numerical range and resolution for a 32-bit Q24 number is as follows:

<table>
<thead>
<tr>
<th>Q value</th>
<th>Min Value</th>
<th>Max Value</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q24</td>
<td>(-2^{32-24} = -128,000,000)</td>
<td>(2^{32-24} \cdot (\frac{1}{2})^{24} = 127,999,999)</td>
<td>((\frac{1}{2})^{24} = 0.000,000,06)</td>
</tr>
</tbody>
</table>

The C code implementation of the linear equation is:

```c
int32 Y, M, X, B; // numbers are all Q24
Y = ((int64) M * (int64) X + (int64) B << 24) >> 24;
```

Compared to the floating-point representation, it looks quite cumbersome and has little resemblance to the floating-point equation. It is obvious why programmers prefer using floating-point math.

The slide shows the implementation of the equation on a processor containing hardware that can perform a 32x32 bit multiplication, 64-bit addition and 64-bit shifts (logical and arithmetic) efficiently.

The basic approach in traditional fixed-point "Q" math is to align the binary point of the operands that get added to or subtracted from the multiplication result. As shown in the slide, the multiplication of M and X (two Q24 numbers) results in a Q48 value that is stored in a 64-bit register. The value B (Q24) needs to be scaled to a Q48 number before addition to the M*X value (low order bits zero filled, high order bits sign extended). The final result is then scaled back to a Q24 number (arithmetic shift right) before storing into Y (Q24). Many programmers may be familiar with 16-bit fixed-point "Q" math that is in common use. The same example using 16-bit numbers with 15 fractional bits (Q15) would be coded as follows:

```c
int16 Y, M, X, B; // numbers are all Q15
Y = ((int32) M * (int32) X + (int32) B << 15) >> 15;
```

In both cases, the principal methodology is the same. The binary point of the operands that get added to or subtracted from the multiplication result must be aligned.
In the "IQmath" approach, rather than scaling the operands, which get added to or subtracted from the multiplication result, we do the reverse. The multiplication result binary point is scaled back such that it aligns to the operands, which are added to or subtracted from it. The C code implementation of this is given by linear equation below:

```c
int32 Y, M, X, B;
Y = ((int64) M * (int64) X) >> 24 + B;
```

The slide shows the implementation of the equation on a processor containing hardware that can perform a 32x32 bit multiply, 32-bit addition/subtraction and 64-bit logical and arithmetic shifts efficiently.

The key advantage of this approach is shown by what can then be done with the C and C++ compiler to simplify the coding of the linear equation example.

Let’s take an additional step and create a multiply function in C that performs the following operation:

```c
int32 _IQ24mpy(int32 M, int32 X) { return ((int64) M * (int64) X) >> 24; }
```

The linear equation can then be written as follows:

```c
Y = _IQ24mpy(M, X) + B;
```

Already we can see a marked improvement in the readability of the linear equation.
Using the operator overloading features of C++, we can overload the multiplication operand "*" such that when a particular data type is encountered, it will automatically implement the scaled multiply operation. Let’s define a data type called "iq" and assign the linear variables to this data type:

```cpp
iq Y, M, X, B // numbers are all Q24
```

The overloading of the multiply operand in C++ can be defined as follows:

```cpp
iq operator*(const iq &M, const iq &X){return((int64)M*(int64) X) >> 24;}
```

Then the linear equation, in C++, becomes:

```cpp
Y = M * X + B;
```

This final equation looks identical to the floating-point representation. It looks "natural". The four approaches are summarized in the table below:

<table>
<thead>
<tr>
<th>Math Implementations</th>
<th>Linear Equation Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-bit floating-point math in C</td>
<td>Y = M * X + B;</td>
</tr>
<tr>
<td>32-bit fixed-point &quot;Q&quot; math in C</td>
<td>Y = ((int64) M * (int64) X) + (int64) B &lt;&lt; 24) &gt;&gt; 24;</td>
</tr>
<tr>
<td>32-bit IQmath in C</td>
<td>Y = _IQ24mpy(M, X) + B;</td>
</tr>
<tr>
<td>32-bit IQmath in C++</td>
<td>Y = M * X + B;</td>
</tr>
</tbody>
</table>

Essentially, the mathematical approach of scaling the multiplier operand enables a cleaner and a more "natural" approach to coding fixed-point problems. For want of a better term, we call this approach "IQmath" or can also be described as "virtual floating-point".
IQmath Approach

Multiply Operation

\[ Y = ((i64) M \times (i64) X) \gg Q + B; \]

Redefine the multiply operation as follows:

\[ _{IQmpy}(M,X) == ((i64) M \times (i64) X) \gg Q \]

This simplifies the equation as follows:

\[ Y = _{IQmpy}(M,X) + B; \]

C28x compiler supports "_{IQmpy}" intrinsic; assembly code generated:

| MOVL XT,@M  | IMPYL P,XT,@X       | P = low 32-bits of M*X |
| QMPIL ACC,XT,@X     | ACC = high 32-bits of M*X |
| LSL64 ACC:P,#(32-Q) | ACC = ACC:P << 32-Q |
| (same as P = ACC:P >> Q) |
| ADDL ACC,@B       | Add B |
| MOVL @Y,ACC       | Result = Y = _{IQmpy}(M*X) + B |

7 Cycles

IQmath Approach

It looks like floating-point!

Floating-Point

\[
\text{float } Y, M, X, B; \\
Y = M \times X + B;
\]

Traditional Fix-Point Q

\[
\text{long } Y, M, X, B; \\
Y = ((i64) M \times (i64) X + (i64) B \ll Q)) \gg Q; \\
\]

"IQmath" In C

\[
_{iq} Y, M, X, B; \\
Y = _{IQmpy}(M, X) + B; \\
\]

"IQmath" In C++

\[
_{iq} Y, M, X, B; \\
Y = M \times X + B; \\
\]

"IQmath" code is easy to read!
The basic "IQmath" approach was adopted in the creation of a standard math library for the Texas Instruments TMS320C28x DSP fixed-point processor. This processor contains efficient hardware for performing 32x32 bit multiply, 64-bit shifts (logical and arithmetic) and 32-bit add/subtract operations, which are ideally suited for 32 bit "IQmath".

Some enhancements were made to the basic "IQmath" approach to improve flexibility. They are:

Setting of GLOBAL_Q Parameter Value: Depending on the application, the amount of numerical resolution or dynamic range required may vary. In the linear equation example, we used a Q value of 24 (Q24). There is no reason why any value of Q can't be used. In the "IQmath" library, the user can set a GLOBAL_Q parameter, with a range of 1 to 30 (Q1 to Q30). All functions used in the program will use this GLOBAL_Q value. For example:

```
#define GLOBAL_Q 18 // set in "IQmathLib.h" file
_iq  Y, M, X, B;
Y = _IQmpy(M, X) + B;  // all values are in Q = 18
```

The user can also explicitly specify the Q value to use:

```
#define GLOBAL_Q 20
_iq20 Y, M, X, B;
Y = _IQ20mpy(M, X) + B;  // all values are in Q = 20
```

The Q value must be consistent for all expressions in the same line of code.
IQmath Provides Compatibility Between Floating-Point and Fixed-Point

1) Develop any mathematical function

\[ Y = \_IQmpy(M, X) + B; \]

2) Select math type in IQmathLib.h

\#if MATH_TYPE == IQ_MATH
\#define \_IQmpy(M, X) \_IQmpy(M, X)
\#elseif MATH_TYPE == FLOAT_MATH
\#define \_IQmpy(M, X) (float) M * (float) X + (float) B;
\#endif

3) Compiler automatically converts to:

**Fixed-Point Math Code**

Compile & Run on Fixed-Point
F2803x

**Floating-Point Math Code**

Compile & Run on Floating-Point
F2806x *

All “IQmath” operations have an equivalent floating-point operation

* Can also compile floating-point code on any floating-point compiler (e.g., PC, Matlab, fixed-point w/ RTS lib, etc.)

**Selecting FLOAT_MATH or IQ_MATH Mode:** As was highlighted in the introduction, we would ideally like to be able to have a single source code that can execute on a floating-point or fixed-point target device simply by recompiling the code. The “IQmath” library supports this by setting a mode, which selects either IQ_MATH or FLOAT_MATH. This operation is performed by simply redefining the function in a header file. For example:

\[
\#if \text{MATH\_TYPE} == \text{IQ\_MATH} \\
\#define _IQmpy(M, X) _IQmpy(M, X) \\
\#elseif \text{MATH\_TYPE} == \text{FLOAT\_MATH} \\
\#define _IQmpy(M, X) (float) M * (float) X \\
\#endif
\]

Essentially, the programmer writes the code using the "IQmath" library functions and the code can be compiled for floating-point or "IQmath" operations.
IQmath Library

### IQmath Library: Math & Trig Functions

<table>
<thead>
<tr>
<th>Operation</th>
<th>Floating-Point</th>
<th>“IQmath” in C</th>
<th>“IQmath” in C++</th>
</tr>
</thead>
<tbody>
<tr>
<td>type</td>
<td>float A, B;</td>
<td>_iq A, B;</td>
<td>iq A, B;</td>
</tr>
<tr>
<td>constant</td>
<td>A = 1.2345</td>
<td>A = _IQ(1.2345)</td>
<td>A = IQ(1.2345)</td>
</tr>
<tr>
<td>multiply</td>
<td>A * B</td>
<td>_IQmpy(A, B)</td>
<td>A * B</td>
</tr>
<tr>
<td>divide</td>
<td>A / B</td>
<td>_IQdiv (A, B)</td>
<td>A / B</td>
</tr>
<tr>
<td>add</td>
<td>A + B</td>
<td>A + B</td>
<td>A + B</td>
</tr>
<tr>
<td>subtract</td>
<td>A - B</td>
<td>A - B</td>
<td>A – B</td>
</tr>
<tr>
<td>boolean</td>
<td>&gt;, &gt;=, &lt;, &lt;=, ==,</td>
<td>&gt;, &gt;=, &lt;, &lt;=, ==,</td>
<td>&gt;, &gt;=, &lt;, &lt;=, ==,</td>
</tr>
<tr>
<td>trig and power</td>
<td>sin(A),cos(A)</td>
<td>_IQsin(A), _IQcos(A)</td>
<td>_IQsin(A), _IQcos(A)</td>
</tr>
<tr>
<td>functions</td>
<td>sin(A<em>2pi),cos(A</em>2pi)</td>
<td>_IQsinPU(A), _IQcosPU(A)</td>
<td>_IQsinPU(A), _IQcosPU(A)</td>
</tr>
<tr>
<td></td>
<td>asin(A),acos(A)</td>
<td>_IQasin(A), _IQacos(A)</td>
<td>_IQasin(A), _IQacos(A)</td>
</tr>
<tr>
<td></td>
<td>atan(A),atan2(A,B)</td>
<td>_IQatan(A), _IQatan2(A,B)</td>
<td>_IQatan(A), _IQatan2(A,B)</td>
</tr>
<tr>
<td></td>
<td>sqrt(A),sqrt(A*B)</td>
<td>_IQsqrt(A), _IQsqrt(A*B)</td>
<td>_IQsqrt(A), _IQsqrt(A*B)</td>
</tr>
<tr>
<td></td>
<td>exp(A)</td>
<td>_IQexp(A)</td>
<td>_IQexp(A)</td>
</tr>
<tr>
<td>saturation</td>
<td>if(A &gt; Pos) A = Pos</td>
<td>_IQsat(A,Pos,Neg)</td>
<td>IQsat(A,Pos,Neg)</td>
</tr>
<tr>
<td></td>
<td>if(A &lt; Neg) A = Neg</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Accuracy of functions/operations approx ~28 to ~31 bits

Additionally, the "IQmath" library contains DSP library modules for filters (FIR & IIR) and Fast Fourier Transforms (FFT & IFFT).

### IQmath Library: Conversion Functions

<table>
<thead>
<tr>
<th>Operation</th>
<th>Floating-Point</th>
<th>“IQmath” in C</th>
<th>“IQmath” in C++</th>
</tr>
</thead>
<tbody>
<tr>
<td>iq to iqN</td>
<td>A</td>
<td>_IQtoQ(N)A</td>
<td>IQtoQ(N)A</td>
</tr>
<tr>
<td>iqN to iq</td>
<td>A</td>
<td>_IQNtoIQ(A)</td>
<td>IQNtoIQ(A)</td>
</tr>
<tr>
<td>integer(iq)</td>
<td>(long) A</td>
<td>_IQint(A)</td>
<td>IQint(A)</td>
</tr>
<tr>
<td>fraction(iq)</td>
<td>A – (long) A</td>
<td>_IQfrac(A)</td>
<td>IQfrac(A)</td>
</tr>
<tr>
<td>iq = iq*long</td>
<td>A * (float) B</td>
<td>_IQmpy32(A,B)</td>
<td>IQmpy32(A,B)</td>
</tr>
<tr>
<td>integer(iq)*long</td>
<td>(long) (A * (float) B)</td>
<td>_IQmpy32int(A,B)</td>
<td>IQmpy32int(A,B)</td>
</tr>
<tr>
<td>fraction(iq)*long</td>
<td>A - (long) (A * (float) B)</td>
<td>_IQmpy32frac(A,B)</td>
<td>IQmpy32frac(A,B)</td>
</tr>
<tr>
<td>qN to iq</td>
<td>A</td>
<td>_QNtoIQ(A)</td>
<td>QNtoIQ(A)</td>
</tr>
<tr>
<td>iq to qN</td>
<td>A</td>
<td>_IQtoQ(N)A</td>
<td>IQtoQ(N)A</td>
</tr>
<tr>
<td>string to iq</td>
<td>atof(char)</td>
<td>_atolQ(char)</td>
<td>atolQ(char)</td>
</tr>
<tr>
<td>IQ to float</td>
<td>A</td>
<td>_IQtoF(A)</td>
<td>IQtoF(A)</td>
</tr>
<tr>
<td>IQ to ASCII</td>
<td>sprintf(A,B,C)</td>
<td>_IQtoA(A,B,C)</td>
<td>IQtoA(A,B,C)</td>
</tr>
</tbody>
</table>

IQmath.lib > contains library of math functions
IQmathLib.h > C header file
IQmathCPP.h > C++ header file
16 vs. 32 Bits
The "IQmath" approach could also be used on 16-bit numbers and for many problems, this is sufficient resolution. However, in many control cases, the user needs to use many different "Q" values to accommodate the limited resolution of a 16-bit number.

With DSP devices like the TMS320C28x processor, which can perform 16-bit and 32-bit math with equal efficiency, the choice becomes more of productivity (time to market). Why bother spending a whole lot of time trying to code using 16-bit numbers when you can simply use 32-bit numbers, pick one value of "Q" that will accommodate all cases and not worry about spending too much time optimizing.

Of course there is a concern on data RAM usage if numbers that could be represented in 16 bits all use 32 bits. This is becoming less of an issue in today's processors because of the finer technology used and the amount of RAM that can be cheaply integrated. However, in many cases, this problem can be mitigated by performing intermediate calculations using 32-bit numbers and converting the input from 16 to 32 bits and converting the output back to 16 bits before storing the final results. In many problems, it is the intermediate calculations that require additional accuracy to avoid quantization problems.
Converting ADC Results into IQ Format

As you may recall, the converted values of the ADC are placed in the lower 12 bits of the ADCRESULT0 register. Before these values are filtered using the IQmath library, they need to be put into the IQ format as a 32-bit long. For uni-polar ADC inputs (i.e., 0 to 3.3 V inputs), a conversion to global IQ format can be achieved with:

\[
\text{IQresult\_unipolar} = \text{IQmpy}(\text{IQ}(3.3), \text{IQ12toIQ}((\text{iq}) \text{AdcResult.ADCRESULT0}))
\]

How can we modify the above to recover bi-polar inputs, for example +1.65 volts? One could do the following to offset the +1.65V analog biasing applied to the ADC input:

\[
\text{IQresult\_bipolar} = \text{IQmpy}(\text{IQ}(3.3), \text{IQ12toIQ}((\text{iq}) \text{AdcResult.ADCRESULT0}) - \text{IQ}(1.65))
\]

However, one can see that the largest intermediate value the equation above could reach is 3.3. This means that it cannot be used with an IQ data type of IQ30 (IQ30 range is \(-2 < x < -2\)). Since the IQmath library supports IQ types from IQ1 to IQ30, this could be an issue in some applications.

The following clever approach supports IQ types from IQ1 to IQ30:

\[
\text{IQresult\_bipolar} = \text{IQmpy}(\text{IQ}(1.65), \text{IQ15toIQ}((\text{iq}) \text{(int16)} (\text{AdcResult.ADCRESULT0} ^ \text{0x8000})))
\]

The largest intermediate value that this equation could reach is 1.65. Therefore, IQ30 is easily supported.
#if MATH_TYPE == IQ_MATH
#define AdcFsVoltage  _IQ(3.3)           // ADC full scale voltage
#else     // MATH_TYPE is FLOAT_MATH
#define AdcFsVoltage  _IQ(3.3/4096.0)    // ADC full scale voltage
#endif

_iq Result;                                   // ADC result

void main(void)
{
    Result = _IQmpy(AdcFsVoltage, _IQ12toIQ( (_iq)AdcResult.ADCRESULT0));
}

FLOAT_MATH behavior: * does nothing float
The "IQmath" approach is ideally suited for applications where a large numerical dynamic range is not required. Motor control is an example of such an application (audio and communication algorithms are other applications). As an example, the IQmath approach has been applied to the sensor-less direct field control of an AC induction motor. This is probably one of the most challenging motor control problems and as will be shown later, requires numerical accuracy greater than 16-bits in the control calculations.

The above slide is a block diagram representation of the key control blocks and their interconnections. Essentially this system implements a "Forward Control" block for controlling the d-q axis motor current using PID controllers and a "Feedback Control" block using back emf's integration with compensated voltage from current model for estimating rotor flux based on current and voltage measurements. The motor speed is simply estimated from rotor flux differentiation and open-loop slip computation. The system was initially implemented on a "Simulator Test Bench" which uses a simulation of an "AC Induction Motor Model" in place of a real motor. Once working, the system was then tested using a real motor on an appropriate hardware platform.

Each individual block shown in the slide exists as a stand-alone C/C++ module, which can be interconnected to form the complete control system. This modular approach allows reusability and portability of the code. The next few slides show the coding of one particular block, PARK Transform, using floating-point and "IQmath" approaches in C:
The complete system was coded using "IQmath". Based on analysis of coefficients in the system, the largest coefficient had a value of 33.3333. This indicated that a minimum dynamic range of 7 bits (+/-64 range) was required. Therefore, this translated to a GLOBAL_Q value of 32-7 = 25 (Q25). Just to be safe, the initial simulation runs were conducted with GLOBAL_Q = 24 (Q24).
value. The plots start from a step change in reference speed from 0.0 to 0.5 and 1024 samples are taken.

![AC Induction Motor Example](image)

```
GLOBAL_Q = 24, system stable
```

The speed eventually settles to the desired reference value and the stator current exhibits a clean and stable oscillation. The block diagram slide shows at which points in the control system the plots are taken from.

![What’s Happening Here?](image)

```
What’s Happening Here?
Equal Precision in the Computation Region
```

Floating-Point:

I8Q24 Fractions:

In the region where these particular computations occur, the precision of single-precision floating-point just happens to equal the precision of the I8Q24 format.

So, both produce similar results!
AC Induction Motor Example
GLOBAL_Q = 27, system unstable

AC Induction Motor Example
GLOBAL_Q = 16, system unstable
With the ability to select the GLOBAL_Q value for all calculations in the "IQmath", an experiment was conducted to see what maximum and minimum Q value the system could tolerate before it became unstable. The results are tabulated in the slide below:

<table>
<thead>
<tr>
<th>Q range</th>
<th>Stability Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q31 to Q27</td>
<td>Unstable (not enough dynamic range)</td>
</tr>
<tr>
<td>Q26 to Q19</td>
<td>Stable</td>
</tr>
<tr>
<td>Q18 to Q0</td>
<td>Unstable (not enough resolution, quantization problems)</td>
</tr>
</tbody>
</table>

The developer must pick the right GLOBAL_Q value!

The above indicates that, the AC induction motor system that we simulated requires a minimum of 7 bits of dynamic range (+/-64) and requires a minimum of 19 bits of numerical resolution (+/-0.000002). This confirms our initial analysis that the largest coefficient value being 33.33333 required a minimum dynamic range of 7 bits. As a general guideline, users using IQmath should examine the largest coefficient used in the equations and this would be a good starting point for setting the initial GLOBAL_Q value. Then, through simulation or experimentation, the user can reduce the GLOBAL_Q until the system resolution starts to cause instability or performance degradation. The user then has a maximum and minimum limit and a safe approach is to pick a midpoint.

What the above analysis also confirms is that this particular problem does require some calculations to be performed using greater than 16 bit precision. The above example requires a minimum of 7 + 19 = 26 bits of numerical accuracy for some parts of the calculations. Hence, if one was implementing the AC induction motor control algorithm using a 16 bit fixed-point DSP, it would require the implementation of higher precision math for certain portions. This would take more cycles and programming effort.

The great benefit of using GLOBAL_Q is that the user does not necessarily need to go into details to assign an individual Q for each variable in a whole system, as is typically done in conventional fixed-point programming. This is time consuming work. By using 32-bit resolution and the "IQmath" approach, the user can easily evaluate the overall resolution and quickly implement a typical digital motor control application without quantization problems.
### AC Induction Motor Example

**Performance comparisons**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>C28x C (150 MHz)</th>
<th>C28x C (150 MHz)</th>
<th>C28x C (150 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1: ACI module cycles</td>
<td>401</td>
<td>401</td>
<td>625</td>
</tr>
<tr>
<td>B2: Feedforward control cycles</td>
<td>421</td>
<td>371</td>
<td>403</td>
</tr>
<tr>
<td>B3: Feedback control cycles</td>
<td>2336</td>
<td>792</td>
<td>1011</td>
</tr>
<tr>
<td>Total control cycles (B2+B3)</td>
<td>2757</td>
<td>1163</td>
<td>1414</td>
</tr>
<tr>
<td>% of available MHz used (20 kHz control loop)</td>
<td>36.8%</td>
<td>15.5%</td>
<td>18.9%</td>
</tr>
</tbody>
</table>

Notes: C28x compiled on codegen tools v5.0.0, -g (debug enabled), -o3 (max. optimization)
fast RTS lib v1.0beta1
IQmath lib v1.4d

Using the profiling capabilities of the respective DSP tools, the table above summarizes the number of cycles and code size of the forward and feedback control blocks.

The MIPS used is based on a system sampling frequency of 20 kHz, which is typical of such systems.
The IQmath approach, matched to a fixed-point processor with 32x32 bit capabilities enables the following:

- Seamless portability of code between fixed and floating-point devices
- Maintenance and support of one source code set from simulation to target device
- Adjustability of numerical resolution (Q value) based on application requirement
- Implementation of systems that may otherwise require floating-point device
- Rapid conversion/porting and implementation of algorithms
Lab 8: IQmath FIR Filter

Objective

The objective of this lab is to become familiar with IQmath programming. In the previous lab, ePWM1A was setup to generate a 2 kHz, 25% duty cycle symmetric PWM waveform. The waveform was then sampled with the on-chip analog-to-digital converter. In this lab the sampled waveform will be passed through an FIR filter and displayed using the graphing feature of Code Composer Studio. The filter math type is selected in the “IQmathLib.h” file.

Procedure

Open the Project

1. A project named Lab8 has been created for this lab. Open the project by clicking on Project ➔ Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab8\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:
Project Build Options

2. To configure the build options, right-click on Lab8 in the Project Explorer window and select Properties. We need to setup the include search path to include the IQmath header file. Under “C2000 Compiler” select “Include Options”. In the lower box that opens (“Add dir to #include search path”) click the Add icon (first icon with green plus sign). Then in the “Add directory path” window type:

```
$(PROJECT_ROOT)/../../IQmath/include
```

Click OK to include the search path.

3. Next, we need to setup the library search path to include the IQmath library. Under “C2000 Linker” select “File Search Path”. In the top box (“Include library file or command file as input”) click the Add icon. Then in the “Add file path” window type:

```
IQmath.lib
```

Click OK to include the library file.

In the bottom box (“Add <dir> to library search path”) click the Add icon. In the “Add directory path” window type:

```
$(PROJECT_ROOT)/../../IQmath/lib
```

Click OK to include the library search path.

Finally, select OK to save and close the Properties window.

Include IQmathLib.h

4. In the Project Explorer window edit Lab.h and uncomment the line that includes the IQmathLib.h header file. Next, in the Function Prototypes section, uncomment the function prototype for IQssfir(), the IQ math single-sample FIR filter function. In the Global Variable References section uncomment the four _iq references. Save the changes and close the file.

Inspect Lab_8.cmd

5. Open and inspect Lab_8.cmd. First, notice that a section called “IQmath” is being linked to L4SARAM. The IQmath section contains the IQmath library functions (code). Second, notice that a section called “IQmathTables” is being linked to the

Lab 8: IQmath FIR Filter

Adc.c        Filter.c
CodeStartBranch.asm        Gpio.c
DefaultIsr_8.c        Lab.h
DelayUs.asm        Lab_8.cmd
ECap_7_8_9_10_12.c        Main_8.c
EPwm_7_8_9_10_12.c        PieCtrl.c
F2806x_DefaultIsr.h        PieVect.c
F2806x_GlobalVariableDefs.c        SysCtrl.c
F2806x_Headers_nonBIOS.cmd        Watchdog.c
IQTABLES with a TYPE = NOLOAD modifier after its allocation. The IQmath tables are used by the IQmath library functions. The NOLOAD modifier allows the linker to resolve all addresses in the section, but the section is not actually placed into the .out file. This is done because the section is already present in the device ROM (you cannot load data into ROM after the device is manufactured!). The tables were put in the ROM by TI when the device was manufactured. All we need to do is link the section to the addresses where it is known to already reside (the tables are the very first thing in the BOOT ROM, starting at address 0x3F8000). Close the inspected file.

Select a Global IQ value

6. In the Project Explorer window under the Includes folder open: C:\C28x\Labs\IQmath\include\IQmathLib.h. Confirm that the GLOBAL_Q type (near beginning of file) is set to a value of 24. If it is not, modify as necessary:

```
#define GLOBAL_Q 24
```

Recall that this Q type will provide 8 integer bits and 24 fractional bits. Dynamic range is therefore \(-128 \leq x \leq +128\), which is sufficient for our purposes in the workshop.

Notice that the math type is defined as IQmath by:

```
#define MATH_TYPE IQ_MATH
```

Close the file.

IQmath Single-Sample FIR Filter

7. Open and inspect DefaultIsr_8.c. Notice that the ADCINT1_ISR calls the IQmath single-sample FIR filter function, IQssfir(). The filter coefficients have been defined in the beginning of Main_8.c. Also, as discussed in the lecture for this module, the ADC results are read with the following instruction:

```
*AdcBufIQPtr = _IQmpy(ADC_FS_VOLTAGE, _IQ12toIQ((__iq)AdcResult.ADCRESULT0));
```

The value of ADC_FS_VOLTAGE will be discussed in the next lab step.

8. Open and inspect Lab.h. Notice that, as discussed in the lecture for this module, ADC_FS_VOLTAGE is defined as:

```
#if MATH_TYPE == IQ_MATH
    #define ADC_FS_VOLTAGE _IQ(3.3)
#else // MATH_TYPE is FLOAT_MATH
    #define ADC_FS_VOLTAGE _IQ(3.3/4096.0)
#endif
```

9. Open and inspect the IQssfir() function in Filter.c. This is a simple, non-optimized coding of a basic IQmath single-sample FIR filter. Close the inspected files.

Build and Load

10. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.
11. Click the “Debug” button (green bug). The “CCS Debug Perspective” view should open, the program will load automatically, and you should now be at the start of `main()`. If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to EMU_BOOT_SARAM using the Scripts menu.

### Run the Code – Filtered Waveform

12. Open a memory browser to view some of the contents of the filtered ADC results buffer. The address label for the filtered ADC results buffer is `AdcBufFilteredIQ` in the “Data” memory page. Set the format to `32-Bit Signed Integer`. Right-click in the memory window, select `Configure…` and set the Q-Value to `24` (which matches the IQ format being used for this variable). Then click **OK** to save the setting. We will be running our code in real-time mode, and will need to have the window continuously refresh.

**Note:** For the next step, check to be sure that the jumper wire connecting PWM1A (pin # GPIO-00) to ADCINA0 (pin # ADC-A0) is in place on the Docking Station.

13. Run the code in real-time mode using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset, and watch the memory browser update. Verify that the ADC result buffer contains updated values.

14. Open and setup a dual-time graph to plot a 50-point window of the filtered and unfiltered ADC results buffer. Click: Tools → Graph → Dual Time and set the following values:

<table>
<thead>
<tr>
<th>Acquisition Buffer Size</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Data Type</td>
<td>32-bit signed integer</td>
</tr>
<tr>
<td>Q Value</td>
<td>24</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address A</td>
<td>AdcBufFilteredIQ</td>
</tr>
<tr>
<td>Start Address B</td>
<td>AdcBufIQ</td>
</tr>
<tr>
<td>Display Data Size</td>
<td>50</td>
</tr>
<tr>
<td>Time Display Unit</td>
<td>μs</td>
</tr>
</tbody>
</table>

Select **OK** to save the graph options.

15. The graphical display should show the generated FIR filtered 2 kHz, 25% duty cycle symmetric PWM waveform in the Dual Time A display and the unfiltered waveform generated in the previous lab exercise in the Dual Time B display. Notice the shape and phase differences between the waveform plots (the filtered curve has rounded edges, and lags the unfiltered plot by several samples). The amplitudes of both plots should run from 0 to 3.3.
16. Open and setup two (2) frequency domain plots – one for the filtered and another for the unfiltered ADC results buffer. Click: Tools → Graph → FFT Magnitude and set the following values:

<table>
<thead>
<tr>
<th></th>
<th>GRAPH #1</th>
<th>GRAPH #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Buffer Size</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>DSP Data Type</td>
<td>32-bit signed integer</td>
<td>32-bit signed integer</td>
</tr>
<tr>
<td>Q Value</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address</td>
<td>AdcBufFilteredIQ</td>
<td>AdcBufIQ</td>
</tr>
<tr>
<td>Data Plot Style</td>
<td>Bar</td>
<td>Bar</td>
</tr>
<tr>
<td>FFT Order</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

Select OK to save the graph options.

17. The graphical displays should show the frequency components of the filtered and unfiltered 2 kHz, 25% duty cycle symmetric PWM waveforms. Notice that the higher frequency components are reduced using the Low-Pass FIR filter in the filtered graph as compared to the unfiltered graph.

18. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

**Changing Math Type to Floating-Point**

19. Switch to the “CCS Edit Perspective” view by clicking the CCS Edit icon in the upper right-hand corner. In the Project Explorer window under the Includes folder open: C:\C28x\Labs\IQmath\include\IQmathLib.h. Edit IQmathLib.h to define the math type as floating-point. Change #define

```
#define   MATH_TYPE      IQ_MATH
```

To:

```
#define   MATH_TYPE      FLOAT_MATH
```

Save the change to the IQmathLib.h and close the file.

**Build and Load**

20. Click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.
Run the Code – Floating-Point Filtered Waveform

21. Change the dual-time and FFT Magnitude graphs to display 32-bit floating-point rather than 32-bit signed integer. Click the “Show the Graph Properties” icon for each graph and change the DSP Data Type to 32-bit floating-point.

22. Run the code (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset.

23. The graphical display should show the generated FIR filtered 2 kHz, 25% duty cycle symmetric PWM waveform in the Dual Time A display and the unfiltered waveform in the Dual Time B display. The FFT Magnitude graphical displays should show the frequency components of the filtered and unfiltered 2 kHz, 25% duty cycle symmetric PWM waveforms.

24. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

Terminate Debug Session and Close Project

25. Terminate the active debug session using the Terminate button. This will close the debugger and return CCS to the “CCS Edit Perspective” view.

26. Next, close the project by right-clicking on Lab8 in the Project Explorer window and select Close Project.

End of Exercise
Lab 8 Reference: Low-Pass FIR Filter

Bode Plot of Digital Low Pass Filter

Coefficients: [1/16, 4/16, 6/16, 4/16, 1/16]

Sample Rate: 50 kHz
Direct Memory Access Controller

Introduction

This module explains the operation of the direct memory access (DMA) controller. The DMA provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thus freeing up bandwidth for other system functions. The DMA has six channels with independent PIE interrupts.

Module Objectives

◆ Understand the operation of the Direct Memory Access (DMA) controller
◆ Show how to use the DMA to transfer data between peripherals and/or memory without intervention from the CPU

The DMA allows data to be transferred between peripherals and/or memory without intervention from the CPU. The DMA can read data from the ADC result registers, transfer to or from memory blocks L5 through L8, transfer to or from the McBSP, and also modify registers in the ePWM. Triggers are used to initiate the transfers, and when completed the DMA can generate an interrupt.
Module Topics

Direct Memory Access Controller ............................................................................................................9-1

Module Topics..........................................................................................................................................9-2

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DMA Examples...................................................................................................................................9-6
DMA Priority Modes...........................................................................................................................9-8
DMA Throughput.................................................................................................................................9-9
DMA Registers..................................................................................................................................9-10

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Direct Memory Access (DMA)

DMA Triggers, Sources, and Destinations

- ADC Result 0-15
- McBSP-A
- L5 DPSARAM
- L6 DPSARAM
- L7 DPSARAM
- L8 DPSARAM

DMA 6-channels

Triggers

- ADCINT1 / ADCINT2
- MXEVTA / MREVTA
- XINT1-3 / TINT0-2
- ePWM1-6 (SOCA-B)
- USB0EP1-3RX/TX
- software

SysCtrlRegs.EPWMCNF.bit.CONCNF
(map ePWM to DMA bus or CLA bus)

DMA Definitions

- **Word**
  - 16 or 32 bits
  - Word size is configurable per DMA channel

- **Burst**
  - Consists of multiple words
  - Smallest amount of data transferred at one time

- **Burst Size**
  - Number of words per burst
  - Specified by BURST_SIZE register
    - 5-bit ‘N-1’ value (maximum of 32 words/burst)

- **Transfer**
  - Consists of multiple bursts

- **Transfer Size**
  - Number of bursts per transfer
  - Specified by TRANSFER_SIZE register
    - 16-bit ‘N-1’ value - exceeds any practical requirements
Basic Operation

Simplified State Machine Operation
The DMA state machine at its most basic level is two nested loops

Start Transfer

Move Word

Burst Size times

Transfer Size times

End Transfer

DMA can be configured to re-initialize at the end of the transfer (continuous mode)

Basic Address Control Registers

Active pointers

SRC_ADDR

DST_ADDR

Pointer shadow registers copied to active pointers at start of transfer

SRC_ADDR_SHADOW

DST_ADDR_SHADOW

Signed value added to active pointer after each word

SRC_BURST_STEP

DST_BURST_STEP

Signed value added to active pointer after each burst

SRC_TRANSFER_STEP

DST_TRANSFER_STEP
Simplified State Machine Example

3 words/burst
2 bursts/transfer

Start Transfer

Wait for event to start/continue transfer

Read/Write Data

Moved “Burst Size” Words?

Add Burst Step to Address Pointer

Moved “Transfer Size” Bursts?

Add Transfer Step to Address Pointer

End Transfer

DMA Interrupts

Mode #1: Interrupt at start of transfer

- Each DMA channel has its own PIE interrupt
- The mode for each interrupt can be configured individually
- The CHINTMODE bit in the MODE register selects the interrupt mode

Mode #2: Interrupt at end of transfer

Start Transfer

Wait for event to start/continue transfer

Read/Write Data

Moved “Burst Size” Words?

Add Burst Step to Address Pointer

Moved “Transfer Size” Bursts?

Add Transfer Step to Address Pointer

End Transfer
### DMA Examples

#### Simple Example

**Objective:** Move 4 words from memory location 0xF000 to memory location 0x4000 and interrupt CPU at end of transfer

- **BURST_SIZE** = 0x1111 (2 words/burst)
- **TRANSFER_SIZE** = 0x2222 (2 bursts/transfer)

* Size registers are N-1

<table>
<thead>
<tr>
<th>Addr</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xF000</td>
<td>0HandlerContext</td>
</tr>
<tr>
<td>0xF001</td>
<td>0HandlerContext</td>
</tr>
<tr>
<td>0xF002</td>
<td>0HandlerContext</td>
</tr>
<tr>
<td>0xF003</td>
<td>0HandlerContext</td>
</tr>
<tr>
<td>0xF004</td>
<td>0HandlerContext</td>
</tr>
</tbody>
</table>

**Source Registers**
- **SRC_ADDR** = 0x00000000
- **SRC_ADDR_SHADOW** = 0x00000000
- **SRC_BURST_STEP** = 0x0001
- **SRC_TRANSFER_STEP** = 0x0001

**Destination Registers**
- **DST_ADDR** = 0x00004000
- **DST_ADDR_SHADOW** = 0x00004000
- **DST_BURST_STEP** = 0x0001
- **DST_TRANSFER_STEP** = 0x0001

**Note:** This example could also have been done using 1 word/burst and 4 bursts/transfer, or 4 words/burst and 1 burst/transfer. This would affect Round-Robin progression, but not interrupts.

#### Data Binning Example

**Objective:** Bin 3 samples of 5 ADC channels, then interrupt the CPU

**ADC Results**

<table>
<thead>
<tr>
<th>3rd Conversion Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0B00</td>
</tr>
<tr>
<td>0x0B01</td>
</tr>
<tr>
<td>0x0B02</td>
</tr>
<tr>
<td>0x0B03</td>
</tr>
<tr>
<td>0x0B04</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>L7 SARAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH0</td>
</tr>
<tr>
<td>CH0</td>
</tr>
<tr>
<td>CH0</td>
</tr>
<tr>
<td>CH0</td>
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<tr>
<td>CH0</td>
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<td>CH1</td>
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<td>CH4</td>
</tr>
<tr>
<td>CH4</td>
</tr>
<tr>
<td>CH4</td>
</tr>
</tbody>
</table>

**Interrupt to PIE**
Data Binning Example Register Setup

**Objective:** Bin 3 samples of 5 ADC channels, then interrupt the CPU

**ADC Registers:**
SOC0 – SOC4 configured to CH0 – CH4, respectively.
ADC configured to re-trigger (continuous conversion)

**DMA Registers:**

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>BURST_SIZE*</td>
<td>0x0004</td>
<td>5 words/burst</td>
</tr>
<tr>
<td>TRANSFER_SIZE*</td>
<td>0x0002</td>
<td>3 bursts/transfer</td>
</tr>
<tr>
<td>SRC_ADDR_SHADOW</td>
<td>0x00000000</td>
<td></td>
</tr>
<tr>
<td>SRC_BURST_STEP</td>
<td>0x0001</td>
<td></td>
</tr>
<tr>
<td>SRC_TRANSFER_STEP</td>
<td>0xFFF (-4)</td>
<td></td>
</tr>
<tr>
<td>DST_ADDR_SHADOW</td>
<td>0x0000F000</td>
<td>Starting address**</td>
</tr>
<tr>
<td>DST_BURST_STEP</td>
<td>0x0B02</td>
<td></td>
</tr>
<tr>
<td>DST_TRANSFER_STEP</td>
<td>0xFFF (-11)</td>
<td></td>
</tr>
</tbody>
</table>

* Size registers are N-1
** Typically use a relocatable symbol in your code, not a hard value

---

Ping-Pong Buffer Example

**Objective:** Buffer ADC ch. 0 ping-pong style, 50 samples per buffer

**ADC Result Register**
0xFB00
SOC0 configured to ADCINA0
with 1 conversion per trigger

**L5 DPSARAM**
0xC140

50 word ‘Ping’ buffer
DMA Interrupt

50 word ‘Pong’ buffer
DMA Interrupt
Ping-Pong Example Register Setup

**Objective:** Buffer ADC ch. 0 ping-pong style, 50 samples per buffer

**ADC Registers:**
Convert ADC Channel ADCINA0 – 1 conversion per trigger (i.e. ePWM2SOCA)

**DMA Registers:**
- **BURST_SIZE**
  - 0x0000: 1 word/burst
  - 0x0031: 50 bursts/transfer
- **TRANSFER_SIZE**
- **SRC_ADDR_SHADOW**
  - 0x0000: starting address
  - 0x00000B00: since BURST_SIZE = 0
  - 0x00000C140: starting address**
  - 0x0000B001: since BURST_SIZE = 0
- **SRC_BURST_STEP**
  - don't care
- **SRC_TRANSFER_STEP**
- **DST_ADDR_SHADOW**
- **DST_BURST_STEP**
  - don't care
- **DST_TRANSFER_STEP**
  - 0x0051

**Other:** DMA configured to re-init after transfer (CONTINUOUS = 1)

* Size registers are N-1
** DST_ADDR_SHADOW must be changed between ping and pong buffer address in the DMA ISR. Typically use a relocatable symbol in your code, not a hard value.

### DMA Priority Modes

#### Channel Priority Modes

- **Round Robin Mode:**
  - All channels have equal priority
  - After each enabled channel has transferred a burst of words, the next enabled channel is serviced in round robin fashion

- **Channel 1 High Priority Mode:**
  - Same as Round Robin except CH1 can interrupt DMA state machine
  - If CH1 trigger occurs, the current word (not the complete burst) on any other channel is completed and execution is halted
  - CH1 is serviced for complete burst
  - When completed, execution returns to previous active channel
  - This mode is intended primarily for the ADC, but can be used by any DMA event configured to trigger CH1
**Priority Modes and the State Machine**

**DMA Throughput**

- **4 cycles/word** (5 for McBSP reads)
- **1 cycle delay to start each burst**
- **1 cycle delay returning from CH1 high priority interrupt**
- **32-bit transfer doubles throughput**
  (except McBSP, which supports 16-bit transfers only)

**Example: 128 16-bit words from ADC to RAM**
8 bursts * [(4 cycles/word * 16 words/burst) + 1] = 520 cycles

**Example: 64 32-bit words from ADC to RAM**
8 bursts * [(4 cycles/word * 8 words/burst) + 1] = 264 cycles
**DMA vs. CPU Access Arbitration**

- **DMA has priority over CPU**
  - If a multi-cycle CPU access is already in progress, DMA stalls until current CPU access finishes
  - The DMA will interrupt back-to-back CPU accesses

- **Can the CPU be locked out?**
  - Generally No!
  - DMA is multi-cycle transfer; CPU will sneak in an access when the DMA is accessing the other end of the transfer (e.g. while DMA accesses destination location, the CPU can access the source location)

### DMA Registers

**DmaRegs**

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMACTRL</td>
<td>DMA Control Register</td>
</tr>
<tr>
<td>PRIORITYCTRL1</td>
<td>Priority Control Register 1</td>
</tr>
<tr>
<td>MODE</td>
<td>Mode Register</td>
</tr>
<tr>
<td>CONTROL</td>
<td>Control Register</td>
</tr>
<tr>
<td>BURST_SIZE</td>
<td>Burst Size Register</td>
</tr>
<tr>
<td>BURST_COUNT</td>
<td>Burst Count Register</td>
</tr>
<tr>
<td>SRC_BURST_STEP</td>
<td>Source Burst Step Size Register</td>
</tr>
<tr>
<td>DST_BURST_STEP</td>
<td>Destination Burst Step Size Register</td>
</tr>
<tr>
<td>TRANSFER_SIZE</td>
<td>Transfer Size Register</td>
</tr>
<tr>
<td>TRANSFER_COUNT</td>
<td>Transfer Count Register</td>
</tr>
<tr>
<td>SRC_TRANSFER_STEP</td>
<td>Source Transfer Step Size Register</td>
</tr>
<tr>
<td>DST_TRANSFER_STEP</td>
<td>Destination Transfer Step Size Register</td>
</tr>
<tr>
<td>SRC_ADDR_SHADOW</td>
<td>Shadow Source Address Pointer Register</td>
</tr>
<tr>
<td>SRC_ADDR</td>
<td>Active Source Address Pointer Register</td>
</tr>
<tr>
<td>DST_ADDR_SHADOW</td>
<td>Shadow Destination Address Pointer Register</td>
</tr>
<tr>
<td>DST_ADDR</td>
<td>Active Destination Address Pointer Register</td>
</tr>
</tbody>
</table>

For a complete list of registers refer to the DMA Module Reference Guide
DMA Control Register
DmaRegs.DMACTRL

**Hard Reset**
0 = writes ignored (always reads back 0)
1 = reset DMA module

**Priority Reset**
0 = writes ignored (always reads back 0)
1 = reset state-machine after any pending burst transfer complete

Priority Control Register 1
DmaRegs.PRIORITYCTRL1

**DMA CH1 Priority**
0 = same priority as other channels
1 = highest priority channel
Direct Memory Access (DMA)

**Mode Register**

**Upper Register:**

- **Channel Interrupt**
  - 0 = disable
  - 1 = enable

- **One Shot Mode**
  - 0 = DMA stops
  - 1 = DMA re-initializes

- **Data Size Mode**
  - 0 = 16-bit transfer
  - 1 = 32-bit transfer

**Lower Register:**

- **Channel Interrupt Generation**
  - 0 = at beginning of transfer
  - 1 = at end of transfer

- **Peripheral Interrupt Trigger**
  - 0 = disable
  - 1 = enable

- **Overflow Interrupt Enable**
  - 0 = disable
  - 1 = enable

- **Peripheral Interrupt Source Select**

<table>
<thead>
<tr>
<th>Peripheral INT</th>
<th>Peripheral INT</th>
<th>Peripheral INT</th>
<th>Peripheral INT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 none</td>
<td>8 USB0EP1TX</td>
<td>16 reserved</td>
<td>24 ePWM4SOCB</td>
</tr>
<tr>
<td>1 ADCINT1</td>
<td>9 USB0EP2RX</td>
<td>17 Reserved</td>
<td>25 ePWM4SOCB</td>
</tr>
<tr>
<td>2 ADCINT2</td>
<td>10 USB0EP2TX</td>
<td>18 ePWM1SOCA</td>
<td>26 ePWM5SOCA</td>
</tr>
<tr>
<td>3 XINT1</td>
<td>11 TINT0</td>
<td>19 ePWM1SOCB</td>
<td>27 ePWM5SOCB</td>
</tr>
<tr>
<td>4 XINT2</td>
<td>12 TINT1</td>
<td>20 ePWM2SOCA</td>
<td>28 ePWM6SOCA</td>
</tr>
<tr>
<td>5 XINT3</td>
<td>13 TINT2</td>
<td>21 ePWM2SOCB</td>
<td>29 ePWM6SOCB</td>
</tr>
<tr>
<td>6 reserved</td>
<td>14 MXEVTA</td>
<td>22 ePWM3SOCA</td>
<td>30 USB0EP3RX</td>
</tr>
<tr>
<td>7 USB0EP1RX</td>
<td>15 MREVTA</td>
<td>23 ePWM3SOCB</td>
<td>31 USB0EP3TX</td>
</tr>
</tbody>
</table>
Lab 9: Servicing the ADC with DMA

Objective

The objective of this lab is to become familiar with operation of the DMA. In the previous lab, the CPU was used to store the ADC conversion result in the memory buffer during the ADC ISR. In this lab the DMA will be configured to transfer the results directly from the ADC result registers to the memory buffer. ADC channel A0 will be buffered ping-pong style with 50 samples per buffer. As an operational test, the filtered 2 kHz, 25% duty cycle symmetric PWM waveform (ePWM1A) will be displayed using the graphing feature of Code Composer Studio.

Procedure

Open the Project

1. A project named Lab9 has been created for this lab. Open the project by clicking on Project → Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab9\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:
Inspect Lab_9.cmd

2. Open and inspect Lab_9.cmd. Notice that a section called “dmaMemBufs” is being linked to L5DPSARAM. This section links the destination buffer for the DMA transfer to a DMA accessible memory space.

Setup DMA Initialization

The DMA controller needs to be configured to buffer ADC channel A0 ping-pong style with 50 samples per buffer. One conversion will be performed per trigger with the ADC operating in single sample mode.

3. Edit Dma.c to implement the DMA operation as described in the objective for this lab exercise. Configure the DMA Channel 1 Mode Register (MODE) so that the ADC ADCINT1 is the peripheral interrupt source. Enable the peripheral interrupt trigger and set the channel for interrupt generation at the start of transfer. Configure for 16-bit data transfers with one burst per trigger and auto re-initialization at the end of the transfer. In the DMA Channel 1 Control Register (CONTROL) clear the error and peripheral interrupt bits. Enable the channel to run.

4. Open Main_9.c and add a line of code in main() to call the InitDma() function. There are no passed parameters or return values. You just type

   InitDma();

   at the desired spot in main().

Setup PIE Interrupt for DMA

Recall that ePWM2 is triggering the ADC at a 50 kHz rate. In the previous lab exercise, the ADC generated an interrupt to the CPU, and the CPU implemented the FIR filter in the ADC ISR. For this lab exercise, the ADC is instead triggering the DMA, and the DMA will generate an interrupt to the CPU. The CPU will implement the FIR filter in the DMA ISR.

5. Edit Adc.c to comment out the code used to enable the ADCINT1 interrupt in PIE group 1. This is no longer being used. The DMA interrupt will be used instead.

6. Using the “PIE Interrupt Assignment Table” find the location for the DMA Channel 1 interrupt “DINTCH1” and fill in the following information:

   PIE group #:__________  # within group:__________
This information will be used in the next step.

7. Modify the end of Dma.c to do the following:
   - Enable the “DINTCH1” interrupt in the PIE (Hint: use the PieCtrlRegs structure)
   - Enable the appropriate core interrupt in the IER register

8. Open and inspect DefaultIsr_9.c. Notice that this file contains the DMA interrupt service routine. Save and close all modified files.

Build and Load

9. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.

10. Click the “Debug” button (green bug). The “CCS Debug Perspective” view should open, the program will load automatically, and you should now be at the start of main(). If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to EMU_BOOT_SARAM using the Scripts menu.

Run the Code – Test the DMA Operation

Note: For the next step, check to be sure that the jumper wire connecting PWM1A (pin # GPIO-00) to ADCINA0 (pin # ADC-A0) is in place on the Docking Station.

11. Run the code in real-time mode using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset, and watch the memory browser update. Verify that the ADC result buffer contains updated values.

12. Setup a dual-time graph of the filtered and unfiltered ADC results buffer. Click: Tools → Graph → Dual Time and set the following values:

<table>
<thead>
<tr>
<th>Acquisition Buffer Size</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Data Type</td>
<td>32-bit floating-point</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address – A</td>
<td>AdcBufFilteredIQ</td>
</tr>
<tr>
<td>Start Address – B</td>
<td>AdcBufIQ</td>
</tr>
<tr>
<td>Display Data Size</td>
<td>50</td>
</tr>
<tr>
<td>Time Display Unit</td>
<td>µs</td>
</tr>
</tbody>
</table>

13. The graphical display should show the filtered PWM waveform in the Dual Time A display and the unfiltered waveform in the Dual Time B display. You should see that the results match the previous lab exercise.

14. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.
Terminate Debug Session and Close Project

15. Terminate the active debug session using the Terminate button. This will close the debugger and return CCS to the “CCS Edit Perspective” view.

16. Next, close the project by right-clicking on Lab9 in the Project Explorer window and select Close Project.

End of Exercise
Control Law Accelerator

Introduction

This module explains the operation of the control law accelerator (CLA). The CLA is an independent, fully programmable, 32-bit floating-point math processor that enables concurrent execution into the C28x family. This extends the capabilities of the C28x CPU by adding parallel processing. The CLA has direct access to the ADC result registers, and all ePWM, HRPWM, eCAP, eQEP and comparator registers. This allows the CLA to read ADC samples “just-in-time” and significantly reduces the ADC sample to output delay enabling faster system response and higher frequency operation. Utilizing the CLA for time-critical tasks frees up the CPU to perform other system and communication functions concurrently.

Module Objectives

- Explain the purpose and operation of the Control Law Accelerator (CLA)
- Describe the CLA initialization procedure
- Review the CLA registers, instruction set, and programming flow

The control law accelerator is an independent, 32-bit, floating-point, math accelerator. It executes algorithms independently and in parallel with the CPU. It has direct access to the ePWM, high-resolution PWM, eCAP, eQEP, ADC result and comparator registers. It responds to peripheral interrupts independently of the CPU and frees up the CPU for other tasks, such as communications and diagnostics.
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Control Law Accelerator (CLA)

- An independent 32-bit floating-point math accelerator
- Executes algorithms independently and in parallel with the main CPU
- Direct access to ePWM / HRPWM, eCAP, eQEP, ADC result and comparator registers
- Responds to peripheral interrupts independent of the CPU
- Frees up the CPU for other tasks (communications and diagnostics)

CLA Block Diagram
CLA Memory and Register Access

CLA Memory and Register Access

**CLA Program Memory**
- Contains CLA program code
- Mapped to the CPU at reset
- Initialized by the CPU

**Message RAMs**
- Used to pass data between the CPU and CLA
- Always mapped to both the CPU and CLA

**CLA Data Memory**
- Contains variables and coefficients used by the CLA program code
- Mapped to the CPU at reset
- Initialized by CPU

**Peripheral Reg Access**
- ADC Results Regs
- ePWM (all regs)
- HRPWM (all regs)
- Comparator (all regs)
- eCAP (all regs)
- eQEP (all regs)

CLA Tasks

**Task Triggers** (Peripheral Interrupts)
- ADCINT1 to ADCINT8
- EPWM1_INT to EPWM8_INT
- ECAP1_INT to ECAP3_INT
- EQEP1_INT to EQEP2_INT
- CPU Timer 0

**CLA Control & Execution Registers**
- CLA_INT1-8
- MPERINT1-8
- PIE
- INT11
- INT12
- C28x CPU

- A Task is similar to an interrupt service routine
- CLA supports 8 Tasks (Task1-8)
- A task is started by a peripheral interrupt trigger
  - Triggers are enabled in the MPISRCSEL1 register
  - When a trigger occurs the CLA begins execution at the associated task vector entry (MVECT1-8)
- Once a task begins it runs to completion (no nesting)
Software Triggering a Task

- Tasks can also be started by a software trigger using the CPU

  - **Method #1:** Write to Interrupt Force Register (MIFRC) register
    
    ```
    asm("EALLOW");        //enable protected register access
    Cla1Regs.MIFRC.bit.INT4 = 1; //start task 4
    asm("EDIS");                //disable protected register access
    ```

  - **Method #2:** Use IACK instruction
    
    ```
    asm("IACK #0x0008");        //set bit 3 in MIFRC to start task 4
    ```

**More efficient – does not require EALLOW**

Note: Use of IACK requires Cla1Regs.MCTL.bit.IACKE = 1

Control and Execution Registers

**CLA Control and Execution Registers**

- **MPISRCSEL1** – Peripheral Interrupt Source Select (Task 1-8)
- **MVECT1-8** – Task Interrupt Vector (MVECT1/2/3/4/5/6/7/8)
- **MMEMCFG** – Memory Map Configuration (RAM2E, RAM1E, RAM0E, PROGE)
- **MPC** – 12-bit Program Counter (initialized by appropriate MVECTx register)
- **MR0-3** – CLA Floating-Point Result Registers (32-bit)
- **MAR0-1** – CLA Auxiliary Registers (16-bit)
CLA Registers

### CLA Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCTL</td>
<td>Control Register</td>
</tr>
<tr>
<td>MMEMCFG</td>
<td>Memory Configuration Register</td>
</tr>
<tr>
<td>MPISRCSEL1</td>
<td>Peripheral Interrupt Source Select 1 Register</td>
</tr>
<tr>
<td>MIFR</td>
<td>Interrupt Flag Register</td>
</tr>
<tr>
<td>MIER</td>
<td>Interrupt Enable Register</td>
</tr>
<tr>
<td>MIFRC</td>
<td>Interrupt Force Register</td>
</tr>
<tr>
<td>MICLR</td>
<td>Interrupt Flag Clear Register</td>
</tr>
<tr>
<td>MIOVF</td>
<td>Interrupt Overflow Flag Register</td>
</tr>
<tr>
<td>MICLROVF</td>
<td>Interrupt Overflow Flag Clear Register</td>
</tr>
<tr>
<td>MIRUN</td>
<td>Interrupt Run Status Register</td>
</tr>
<tr>
<td>MVECTx</td>
<td>Task x Interrupt Vector (x = 1-8)</td>
</tr>
<tr>
<td>MPC</td>
<td>CLA 12-bit Program Counter</td>
</tr>
<tr>
<td>MARx</td>
<td>CLA Auxiliary Register x (x = 0-1)</td>
</tr>
<tr>
<td>MRx</td>
<td>CLA Floating-Point 32-bit Result Register (x = 0-3)</td>
</tr>
<tr>
<td>MSTF</td>
<td>CLA Floating-Point Status Register</td>
</tr>
</tbody>
</table>

#### CLA Control Register

**Cla1Regs.MCTL**

- **Hard Reset**
  - 0 = no effect
  - 1 = CLA reset (registers set to default state)

- **IACK Enable**
  - 0 = CPU IACK instruction ignored
  - 1 = CPU IACK instruction triggers a task

- **Soft Reset**
  - 0 = no effect
  - 1 = CLA reset (stop current task)
CLA Memory Configuration Register

Cla1Regs.MMEMCFG

CLA Data RAM2 / RAM1 / RAM0 CPU Access Enable
0 = mapped as RAM2E / RAM1E / RAM0E
1 = CPU access to RAM while mapped to CLA data space

CLA Program Space Enable
0 = mapped to CPU program and data space
1 = mapped to CLA program space

CLA Data RAM2 / RAM1 / RAM0 Enable
0 = mapped to CPU program and data space
1 = mapped to CLA data space

CLA Peripheral Interrupt Source
Select 1 Register

Cla1Regs.MPISRCSEL1

Upper Register:

<table>
<thead>
<tr>
<th>Task 8 Peripheral Interrupt Input</th>
<th>Task 7 Peripheral Interrupt Input</th>
<th>Task 6 Peripheral Interrupt Input</th>
<th>Task 5 Peripheral Interrupt Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 = ADCINT8</td>
<td>0000 = ADCINT7</td>
<td>0000 = ADCINT6</td>
<td>0000 = ADCINT5</td>
</tr>
<tr>
<td>0010 = CPU Timer 0</td>
<td>0010 = ePWM7</td>
<td>0010 = ePWM6</td>
<td>0010 = ePWM5</td>
</tr>
<tr>
<td>0100 = eQEP1</td>
<td>0100 = eQEP1</td>
<td>0100 = eQEP1</td>
<td>0100 = eQEP1</td>
</tr>
<tr>
<td>0101 = eQEP2</td>
<td>0101 = eQEP2</td>
<td>0101 = eQEP2</td>
<td>0101 = eQEP2</td>
</tr>
<tr>
<td>1000 = eCAP1</td>
<td>1000 = eCAP1</td>
<td>1000 = eCAP1</td>
<td>1000 = eCAP1</td>
</tr>
<tr>
<td>1001 = eCAP2</td>
<td>1001 = eCAP2</td>
<td>1001 = eCAP2</td>
<td>1001 = eCAP2</td>
</tr>
<tr>
<td>1010 = eCAP3</td>
<td>1010 = eCAP3</td>
<td>1010 = eCAP3</td>
<td>1010 = eCAP3</td>
</tr>
<tr>
<td>other = no source</td>
<td>other = no source</td>
<td>other = no source</td>
<td>other = no source</td>
</tr>
</tbody>
</table>

Note: select 'no source' if task is generated by software

0000 = Default
CLA Peripheral Interrupt Source
Select 1 Register

Cla1Regs.MPISRCSEL1

Lower Register:

<table>
<thead>
<tr>
<th>15 - 12</th>
<th>11 - 8</th>
<th>7 - 4</th>
<th>3 - 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PERINT4SEL</td>
<td>PERINT3SEL</td>
<td>PERINT2SEL</td>
<td>PERINT1SEL</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Task 4 Peripheral Interrupt Input</th>
<th>Task 3 Peripheral Interrupt Input</th>
<th>Task 2 Peripheral Interrupt Input</th>
<th>Task 1 Peripheral Interrupt Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 = ADCINT4</td>
<td>0000 = ADCINT3</td>
<td>0000 = ADCINT2</td>
<td>0000 = ADCINT1</td>
</tr>
<tr>
<td>0010 = ePWM4</td>
<td>0010 = ePWM3</td>
<td>0010 = ePWM2</td>
<td>0010 = ePWM1</td>
</tr>
<tr>
<td>0100 = eQEP1</td>
<td>0100 = no source</td>
<td>0101 = no source</td>
<td>0100 = no source</td>
</tr>
<tr>
<td>0101 = eQEP2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000 = eCAP1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1001 = eCAP2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1010 = eCAP3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>other = no source</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: select 'no source' if task is generated by software

0000 = Default

CLA Interrupt Enable Register

Cla1Regs.MIER

<table>
<thead>
<tr>
<th>15 - 8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>INT8</td>
<td>INT7</td>
<td>INT6</td>
<td>INT5</td>
<td>INT4</td>
<td>INT3</td>
<td>INT2</td>
<td>INT1</td>
</tr>
</tbody>
</table>

0 = task interrupt disable (default)
1 = task interrupt enable

#include “F2806x_Device.h”
Cla1Regs.MIER.bit.INT2 = 1;  //enable Task 2 interrupt
Cla1Regs.MIER.all = 0x0028;  //enable Task 6 and 4 interrupts
CLA Initialization

<table>
<thead>
<tr>
<th>CLA Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLA initialization is performed by the CPU using C code (typically done with the Peripheral Register Header Files)</td>
</tr>
</tbody>
</table>

1. Copy CLA task code from flash to CLA program RAM
2. Initialize CLA data RAMs, as needed
   - Populate with data coefficients, constants, etc.
3. Configure the CLA registers
   - Enable the CLA clock (PCLKCR3 register)
   - Populate the CLA task interrupt vectors (MVECT1-8 registers)
   - Select the desired task interrupt sources (MPISRCSEL1 register)
   - If desired, enable IACK to start task using software (avoids EALLOW)
   - Map CLA program RAM and data RAMs to CLA space
4. Configure desired CLA task completion interrupts in the PIE
5. Enable CLA tasks triggers in the MIER register
6. Initialize the desired peripherals to trigger the CLA tasks

Data is passed between the CLA and CPU via message RAMs

Enabling CLA Support in CCS

- Set the “Specify CLA support” project option to ‘cla0’
- When creating a new CCS project, choosing a device variant that has the CLA will automatically select this option, so normally no user action is required
CLA Task Programming

CLA Task Programming

- Can be written in C or assembly code
- Assembly code will give best performance for time-critical tasks
- Writing in assembly may not be so bad!
  - CLA programs in floating point
  - Often not that much code in a task
- Commonly, the user will use assembly for critical tasks, and C for non-critical tasks

CLA C Language Implementation and Restrictions

CLA C Language Implementation

- Supports C only (no C++ or GCC extension support)
- Different data type sizes than C28x CPU
  - No support for 64-bit integer or 64-bit floating point

<table>
<thead>
<tr>
<th>TYPE</th>
<th>CPU</th>
<th>CLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>char, short</td>
<td>16 bit</td>
<td>16 bit</td>
</tr>
<tr>
<td>int</td>
<td>16 bit</td>
<td>32 bit</td>
</tr>
<tr>
<td>long</td>
<td>32 bit</td>
<td>32 bit</td>
</tr>
<tr>
<td>long long</td>
<td>64 bit</td>
<td>32 bit</td>
</tr>
<tr>
<td>float, double</td>
<td>32 bit</td>
<td>32 bit</td>
</tr>
<tr>
<td>long double</td>
<td>64 bit</td>
<td>32 bit</td>
</tr>
<tr>
<td>pointers</td>
<td>32 bit</td>
<td>16 bit</td>
</tr>
</tbody>
</table>

- CLA architecture is designed for 32-bit data types
  - 16-bit computations incur overhead for sign-extension
  - Primarily used for reading and writing to 16-bit peripheral registers
CLA C Language Restrictions (1 of 2)

◆ CLA C compiler does not support:
  ◆ Initialized global and static data
    ```
    int x; // valid
    int x=5; // not valid
    ```
  ◆ Initialized variables need to be manually handled by an initialization task
  ◆ More than 1 level of function nesting
    ◆ Task can call a function, but a function cannot call another function
  ◆ Function with more than two arguments
  ◆ Recursive function calls
  ◆ Function pointers

CLA C Language Restrictions (2 of 2)

◆ CLA C compiler does not support:
  ◆ Certain fundamental math operations
    ◆ integer division: \( z = x/y; \)
    ◆ modulus (remainder): \( z = x \% y; \)
    ◆ unsigned 32-bit integer compares
      ```
      Uint32 i; if(i < 10) {...} // not valid
      int32 i;  if(i < 10) {...} // valid
      Uint16 i; if(i < 10) {...} // valid
      int16 i;  if(i < 10) {...} // valid
      float32 x; if(x < 10) {...} // valid
      ```
  ◆ C Standard math library functions
CLA Compiler Scratchpad Memory Area

- For local and compiler temporary variables
- Static allocation, used instead of a stack
- Defined in linker command file

Lab.cmd

CLA_SCRATCHPAD_SIZE = 0x100;
--undef_sym=_cla_scratchpad_end
--undef_sym=_cla_scratchpad_start
MEMORY
{

} SECTIONS
{

 Cla1Prog :{*.obj(CLAscratch
 . += CLA_SCRATCHPAD_SIZE;
 *.obj(CLAscratch_end)
 } > L2DPSARAM, PAGE = 1

 Cla1Prog : > L3DPSARAM, PAGE = 0

 RUN_START(_Cla1Prog_Start)

 ClaTasks_C.cla

#include "Lab.h"

interrupt void Cla1Task1 (void) {
    __mdebugstop();
    xDelay[0] = (float32)AdcResult.ADCRESULT0;
    Y = coeffs[4] * xDelay[4];
    xDelay[4] = xDelay[3];
    xDelay[1] = xDelay[0];
    Y = Y + coeffs[0] * xDelay[0];
    ClaFilteredOutput = (Uint16)Y;
}

interrupt void Cla1Task2 (void) {

}

.CLA extension causes the c2000 compiler to invoke the CLA compiler

All code within this file is placed in the section “Cla1Prog”

C Peripheral Register Header File references can be used in CLA C and assembly code

Closing braces are replaced with MSTOP instructions when compiled
CLA Assembly Language Implementation

**CLA Assembly Language Implementation**

- Same assembly instruction format as the C28x and C28x+FPU
- Destination operand is always on the left
- Same mnemonics as C28x+FPU but with a leading “M”

<table>
<thead>
<tr>
<th>CPU: MPY ACC, T, loc16</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU: MPYF32 R0H, R1H, R2H</td>
</tr>
<tr>
<td>CLA: MMPYF32 MR0, MR1, MR2</td>
</tr>
</tbody>
</table>

**CLA Assembly Instruction Overview**

<table>
<thead>
<tr>
<th>Type</th>
<th>Example</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load (Conditional)</td>
<td>MMOV32 MRa,mem32{,CONDF}</td>
<td>1</td>
</tr>
<tr>
<td>Store</td>
<td>MMOV32 mem32,MRa</td>
<td>1</td>
</tr>
<tr>
<td>Load with Data Move</td>
<td>MBMOV32 MRa,mem32</td>
<td>1</td>
</tr>
<tr>
<td>Store/Load MSTF</td>
<td>MBMOV32 MSTF,mem32</td>
<td>1</td>
</tr>
<tr>
<td>Compare, Min, Max</td>
<td>MCMPP32 MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>Absolute, Negative Value</td>
<td>MABSPP32 MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>Unsigned Integer to Float</td>
<td>MNUI16TOF32 MRa,mem16</td>
<td>1</td>
</tr>
<tr>
<td>Integer to Float</td>
<td>M1132TOF32 MRa,mem32</td>
<td>1</td>
</tr>
<tr>
<td>Float to Integer &amp; Round</td>
<td>MF127TO16HR MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>Float to Integer</td>
<td>MF537TO13MR MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>Multiply, Add, Subtract</td>
<td>MUPYF32 MRa,MRb,MRc</td>
<td>1</td>
</tr>
<tr>
<td>1/X (16-bit Accurate)</td>
<td>MEINVF32 MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>1/Sqrt(x) (16-bit Accurate)</td>
<td>MEISQRTF32 MRa,MRb</td>
<td>1</td>
</tr>
<tr>
<td>Integer Load/Store</td>
<td>MMOV16 MRa,mem16</td>
<td>1</td>
</tr>
<tr>
<td>Integer Load/Store Auxiliary Register</td>
<td>MMOV16 MAR,mem16</td>
<td>1</td>
</tr>
<tr>
<td>Branch/Call/Return</td>
<td>MBRCHD 16bitdest{,COND}</td>
<td>1-7</td>
</tr>
<tr>
<td>Integer Bitwise AND, OR, XOR</td>
<td>MAND32 MRa,MRb,MRc</td>
<td>1</td>
</tr>
<tr>
<td>Integer Add and Subtract</td>
<td>MSUB32 MRa,MRb,MRc</td>
<td>1</td>
</tr>
<tr>
<td>Integer Shifts</td>
<td>MSLR32 MRa,#SHIFT</td>
<td>1</td>
</tr>
<tr>
<td>Write Protection Enable/Disable</td>
<td>MALLOW</td>
<td>1</td>
</tr>
<tr>
<td>Halt Code or End Task</td>
<td>MSTOP</td>
<td>1</td>
</tr>
<tr>
<td>No Operation</td>
<td>MNOP</td>
<td>1</td>
</tr>
</tbody>
</table>
CLA Assembly Parallel Instructions

- Parallel bars indicate a parallel instruction
- Parallel instructions operate as a single instruction with a single opcode and performs two operations
- Example: Add + Parallel Store

```
MADDF32 MR3, MR3, MR1
|| MMOV32 @Var, MR3
```

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Example</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiply &amp; Parallel Add/Subtract</td>
<td>MMPYF32 MRa,MRb,MRc</td>
<td></td>
</tr>
<tr>
<td>Multiply, Add, Subtract &amp; Parallel Store</td>
<td>MADDF32 MRa,MRb,MRc</td>
<td></td>
</tr>
<tr>
<td>Multiply, Add, Subtract, MAC &amp; Parallel Load</td>
<td>MADDF32 MRa,MRb,MRc</td>
<td></td>
</tr>
</tbody>
</table>

Both operations complete in a single cycle

CLA Assembly Addressing Modes

- Two addressing modes: Direct and Indirect
- Both modes can access the low 64Kw of memory only:
  - All of the CLA data space
  - Both message RAMs
  - Shared peripheral registers

- **Direct** – Populates opcode field with 16-bit address of the variable
  - example 1: MMOV32 MR1, @_VarA
  - example 2: MMOV32 MR1, @_EPwm1Regs.CMPA.all

- **Indirect** – Uses the address in MAR0 or MAR1 to access memory; after the read or write MAR0/MAR1 is incremented by a 16 bit signed value
  - example 1: MMOV32 MR0, *MAR0[2]++
  - example 2: MMOV32 MR1, *MAR1[-2]++
CLA Task Assembly Code Example

CLA Initialization Code Example

MVECTx contains the offset address from the start of the CLA Program RAM
CLA Code Debugging

CLA Code Debugging

- The CLA can halt, single-step and run independently from the CPU
- Both the CLA and CPU are debugged from the same JTAG port

1. Insert a breakpoint in CLA code
   - Insert MDEBUGSTOP instruction to halt CLA and then rebuild/reload

2. Enable CLA breakpoints
   - Enable CLA breakpoints in the debugger

3. Start the task
   - Done by peripheral interrupt, software (IACK) or MIFRC register
   - CLA executes instructions until MDEBUGSTOP
   - MPC will the have address of MDEBUGSTOP instruction

4. Single step the CLA code
   - Once halted, single step the CLA code
   - Can also run to the next MDEBUGSTOP or to the end of task
   - If another task is pending it will start at end of previous task

5. Disable CLA breakpoints, if desired

Note: When debugging C code, the _mdebugstop() intrinsic places the MDEBUGSTOP instruction at that position in the generated assembly code

- CLA single step – CLA pipeline is clocked only one cycle and then frozen
- CPU single step – CPU pipeline is flushed for each single step

controlSUITE™ - CLA Software Support

- TI provided functions to support floating-point math CLA operations
Lab 10: CLA Floating-Point FIR Filter

Objective

The objective of this lab is to become familiar with operation and programming of the CLA. In the previous lab, the CPU was used to filter the ePWM1A generated 2 kHz, 25% duty cycle symmetric PWM waveform. In this lab, the PWM waveform will be filtered using the CLA. The CLA will directly read the ADC result register and a task will run a low-pass FIR filter on the sampled waveform. The filtered result will be stored in a circular memory buffer. Note that the CLA is operating concurrently with the CPU. As an operational test, the filtered and unfiltered waveforms will be displayed using the graphing feature of Code Composer Studio.

Recall that a task is similar to an interrupt service routine. Once a task is triggered it runs to completion. In this lab two tasks will be used. Task 1 contains the low-pass filter. Task 8 contains a one-time initialization routine that is used to clear (set to zero) the filter delay chain. This must be done by the CLA since the CPU does not have access to this array.

Since there are tradeoffs between the conveniences of C programming and the performance advantages of assembly language programming, three different task scenarios will be explored:

1. Filter and initialization tasks both in C
2. Filter task in assembly, initialization task in C
3. Filter and initialization tasks both in assembly

These three scenarios will highlight the flexibility of programming the CLA tasks, as well as show the required configuration steps for each. Note that scenarios 1 and 2 are the most likely to be used in a real application. There is little to be gained by putting the initialization task in assembly with scenario 3, but it is shown here for completeness as an all-assembly CLA setup.
Procedure

Open the Project

1. A project named Lab10 has been created for this lab. Open the project by clicking on Project → Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab10\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:

   - Adc.c
   - Cla_10.c
   - ClaTasks.asm
   - ClaTasks_C.cla
   - CodeStartBranch.asm
   - DefaultIsr_10_12.c
   - DelayUs.asm
   - Dma.c
   - ECap_7_8_9_10_12.c
   - EPwm_7_8_9_10_12.c
   - F2806x_Cla_typedefs.h
   - F2806x_GlobalVariableDefs.c
   - F2806x_Headers_nonBIOS.cmd
   - Filter.c
   - Gpio.c
   - Lab.h
   - Lab_10.cmd
   - Main_10.c
   - PieCtrl.c
   - PieVect.c
   - SysCtrl.c
   - Watchdog.c

   Note: The ClaTasks.asm file will be added during the lab exercise.

Enabling CLA Support in CCS

2. Open the build options by right-clicking on Lab10 in the Project Explorer window and select Properties. Then under “C2000 Compiler” select “Processor Options”. Notice the “Specify CLA support” is set to cla0. This is needed to compile and assemble CLA code. Click OK to close the Properties window.

Inspect Lab_10.cmd

3. Open and inspect Lab_10.cmd. Notice that a section called “Cla1Prog” is being linked to L3DPSARAM. This section links the CLA program tasks to the CPU memory space. This memory space will be remapped to the CLA memory space during initialization. Additionally, we are defining a symbol (Cla1Prog_Start) with the run-time start address of this memory block. This symbol will be used to calculate the CLA task vector addresses. Also, notice the two message RAM sections used to pass data between the CPU and CLA.

   We are linking CLA code directly to the CLA program RAM because we are not yet using the flash memory. CCS will load the code for us into RAM, and therefore the CPU will not need to copy the CLA code into the CLA program RAM. In the flash programming lab later in this workshop, we will modify the linking so that the CLA code is loaded into flash, and the CPU will do the copy.

4. The CLA C compiler uses a memory section called CLAscratch for storing local and compiler temporary variables. This scratchpad memory area is allocated using the linker command file. It is accessed directly using the symbols __cla_scratchpad_start
and __cla_scratchpad_end. The scratchpad size is designated using the linker defined symbol CLA_SCRATCHPAD_SIZE. We are reserving a 0x100 word memory hole to be used as the compiler scratchpad area. This value can be changed based on your application. At the top of Lab_10.cmd notice the preprocessor option setting for including the scratchpad. We will make use of this setting later in the lab exercise.

**Setup CLA Initialization**

During the CLA initialization, the CPU memory block L3DPSARAM needs to be configured as CLA program memory. This memory space contains the CLA Task routines. A one-time force of the CLA Task 8 will be executed to clear the delay buffer. The CLA Task 1 has been configured to run an FIR filter. The CLA needs to be configured to start Task 1 on the ADCINT1 interrupt trigger. The next section will setup the PIE interrupt for the CLA.

5. Open ClaTasks_C.cla and notice Task 1 has been configured to run an FIR filter. Within this code the ADC result integer (i.e. the filter input) is being first converted to floating-point, and then at the end the floating-point filter output is being converted back to integer. Also, notice Task 8 is being used to initialize the filter delay line. The .cla extension is recognized by the compiler as a CLA C file, and the compiler will generate CLA specific code. At the beginning of the file notice the line that includes the F2806x_Cla_typedefs.h header file. This file is needed to make the CLA C compiler work correctly with the peripheral register header files when unsupported data types are used.

6. Edit Cla_10.c to implement the CLA operation as described in the objective for this lab exercise. Configure the L3DPSARAM memory block to be mapped to CLA program memory space. Configure the L2DPSARAM memory block to be mapped to CLA data memory space for the CLA C compiler scratchpad. Set Task 1 peripheral interrupt source to ADCINT1 and set the other Task peripheral interrupt source inputs to no source. Enable CLA Task 1 interrupt. Enable the use of the IACK instruction to trigger a task, and then enable Task 8 interrupt.

7. Open Main_10.c and add a line of code in main() to call the InitCla() function. There are no passed parameters or return values. You just type

   ```c
   InitCla();
   ```

   at the desired spot in main().

8. In Main_10.c comment out the line of code in main() that calls the InitDma() function. The DMA is no longer being used. The CLA will directly access the ADC RESULT0 register.

**Setup PIE Interrupt for CLA**

Recall that ePWM2 is triggering the ADC at a 50 kHz rate. In the IQmath FIR Filter lab exercise, the ADC generated an interrupt to the CPU, and the CPU implemented the FIR filter in the ADC ISR. Then in the DMA lab exercise, the ADC instead triggered the DMA, and the DMA generated an interrupt to the CPU, where the CPU implemented the FIR filter in the DMA ISR. For this lab exercise, the ADC is instead triggering the CLA, and the CLA will directly read the ADC result register and run a task implementing an FIR filter. The CLA will generate an
interrupt to the CPU, which will store the filtered results to a circular buffer implemented in the CLA ISR.

9. Remember that in Adc.c we commented out the code used to enable the ADCINT1 interrupt in PIE group 1. This is no longer being used. The CLA interrupt will be used instead.

10. Using the “PIE Interrupt Assignment Table” find the location for the CLA Task 1 interrupt “CLA1_INT1” and fill in the following information:

   PIE group #: __________  # within group: __________

   This information will be used in the next step.

11. Modify the end of Cla_10.c to do the following:

   - Enable the “CLA1_INT1” interrupt in the PIE (Hint: use the PieCtrlRegs structure)
   - Enable the appropriate core interrupt in the IER register

12. Open and inspect DefaultIsr_10_12.c. Notice that this file contains the CLA interrupt service routine. Save and close all modified files.

**Build and Load**

13. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.

14. Click the “Debug” button (green bug). The “CCS Debug Perspective” view should open, the program will load automatically, and you should now be at the start of main(). If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to EMU_BOOT_SARAM using the Scripts menu.

**Run the Code – Test the CLA Operation (Tasks in C)**

**Note:** For the next step, check to be sure that the jumper wire connecting PWM1A (pin # GPIO-00) to ADCINA0 (pin # ADC-A0) is in place on the Docking Station.

15. Run the code in real-time mode using the Script function: Scripts → Realtime Emulation Control → Run Realtime with Reset, and watch the memory window update. Verify that the ADC result buffer contains updated values.

16. Setup a dual-time graph of the filtered and unfiltered ADC results buffer. Click: Tools → Graph → Dual Time and set the following values:
17. The graphical display should show the filtered PWM waveform in the Dual Time A display and the unfiltered waveform in the Dual Time B display. You should see that the results match the previous lab exercise.

18. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

### Change Task 1 to FIR Filter in Assembly

Previously, the initialization and filter tasks were implemented in C. In this part, we will not be using the C implementation of the FIR filter located at Task 1 in ClaTasks_C.cla. Instead, we will add ClaTasks.asm to the project and use the assembly implementation of the FIR filter located at Task 1 in this file. The CLA setup code in Cla_10.c and the filter initialization C-code located at Task 8 in ClaTasks_C.cla will not need to change.

19. Switch to the “CCS Edit Perspective” view by clicking the CCS Edit icon in the upper right-hand corner. Open ClaTasks_C.cla and at the beginning of Task 1 change the #if preprocessor directive from 1 to 0. The sections of code between the #if and #endif will not be compiled. This has the same effect as commenting out this code. We need to do this to avoid a conflict with the Task 1 in ClaTask.asm file.

20. Add ClaTasks.asm to project from C:\C28x\Labs\Lab10\Files.

21. Open ClaTasks.asm and notice that the .cdecls directive is being used to include the C header file in the CLA assembly file. Therefore, we can use the Peripheral Register Header File references in the CLA assembly code. Next, notice Task 1 has been configured to run an FIR filter. Within this code special instructions have been used to convert the ADC result integer (i.e. the filter input) to floating-point and the floating-point filter output back to integer. Notice at Task 2 the assembly preprocessor .if directive is set to 0. The assembly preprocessor .endif directive is located at the end of Task 8. With this setting, Tasks 2 through 8 will not be assembled, again avoiding a conflict with Task 2 through 8 in the ClaTasks_C.cla file. Save and close all modified files.
Build and Load

22. Click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.

Run the Code – Test the CLA Operation (Tasks in C and ASM)

23. Run the code in real-time mode using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset, and watch the graph window update. To confirm these are updated values, carefully remove and replace the connector wire to ADCINA0. The results should be the same as before.

24. Fully halt the CPU (real-time mode) by using the Script function: Scripts → Realtime Emulation Control → Full_Halt.

Change All Tasks to Assembly

In this part, we will be using the assembly implementation of the FIR filter and filter delay line initialization routine located at Task 1 and Task 8, respectively, in the ClaTasks.asm file. The setup in Cla_10.c will remain the same. The ClaTasks_C.cla is no longer needed and will be excluded from the build. As a result, the CLA C compiler is not used and the CLA C compiler scratchpad area allocated by the linker command file will not be needed.

25. Switch to the “CCS Edit Perspective” view by clicking the CCS Edit icon in the upper right-hand corner. Open ClaTasks.asm and at the beginning of Task 2 change the assembly preprocessor .if directive to 1. Recall that the assembly preprocessor .endif directive is located at the end of Task 8. Now Task 2 through Task 8 will be assembled, along with Task 1.

26. Exclude ClaTasks_C.cla from the project to avoid conflicts with ClaTasks.asm. In the Project Explorer window right-click on ClaTasks_C.cla and select:

Resource Configurations → Exclude from Build...

click Select All (for Debug and Release) and then OK. This file is no longer needed since all of the tasks are now in ClaTasks.asm.

27. Open Lab_10.cmd and at the beginning of the file change the preprocessor option setting to 0 so that the scratchpad will not be used. This needs to be done to avoid linking errors. Save and close all modified files.

Build and Load

28. Click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “CCS Debug Perspective” view by clicking the CCS Debug icon in the upper right-hand corner.

Run the Code – Test the CLA Operation (Tasks in ASM)

29. Run the code in real-time mode using the Script function: Scripts → Realtime Emulation Control → Run_Realtime_with_Reset, and watch the graph
window update. To confirm these are updated values, carefully remove and replace the
connector wire to ADCINA0. The results should be the same as before.

30. Fully halt the CPU (real-time mode) by using the Script function: Scripts →
Realtime Emulation Control → Full_Halt.

**Terminate Debug Session and Close Project**

31. Terminate the active debug session using the Terminate button. This will close the
debugger and return CCS to the “CCS Edit Perspective” view.

32. Next, close the project by right-clicking on Lab10 in the Project Explorer
window and select Close Project.

**End of Exercise**
**Viterbi, Complex Math, CRC Unit**

**Introduction**

The Viterbi, Complex Math, CRC Unit (VCU) is a fully programmable block that greatly increases the performance of communication, as well as signal processing algorithms. In addition, the VCU eliminates the need for a second processor to manage the communication link.

**Module Objectives**

- Understand the purpose and operation of the Viterbi, Complex Math and CRC Unit (VCU)
  - VCU Overview
  - CRC Unit
  - Viterbi Unit
  - Complex Math Unit

The Viterbi complex math CRC unit extends the C2000 instruction set to support Viterbi operations used in communications; complex math, which includes complex FFTs and complex filters, and is used in power line communications and radar applications; and cyclical redundancy check, which is used in communications and memory robustness checks.
Module Topics

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CRC Unit...................................................................................................................................................... 11-5
Viterbi Unit.................................................................................................................................................. 11-6
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Viterbi, Complex Math, CRC Unit

VCU Overview

**VCU Overview**

*Extends C28x instruction set to support:*

- **Viterbi operations**
- **Complex math**
  - 16-bit fixed-point complex FFT (5 cycle butterfly)
    - *used in spread spectrum communications, and many signal processing algorithms*
  - **Complex filters**
    - *used to improve data reliability, transmission distance, and power efficiency*
  - **Power Line Communications (PLC) and radar applications**
  - **Cyclic Redundancy Check (CRC)**
    - **Communications and memory robustness checks**

---

**VCU Registers**

Status register

Viterbi transition registers

Viterbi and Complex Math general purpose registers

Accumulated CRC result

---

VSTATUS

VT0

VT1

VR0

VR1

VR2

VR3

VR4

VR5

VR6

VR7

VR8

VCRU
VCU Instructions

- Same instruction format as the C28x and C28x+FPU
  - Destination operand is always on the left
  - Same mnemonics as C28x and FPU but with a leading “V”

<table>
<thead>
<tr>
<th>CPU:</th>
<th>MPY</th>
<th>ACC, T, loc16</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU:</td>
<td>MPYF32</td>
<td>R0H, R1H, R2H</td>
</tr>
<tr>
<td>VCU:</td>
<td>VCMPY</td>
<td>VR3, VR2, VR1, VR0</td>
</tr>
</tbody>
</table>

Enabling VCU Support in CCS

- Set the “Specify VCU support” project option to ‘vcu0’
- When creating a new CCS project, choosing a device variant that has the VCU will automatically select this option, so normally no user action is required
controlSUITE™ - VCU Software Support

- TI provided C-callable assembly functions (including source code) to support VCU operation:
  - plcSUITE
  - Viterbi Decoder
  - CRC Functions
  - Complex FFT and Filters

- C28x Codegen Tools (v6.x) linker can generate a CRC of an output section and automatically embed it into the .out file

CRC Unit

Cyclic Redundancy Check (CRC) is an error detecting code used to ensure data integrity:
- Communication networks
- Data storage (memory content check)
- Supports 4 different CRC polynomials:

<table>
<thead>
<tr>
<th>CRC Operation</th>
<th>Polynomial</th>
<th>Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC8</td>
<td>0x07</td>
<td>PRIME</td>
</tr>
<tr>
<td>CRC16 Poly 1</td>
<td>0x8005</td>
<td>G3-PLC, Zigbee</td>
</tr>
<tr>
<td>CRC16 Poly 2</td>
<td>0x1021</td>
<td>G3-PLC, Zigbee</td>
</tr>
<tr>
<td>CRC32</td>
<td>0x4c11db7</td>
<td>PRIME, Ethernet, memory</td>
</tr>
</tbody>
</table>

PRIME = PoweRline Intelligent Metering Evolution
CRC Instructions

- Polynomial used is determined by instruction

<table>
<thead>
<tr>
<th>CRC Operation</th>
<th>Example Instruction</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load CRC result register</td>
<td>VMOV32 VCRC, mem32</td>
<td>1</td>
</tr>
<tr>
<td>Store CRC result register</td>
<td>VMOV32 mem32, VCRC</td>
<td>1</td>
</tr>
<tr>
<td>Clear CRC result register</td>
<td>VCRCCCLR</td>
<td>1</td>
</tr>
<tr>
<td>CRC8 Poly: 0x07</td>
<td>VCRC8L_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VCRC8H_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td>CRC16 Poly 1: 0x8005</td>
<td>VCRC16P1L_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VCRC16P1H_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td>CRC16 Poly 2: 0x1021</td>
<td>VCRC16P2L_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VCRC16P2H_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td>CRC32 Poly: 0x04C11DB7</td>
<td>VCRC32L_1 mem16</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VCRC32H_1 mem16</td>
<td>1</td>
</tr>
</tbody>
</table>

- CRC register (VCRC) contains current CRC value; updated as CRC instructions read memory

Viterbi Unit

- Viterbi – an error correcting decoder
  - Encoder adds redundant data to a message
  - Viterbi decoder used to detect and correct errors

- Commonly used in:
  - Power line communications (PLC)
  - Mobile communications
  - Satellite communications
  - Digital video and radio
Viterbi Decoder

- VCU efficiently implements a software Viterbi decoder
  - Allows flexibility and can change with evolving standards
- Viterbi is a maximum likelihood decoding algorithm
  - Identifies the path taken through a Trellis diagram
  - Selects survivor paths for each state by using a Hamming distance calculation

Viterbi Implementation

- Decoder has 3 main parts:
  - Branch metrics calculation
    - Calculates local distance between every possible state and the received symbol
      - Code Rate = 1/2  1 cycle
      - Code Rate = 1/3  2p cycles
  - Butterfly “add-compare-select” operation
    - Calculates path metrics to choose an optimal path
    - 4 calculations done in a single cycle (VITDLADDSUB)
      - VCU: 2 cycles  F28x: 15 cycles
  - Trace back
    - Reconstructs the original data using the maximum likelihood path for the input sequence (VTRACE)
      - VCU: 3 cycles/stage  F28x: 22 cycles/stage

Code Rate = number of inputs / number of outputs; VCU supports CR = 1/2 and CR = 1/3
# Viterbi Instructions

<table>
<thead>
<tr>
<th>Viterbi Operation</th>
<th>Example Instruction</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Viterbi Transition Registers (VT0, VT1)</td>
<td>VT_CLEAR</td>
<td>1</td>
</tr>
<tr>
<td>Double Add and Subtract (low or high)</td>
<td>VitDLADDSUB VR4,VR3,VR2,VRa</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VitDHADDSUB VR4,VR3,VR2,VRa</td>
<td>1</td>
</tr>
<tr>
<td>Double Subtract and Add (low or high)</td>
<td>VitDLSUBADD VR4,VR3,VR2,VRa</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VitDHSUBADD VR4,VR3,VR2,VRa</td>
<td>1</td>
</tr>
<tr>
<td>Branch Metrics Calculation Code Rate = 1/2 or 1/3</td>
<td>VBITM2 VR0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VBITM3 VR0, VR1, VR2</td>
<td>2p</td>
</tr>
<tr>
<td>Viterbi Select (low or high)</td>
<td>VitLSEL VRa, VRb, VR4, VR3</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VitHSEL VRa, VRb, VR4, VR3</td>
<td>1</td>
</tr>
<tr>
<td>Trace Back</td>
<td>VTRACE mem32, VR0, VT0, VT1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VTRACE VR1, VR0, VT0, VT1</td>
<td>1</td>
</tr>
<tr>
<td>Double Add and Subtract or Subtract and Add with Parallel Store</td>
<td>VitDLADDSUB VR4,VR3,VR2,VRa</td>
<td>1/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Branch Metric (CR=1/2 or 1/3) with Parallel Load</td>
<td>VBITM3 VR0, VR1, VR2</td>
<td>2p/1**</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Viterbi Select with Parallel Load</td>
<td>VitLSEL VRa, VRb, VR4, VR3</td>
<td>1/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

** VBITM2 || VMOV32 (For CR = 1/2) cycles are 1/1

---

## Complex Math Unit

**Complex number:** \( a + bj \)

\[ a = \text{real part} \]
\[ b = \text{imaginary part} \]
\[ j^2 = -1 \]

- Supports 16-bit complex number calculations
  - Arithmetic, complex filters, and complex FFT
- Complex addition and subtraction (1-cycle)
- Complex multiplication
  - 16-bit x 16-bit = 32-bit real and imaginary parts (2 pipelined cycles)
  - 2-cycle Complex multiply and accumulate (MAC)
  - Repeat (RPT ||) complex MAC operation
### 32-bit Complex Addition

\[(a + bj) + (c + dj) = (a + c) + (b + d)j\]

<table>
<thead>
<tr>
<th>VR3</th>
<th>a</th>
<th>Input 1; VR3: 32-bit real</th>
</tr>
</thead>
<tbody>
<tr>
<td>VR2</td>
<td>bj</td>
<td>VR2: 32-bit imaginary</td>
</tr>
<tr>
<td>VR5</td>
<td>c</td>
<td>Input 2; VR5: 32-bit real</td>
</tr>
<tr>
<td>VR4</td>
<td>dj</td>
<td>VR4: 32-bit imaginary</td>
</tr>
</tbody>
</table>

\[
\text{VCADD VR5, VR4, VR3, VR2}
\]

<table>
<thead>
<tr>
<th>VR5</th>
<th>((a + c &gt;&gt; \text{SHR}))</th>
<th>Result; VR5: 32-bit real</th>
</tr>
</thead>
<tbody>
<tr>
<td>VR4</td>
<td>((b + d &gt;&gt; \text{SHR})j)</td>
<td>VR4: 32-bit imaginary</td>
</tr>
</tbody>
</table>

### Complex Multiply

\[(a + bj)(c + dj) = ac + bcj + adj + bdj^2 = (ac - bd) + (bc + ad)j\]

<table>
<thead>
<tr>
<th>VR0</th>
<th>a</th>
<th>Input 1; VR0H: 16-bit real</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>bj</td>
<td>VR0L: 16-bit imaginary</td>
</tr>
<tr>
<td>VR1</td>
<td>c</td>
<td>Input 2; VR1H: 16-bit real</td>
</tr>
<tr>
<td></td>
<td>dj</td>
<td>VR1L: 16-bit imaginary</td>
</tr>
</tbody>
</table>

\[
\text{VCMPY VR3, VR2, VR1, VR0}
\]

<table>
<thead>
<tr>
<th>VR3</th>
<th>((ac - bd))</th>
<th>Result; VR3: 32-bit real</th>
</tr>
</thead>
<tbody>
<tr>
<td>VR2</td>
<td>((bc + ad)j)</td>
<td>VR2: 32-bit imaginary</td>
</tr>
</tbody>
</table>
Complex Math Instructions

<table>
<thead>
<tr>
<th>Complex Math Operation</th>
<th>Example Instruction</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negative</td>
<td>VNEG VRa</td>
<td>1</td>
</tr>
<tr>
<td>Setup Shift Value</td>
<td>VSETSHR #5bit</td>
<td>1</td>
</tr>
<tr>
<td>Left and Right</td>
<td>VSETSHL #5bit</td>
<td>1</td>
</tr>
<tr>
<td>Saturation On/Off</td>
<td>VSATON / VSATOFF</td>
<td>1</td>
</tr>
<tr>
<td>Rounding On/Off</td>
<td>VRNDO / VRNDOFF</td>
<td>1</td>
</tr>
<tr>
<td>Clear Overflow Flag</td>
<td>VCLROVFR</td>
<td>1</td>
</tr>
<tr>
<td>Real &amp; Imaginary</td>
<td>VCLROVFI</td>
<td></td>
</tr>
<tr>
<td>32+32=32-bit Add or Subtract</td>
<td>VCADD VR5, VR4, VR3, VR2</td>
<td>1</td>
</tr>
<tr>
<td>16+32=16-bit Add or Subtract</td>
<td>VCDADD16 VR5, VR4, VR3, VR2</td>
<td>1</td>
</tr>
<tr>
<td>16x16 = 32-bit Multiply</td>
<td>VCMPY VR3, VR2, VR1, VR0</td>
<td>2p</td>
</tr>
<tr>
<td>Complex MAC</td>
<td>VCMAC VR5, VR4, VR3, VR2, VR1, VR0</td>
<td>2p</td>
</tr>
<tr>
<td>RPT</td>
<td></td>
<td>MAC</td>
</tr>
<tr>
<td>Add/Sub/Multiply with Parallel Load</td>
<td>VCADD VR5,VR4,VR3,VR2,</td>
<td>1/1</td>
</tr>
<tr>
<td>ADD16/SUB16 with Parallel Load</td>
<td>VCMAC VR7, VR6, VR5, VR4, VR3, VR2, mem32, XAR7++</td>
<td>1/1</td>
</tr>
<tr>
<td>Multiply with Parallel Store</td>
<td>VCMPY VR3, VR2, VR1, VR0</td>
<td>2p/1</td>
</tr>
<tr>
<td>MAC with Parallel Load</td>
<td>VMAC VR5, VR4, VR3, VR2, VR1, VR0</td>
<td>2p/1</td>
</tr>
</tbody>
</table>

VCU Summary

- VCU extends the capability of the C28x CPU with additional support for:
  - CRC operations
  - Viterbi decode
  - Complex math
- Instructions are an extension of the current instruction set
- Targeted towards specific algorithms
  - Communications and memory robustness checking
  - Fast Viterbi decode for communications
  - Complex filters and FFT
  - PLC and radar applications
System Design

Introduction

This module discusses various aspects of system design. Details of the emulation and analysis block along with JTAG will be explored. Flash memory programming and the Code Security Module will be described.

Module Objectives

- Emulation and Analysis Block
- Flash Configuration and Memory Performance
- Flash Programming
- Code Security Module (CSM)
## Module Topics

### System Design

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- Lab 12: Programming the Flash................................................................................................ 12-14
Emulation and Analysis Block

JTAG Emulation System
(based on IEEE 1149.1 Boundary Scan Standard)

Some Available Emulators

**XDS510 CLASS** -
BlackHawk: USB2000
Signum System: JTAGjet-C2000
Spectrum Digital: XDS510LC

These emulators are C2000 specific, and are much lower cost than emulators that support all TI MCU/DSP platforms (although those can certainly be used).

**XDS100 CLASS** -
BlackHawk: USB100
Olimex: TMS320-JTAG-USB
Spectrum Digital: XDS100

These emulators are much slower than the ones listed above, but are also available at a lower cost than XDS510 class and are NOT C2000 specific.

**XDS200 CLASS** - offers a balance of low cost with good performance fitting between XDS100 and XDS510.

### Emulator Connections to the Device

- **TMS320F2806x**
  - TRST
  - TMS
  - TDI
  - TDO
  - TCK

- **Emulator Header**
  - EMU0
  - EMU1
  - TRST
  - TMS
  - TDI
  - TDO
  - TCK

- **Vcc (3.3 V)**
- **GND**

**Note:** If distance between device and header is greater than 6 inches
On-Chip Emulation Analysis Block: Capabilities

Two hardware analysis units can be configured to provide any one of the following advanced debug features:

<table>
<thead>
<tr>
<th>Analysis Configuration</th>
<th>Debug Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 Hardware Breakpoints</td>
<td>⇒ Halt on a specified instruction (for debugging in Flash)</td>
</tr>
<tr>
<td>2 Address Watchpoints</td>
<td>⇒ A memory location is getting corrupted; halt the processor when any value is written to this location</td>
</tr>
<tr>
<td>1 Address Watchpoint with Data</td>
<td>⇒ Halt program execution after a specific value is written to a variable</td>
</tr>
<tr>
<td>1 Pair Chained Breakpoints</td>
<td>⇒ Halt on a specified instruction only after some other specific routine has executed</td>
</tr>
</tbody>
</table>

On-Chip Emulation Analysis Block: Hardware Breakpoints and Watchpoints

View ➔ Breakpoints

Hardware Breakpoint Properties

Hardware Watchpoint Properties
On-Chip Emulation Analysis Block: Online Stack Overflow Detection

- Emulation analysis registers are accessible to code as well!
- Configure a watchpoint to monitor for writes near the end of the stack
- Watchpoint triggers maskable RTOSINT interrupt
- Works with DSP/BIOS and non-DSP/BIOS
  - See TI application report SPRA820 for implementation details

![Diagram of stack and data memory with stack overflow detection](image)

- Region of memory occupied by the stack
- Stack grows towards higher memory addresses
- Data Memory
- Monitor for data writes in region near the end of the stack
Flash Configuration and Memory Performance

Basic Flash Operation

- Flash is arranged in pages of 128 words
- Wait states are specified for consecutive accesses within a page, and random accesses across pages
- OTP has random access only
- Must specify the number of SYSCLKOUT wait-states; Reset defaults are maximum value (15)
- Flash configuration code should not be run from the Flash memory

### FlashRegs.FBANKWAIT

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>PAGEWAIT</td>
<td>reserved</td>
<td>RANDWAIT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FlashRegs.FOTPWAIT

<table>
<thead>
<tr>
<th>15</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>OTPWAIT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*** Refer to the F2806x datasheet for detailed numbers ***

For 90 MHz, PAGEWAIT = 3, RANDWAIT = 3, OTPWAIT = 5

Speeding Up Code Execution in Flash

Flash Pipelining (for code fetch only)

FlashPipeline Enable
0 = disable (default)
1 = enable

FlashRegs.FOPT.bit.ENPIPE = 1;

15 12 11 8 7 4 3 0
reserved 1 ENPIPE
**Code Execution Performance**

- **Assume 90 MHz SYSCLKOUT, 16-bit instructions**
  
  (80% of instructions are 16 bits wide – Rest are 32 bits)

**Internal RAM: 90 MIPS**

Fetch up to 32-bits every cycle ➔ 1 instruction/cycle * 90 MHz = 90 MIPS

**Flash (w/ pipelining): 90 MIPS**

RANDWAIT = 3

Fetch 64 bits every 3 cycles, but it will take 4 cycles to execute them ➔

4 instructions/4 cycles * 90 MHz = 90 MIPS

RPT will increase this; PC discontinuity will degrade this

Benchmarking in control applications has shown actual performance of about 81 MIPS

---

**Data Access Performance**

- **Assume 90 MHz SYSCLKOUT**

<table>
<thead>
<tr>
<th>Memory</th>
<th>16-bit access (words/cycle)</th>
<th>32-bit access (words/cycle)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal RAM</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
| Flash       | 0.33                       | 0.33                       | RANDWAIT = 2
              |                             |                            | Flash is read only!    |

- Internal RAM has best data performance – put time critical data here
- Flash performance usually sufficient for most constants and tables
- Note that the flash instruction fetch pipeline will also stall during a flash data access
### Other Flash Configuration Registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00 0A80</td>
<td>FOPT</td>
<td>Flash option register</td>
</tr>
<tr>
<td>0x00 0A82</td>
<td>FPWR</td>
<td>Flash power modes registers</td>
</tr>
<tr>
<td>0x00 0A83</td>
<td>FSTATUS</td>
<td>Flash status register</td>
</tr>
<tr>
<td>0x00 0A84</td>
<td>FSTDBYWAIT</td>
<td>Flash sleep to standby wait register</td>
</tr>
<tr>
<td>0x00 0A85</td>
<td>FACTIVEWAIT</td>
<td>Flash standby to active wait register</td>
</tr>
<tr>
<td>0x00 0A86</td>
<td>FBANKWAIT</td>
<td>Flash read access wait state register</td>
</tr>
<tr>
<td>0x00 0A87</td>
<td>FOTPWAIT</td>
<td>OTP read access wait state register</td>
</tr>
</tbody>
</table>

- **FPWR**: Save power by putting Flash/OTP to ‘Sleep’ or ‘Standby’ mode; Flash will automatically enter active mode if a Flash/OTP access is made.
- **FSTATUS**: Various status bits (e.g. PWR mode)
- **FSTDBYWAIT, FACTIVEWAIT**: Specify # of delay cycles during wake-up from sleep to standby, and from standby to active, respectively. The delay is needed to let the flash stabilize. *Leave these registers set to their default maximum value.*

See the “TMS320x2806x Piccolo Technical Reference Manual” – Systems Control and Interrupts section in SPRUH18 for more information.
Flash Programming

Flash Programming Basics

- The device CPU performs the flash programming
- The CPU executes Flash utility code from RAM that reads the Flash data and writes it into the Flash
- We need to get the Flash utility code and the Flash data into RAM

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Erase</td>
<td>- Set all bits to zero, then to one</td>
</tr>
<tr>
<td>2. Program</td>
<td>- Program selected bits with zero</td>
</tr>
<tr>
<td>3. Verify</td>
<td>- Verify flash contents</td>
</tr>
</tbody>
</table>

- Minimum **Erase** size is a sector (8Kw or 16Kw)
- Minimum **Program** size is a bit!
- Important not to lose power during erase step: If CSM passwords happen to be all zeros, the CSM will be permanently locked!
- Chance of this happening is quite small! (Erase step is performed sector by sector)
Flash Programming Utilities

- **JTAG Emulator Based**
  - Code Composer Studio on-chip Flash programmer
  - BlackHawk Flash utilities (requires Blackhawk emulator)
  - Elprotronic FlashPro2000
  - Spectrum Digital SDFlash JTAG (requires SD emulator)
  - Signum System Flash utilities (requires Signum emulator)

- **SCI Serial Port Bootloader Based**
  - Code-Skin (http://www.code-skin.com)
  - Elprotronic FlashPro2000

- **Production Test/Programming Equipment Based**
  - BP Micro programmer
  - Data I/O programmer

- **Build your own custom utility**
  - Can use any of the ROM bootloader methods
  - Can embed flash programming into your application
  - Flash API algorithms provided by TI

* TI web has links to all utilities (http://www.ti.com/c2000)

---

**CCS On-Chip Flash Programmer**

- On-Chip Flash programmer is integrated into the CCS debugger

* Tools → On-Chip Flash
Code Security Module (CSM)

- Access to the following on-chip memory is restricted:

<table>
<thead>
<tr>
<th>0x000A80</th>
<th>Flash Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x008800</td>
<td>L0 DPSARAM (2Kw)</td>
</tr>
<tr>
<td>0x008C00</td>
<td>L1 DPSARAM (1Kw)</td>
</tr>
<tr>
<td>0x009000</td>
<td>L2 DPSARAM (1Kw)</td>
</tr>
<tr>
<td>0x00A000</td>
<td>L3 DPSARAM (4Kw)</td>
</tr>
<tr>
<td>0x00C000</td>
<td>L4 DPSARAM (8Kw)</td>
</tr>
<tr>
<td>0x3D7800</td>
<td>reserved</td>
</tr>
<tr>
<td>0x3D7C00</td>
<td>User OTP (1Kw)</td>
</tr>
<tr>
<td>0x3D7C80</td>
<td>reserved</td>
</tr>
<tr>
<td>0x3D7CC0</td>
<td>ADC / OSC cal. data</td>
</tr>
<tr>
<td>0x3D8000</td>
<td>FLASH (128Kw)</td>
</tr>
<tr>
<td>0x3F7FF8</td>
<td>PASSWORDS (8w)</td>
</tr>
</tbody>
</table>

- Data reads and writes from restricted memory are only allowed for code running from restricted memory
- All other data read/write accesses are blocked:
  - JTAG emulator/debugger, ROM bootloader, code running in external memory or unrestricted internal memory

CSM Password

- 128-bit user defined password is stored in Flash
- 128-bit KEY registers are used to lock and unlock the device
  - Mapped in memory space 0x00 0AE0 – 0x00 0AE7
  - Registers “EALLOW” protected
## CSM Registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00 0AE0</td>
<td>KEY0</td>
<td>Low word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE1</td>
<td>KEY1</td>
<td>2nd word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE2</td>
<td>KEY2</td>
<td>3rd word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE3</td>
<td>KEY3</td>
<td>4th word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE4</td>
<td>KEY4</td>
<td>5th word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE5</td>
<td>KEY5</td>
<td>6th word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE6</td>
<td>KEY6</td>
<td>7th word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AE7</td>
<td>KEY7</td>
<td>High word of 128-bit Key register</td>
</tr>
<tr>
<td>0x00 0AEF</td>
<td>CSMSCR</td>
<td>CSM status and control register</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3F 7FF8</td>
<td>PWL0</td>
<td>Low word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FF9</td>
<td>PWL1</td>
<td>2nd word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFA</td>
<td>PWL2</td>
<td>3rd word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFB</td>
<td>PWL3</td>
<td>4th word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFC</td>
<td>PWL4</td>
<td>5th word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFD</td>
<td>PWL5</td>
<td>6th word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFE</td>
<td>PWL6</td>
<td>7th word of 128-bit password</td>
</tr>
<tr>
<td>0x3F 7FFF</td>
<td>PWL7</td>
<td>High word of 128-bit password</td>
</tr>
</tbody>
</table>

### Locking and Unlocking the CSM

- **The CSM is always locked after reset**
- **To unlock the CSM:**
  - Perform a dummy read of each PWL (passwords in the flash)
  - Write the correct password to each KEY register
- **Passwords are all 0xFFFF on new devices**
  - When passwords are all 0xFFFF, only a read of each PWL is required to unlock the device
  - The bootloader does these dummy reads and hence unlocks devices that do not have passwords programmed
## CSM Caveats

- Never program all the PWL’s as 0x0000
  - Doing so will permanently lock the CSM
- Flash addresses 0x3F7F80 to 0x3F7FF5, inclusive, must be programmed to 0x0000 to securely lock the CSM
- Remember that code running in unsecured RAM cannot access data in secured memory
  - Don’t link the stack to secured RAM if you have any code that runs from unsecured RAM
- Do not embed the passwords in your code!
  - Generally, the CSM is unlocked only for debug
  - Code Composer Studio can do the unlocking

## CSM Password Match Flow

1. **Start**
2. Flash device secure after reset or runtime
3. Do dummy reads of PWL 0x3F 7FF8 – 0x3F 7FFF
4. Is PWL = all 0s?
   - Yes: Device permanently locked
   - No: Is PWL = all Fs?
     - Yes: Write password to KEY registers 0x00 0AE0 – 0x00 0AE7 (EALLOW) protected
       - Correct password?
         - Yes: Device unlocked, User can access on-chip secure memory
         - No: Is PWL = all Fs?
           - Yes: Correct password?
             - Yes: Device unlocked, User can access on-chip secure memory
             - No: Device permanently locked
Lab 12: Programming the Flash

Objective

The objective of this lab is to program and execute code from the on-chip flash memory. The TMS320F28069 device has been designed for standalone operation in an embedded system. Using the on-chip flash eliminates the need for external non-volatile memory or a host processor from which to bootload. In this lab, the steps required to properly configure the software for execution from internal flash memory will be covered.

Procedure

Open the Project

1. A project named Lab12 has been created for this lab. Open the project by clicking on Project ➔ Import CCS Projects. The “Import CCS Eclipse Projects” window will open then click Browse... next to the “Select search-directory” box. Navigate to: C:\C28x\Labs\Lab12\Project and click OK. Then click Finish to import the project. All build options have been configured the same as the previous lab. The files used in this lab are:
Lab 12: Programming the Flash

Adc.c
Cla_12.c
ClaTasks.asm
ClaTasks_C.cla
CodeStartBranch.asm
DefaultIsr_10_12.c
DelayUs.asm
Dma.c
ECap_7_8_9_10_12.c
EPwm_7_8_9_10_12.c
F2806x_Cla_typedefs.h
F2806x_DefaultIsr.h
F2806x_GlobalVariableDefs.c

Note: The Flash.c and Passwords.asm files will be added during the lab exercise.

Link Initialized Sections to Flash

Initialized sections, such as code and constants, must contain valid values at device power-up. Stand-alone operation of an F28069 embedded system means that no emulator is available to initialize the device RAM. Therefore, all initialized sections must be linked to the on-chip flash memory.

Each initialized section actually has two addresses associated with it. First, it has a LOAD address which is the address to which it gets loaded at load time (or at flash programming time). Second, it has a RUN address which is the address from which the section is accessed at runtime. The linker assigns both addresses to the section. Most initialized sections can have the same LOAD and RUN address in the flash. However, some initialized sections need to be loaded to flash, but then run from RAM. This is required, for example, if the contents of the section needs to be modified at runtime by the code.

2. Open and inspect the linker command file Lab_12.cmd. Notice that a memory block named FLASH_ABCDEFGH has been created at origin = 0x3D8000, length = 0x01FF80 on Page 0. This flash memory block length has been selected to avoid conflicts with other required flash memory spaces. See the reference slide at the end of this lab exercise for further details showing the address origins and lengths of the various memory blocks used.

3. Edit Lab_12.cmd to link the following compiler sections to on-chip flash memory block FLASH_ABCDEFGH:

<table>
<thead>
<tr>
<th>Compiler Sections:</th>
</tr>
</thead>
<tbody>
<tr>
<td>.text</td>
</tr>
</tbody>
</table>

4. In Lab_12.cmd notice that the section named “IQmath” is an initialized section that needs to load to and run from flash. Previously the “IQmath” section was linked to L4SARAM. Edit Lab_12.cmd so that this section is now linked to FLASH_ABCDEFGH. Save your work and close the file.
Copying Interrupt Vectors from Flash to RAM

The interrupt vectors must be located in on-chip flash memory and at power-up needs to be copied to the PIE RAM as part of the device initialization procedure. The code that performs this copy is located in InitPieCtrl(). The C-compiler runtime support library contains a memory copy function called memcpy() which will be used to perform the copy.

5. Open and inspect InitPieCtrl() in PieCtrl.c. Notice the memcpy() function used to initialize (copy) the PIE vectors. At the end of the file a structure is used to enable the PIE.

Initializing the Flash Control Registers

The initialization code for the flash control registers cannot execute from the flash memory (since it is changing the flash configuration!). Therefore, the initialization function for the flash control registers must be copied from flash (load address) to RAM (run address) at runtime. The memory copy function memcpy() will again be used to perform the copy. The initialization code for the flash control registers InitFlash() is located in the Flash.c file.

6. Add Flash.c to the project.

7. Open and inspect Flash.c. The C compiler CODE_SECTION pragma is used to place the InitFlash() function into a linkable section named “secureRamFuncs”.

8. The “secureRamFuncs” section will be linked using the user linker command file Lab_12.cmd. Open and inspect Lab_12.cmd. The “secureRamFuncs” will load to flash (load address) but will run from L4SARAM (run address). Also notice that the linker has been asked to generate symbols for the load start, load size, and run start addresses.

While not a requirement from a MCU hardware or development tools perspective (since the C28x MCU has a unified memory architecture), historical convention is to link code to program memory space and data to data memory space. Therefore, notice that for the L4SARAM memory we are linking “secureRamFuncs” to, we are specifying “PAGE = 0” (which is program memory).

9. Open and inspect Main_12.c. Notice that the memory copy function memcpy() is being used to copy the section “secureRamFuncs”, which contains the initialization function for the flash control registers.

10. Add a line of code in main() to call the InitFlash() function. There are no passed parameters or return values. You just type

    InitFlash();

    at the desired spot in main().

Code Security Module and Passwords

The CSM module provides protection against unwanted copying (i.e. pirating!) of your code from flash, OTP memory, and the L0, L1, L2, L3 and L4 RAM blocks. The CSM uses a 128-bit password made up of 8 individual 16-bit words. They are located in flash at addresses 0x3F7FF8.
to 0x3F7FFF. During this lab, dummy passwords of 0xFFFF will be used – therefore only dummy reads of the password locations are needed to unsecure the CSM. **DO NOT PROGRAM ANY REAL PASSWORDS INTO THE DEVICE.** After development, real passwords are typically placed in the password locations to protect your code. We will not be using real passwords in the workshop.

The CSM module also requires programming values of 0x0000 into flash addresses 0x3F7F80 through 0x3F7FF5 in order to properly secure the CSM. Both tasks will be accomplished using a simple assembly language file `Passwords.asm`.

11. Add `Passwords.asm` to the project.

12. Open and inspect `Passwords.asm`. This file specifies the desired password values *(DO NOT CHANGE THE VALUES FROM 0xFFFF)* and places them in an initialized section named “passwords”. It also creates an initialized section named “csm_rsvd” which contains all 0x0000 values for locations 0x3F7F80 to 0x3F7FF5 (length of 0x76).

13. Open `Lab_12.cmd` and notice that the initialized sections for “passwords” and “csm_rsvd” are linked to memories named PASSWORDS and CSM_RSVD, respectively.

### Executing from Flash after Reset

The F28069 device contains a ROM bootloader that will transfer code execution to the flash after reset. When the boot mode selection is set for “Jump to Flash” mode, the bootloader will branch to the instruction located at address 0x3F7FF6 in the flash. An instruction that branches to the beginning of your program needs to be placed at this address. Note that the CSM passwords begin at address 0x3F7FF8. There are exactly two words available to hold this branch instruction, and not coincidentally, a long branch instruction “LB” in assembly code occupies exactly two words. Generally, the branch instruction will branch to the start of the C-environment initialization routine located in the C-compiler runtime support library. The entry symbol for this routine is `_c_int00`. Recall that C code cannot be executed until this setup routine is run. Therefore, assembly code must be used for the branch. We are using the assembly code file named `CodeStartBranch.asm`.

14. Open and inspect `CodeStartBranch.asm`. This file creates an initialized section named “codestart” that contains a long branch to the C-environment setup routine. This section needs to be linked to a block of memory named BEGIN_FLASH.

15. In the earlier lab exercises, the section “codestart” was directed to the memory named BEGIN_M0. Edit `Lab_12.cmd` so that the section “codestart” will be directed to BEGIN_FLASH. Save your work and close the opened files.

On power up the reset vector will be fetched and the ROM bootloader will begin execution. If the emulator is connected, the device will be in emulator boot mode and will use the EMU_KEY and EMU_BMODE values in the PIE RAM to determine the boot mode. This mode was utilized in an earlier lab. In this lab, we will be disconnecting the emulator and running in stand-alone boot mode (but do not disconnect the emulator yet!). The bootloader will read the OTP_KEY and OTP_BMODE values from their locations in the OTP. The behavior when these values have not been programmed (i.e., both 0xFFFF) or have been set to invalid values is boot to flash boot mode.
Initializing the CLA

Previously, the named section “Cla1Prog” containing the CLA program tasks was linked directly to the CPU memory block L3DPSARAM for both load and run purposes. At runtime, all the code did was map the L3DPSARAM block to the CLA program memory space during CLA initialization. For an embedded application, the CLA program tasks are linked to load to flash and run from RAM. At runtime, the CLA program tasks must be copied from flash to L3DPSARAM. The memory copy function memcpy() will once again be used to perform the copy. After the copy is performed, the L3DPSARAM block will then be mapped to CLA program memory space as was done in the earlier lab.

16. Open and inspect Lab_12.cmd. Notice that the named section “Cla1Prog” will now load to flash (load address) but will run from L3DPSARAM (run address). The linker will also be used to generate symbols for the load start, load size, and run start addresses.

17. Open Cla_12.c and notice that the memory copy function memcpy() is being used to copy the CLA program code from flash to L3DPSARAM using the symbols generated by the linker. Just after the copy the Cla1Regs structure is used to configure the L3DPSARAM block as CLA program memory space. Close the inspected files.

Build – Lab.out

18. Click the “Build” button to generate the Lab.out file to be used with the CCS Flash Programmer. Check for errors in the Problems window.

Programming the On-Chip Flash Memory

In CCS the on-chip flash programmer is integrated into the debugger. When the program is loaded CCS will automatically determine which sections reside in flash memory based on the linker command file. CCS will then program these sections into the on-chip flash memory. Additionally, in order to effectively debug with CCS, the symbolic debug information (e.g., symbol and label addresses, source file links, etc.) will automatically load so that CCS knows where everything is in your code. Clicking the “Debug” button in the “CCS Edit Perspective” will automatically launch the debugger, connect to the target, and program the flash memory in a single step.

19. Program the flash memory by clicking the “Debug” button (green bug). (If needed, when the “Progress Information” box opens select “Details >>” in order to watch the programming operation and status). After successfully programming the flash memory the “Progress Information” box will close.

Running the Code – Using CCS

20. Reset the CPU using the “Reset CPU” button or click:

Run → Reset → Reset CPU

The program counter should now be at address 0xFF75C in the “Disassembly” window, which is the start of the bootloader in the Boot ROM. If needed, click on the “View Disassembly…” button in the window that opens, or click View → Disassembly.
21. Under Scripts on the menu bar click:
   EMU Boot Mode Select → EMU_BOOT_FLASH.
   This has the debugger load values into EMU_KEY and EMU_BMODE so that the
   bootloader will jump to "Flash" at address 0x3F7FF6.

22. Single-Step by using the <F5> key (or you can use the Step Into button on the
   horizontal toolbar) through the bootloader code until you arrive at the beginning of the
codestart section in the CodeStartBranch.asm file. (Be patient, it will take about
125 single-steps). Notice that we have placed some code in CodeStartBranch.asm
to give an option to first disable the watchdog, if selected.

23. Step a few more times until you reach the start of the C-compiler initialization routine at
the symbol _c_int00.

24. Now do Run → Go Main. The code should stop at the beginning of your
   main() routine. If you got to that point successfully, it confirms that the flash has been
   programmed properly, that the bootloader is properly configured for jump to flash mode,
   and that the codestart section has been linked to the proper address.

25. You can now run the CPU, and you should observe the LED on the controlCARD
   blinking. Try resetting the CPU, select the EMU_BOOT_FLASH boot mode, and then
   hitting run (without doing all the stepping and the Go Main procedure). The LED should
   be blinking again.

26. Halt the CPU.

Terminaté Debug Session and Close Project

27. Terminate the active debug session using the Terminate button. This will close the
debugger and return CCS to the “CCS Edit Perspective” view.

28. Next, close the project by right-clicking on Lab12 in the Project Explorer
   window and select Close Project.

Running the Code – Stand-alone Operation (No Emulator)

Recall that if the device is in stand-alone boot mode, the state of GPIO34 and GPIO37 pins are
used to determine the boot mode. On the controlCARD switch SW1 controls the boot options for
the F28069 device. Check that switch SW1 positions 1 and 2 are set to the default “1 – on”
position (both switches up). This will configure the device (in stand-alone boot mode) to
GetMode. Since the OTP_KEY has not been programmed, the default GetMode will be boot
from flash. Details of the switch positions can be found in Appendix A.


30. Disconnect the USB cable (emulator) from the Docking Station (i.e. remove power from
   the controlCARD).

31. Re-connect the USB cable to the Docking Station to power the controlCARD. The LED
   should be blinking, showing that the code is now running from flash memory.

   End of Exercise
Flash Memory Section Blocks

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
<th>Length</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3D 8000</td>
<td>FLASH</td>
<td>0x1FF80</td>
<td>0</td>
</tr>
<tr>
<td>0x3F 7FF8</td>
<td>CSM_RSVD</td>
<td>0x76</td>
<td>0</td>
</tr>
<tr>
<td>0x3F 7FF6</td>
<td>BEGIN_FLASH</td>
<td>0x2</td>
<td>0</td>
</tr>
<tr>
<td>0x3F 7FF8</td>
<td>PASSWORDS</td>
<td>0x8</td>
<td>0</td>
</tr>
</tbody>
</table>

Lab_12.cmd

```
SECTIONS
{
    codestart    :> BEGIN_FLASH, PAGE = 0
    passwords    :> PASSWORDS, PAGE = 0
    csm_rsvd     :> CSM_RSVD, PAGE = 0
}
```

Startup Sequence from Flash Memory

1. **RESET**
2. Boot ROM (32Kw)
3. Boot Code
4. _c_int00
5. "rts2800_ml.lib"

```
"user" code sections
main ()
{
    ...... 
    ...... 
}
```
Communications

Introduction

The TMS320C28x contains features that allow several methods of communication and data exchange between the C28x and other devices. Many of the most commonly used communications techniques are presented in this module.

The intent of this module is not to give exhaustive design details of the communication peripherals, but rather to provide an overview of the features and capabilities. Once these features and capabilities are understood, additional information can be obtained from various resources such as documentation, as needed. This module will cover the basic operation of the communication peripherals, as well as some basic terms and how they work.

Module Objectives

- Serial Peripheral Interface (SPI)
- Serial Communication Interface (SCI)
- Multichannel Buffered Serial Port (McBSP)
- Inter-Integrated Circuit (I2C)
- Universal Serial Bus (USB)
- Enhanced Controller Area Network (eCAN)

Note: Up to 2 SPI modules (A/B), 2 SCI module (A), 1 McBSP module (A), 1 I2C module (A), 1 USB (0), and 1 eCAN module (A) are available on the F2806x devices
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Communications Techniques

Several methods of implementing a TMS320C28x communications system are possible. The method selected for a particular design should reflect the method that meets the required data rate at the lowest cost. Various categories of interface are available and are summarized in the learning objective slide. Each will be described in this module.

**Synchronous vs. Asynchronous**

- **Synchronous**
  - Short distances (on-board)
  - High data rate
  - Explicit clock

- **Asynchronous**
  - longer distances
  - Lower data rate \( \approx 1/8 \) of SPI
  - Implied clock (clk/data mixed)
  - Economical with reasonable performance

Serial ports provide a simple, hardware-efficient means of high-level communication between devices. Like the GPIO pins, they may be used in stand-alone or multiprocessing systems.

In a multiprocessing system, they are an excellent choice when both devices have an available serial port and the data rate requirement is relatively low. Serial interface is even more desirable when the devices are physically distant from each other because the inherently low number of wires provides a simpler interconnection.

Serial ports require separate lines to implement, and they do not interfere in any way with the data and address lines of the processor. The only overhead they require is to read/write new words from/to the ports as each word is received/transmitted. This process can be performed as a short interrupt service routine under hardware control, requiring only a few cycles to maintain.

The C28x family of devices have both synchronous and asynchronous serial ports. Detailed features and operation will be described next.
Serial Peripheral Interface (SPI)

The SPI module is a synchronous serial I/O port that shifts a serial bit stream of variable length and data rate between the C28x and other peripheral devices. During data transfers, one SPI device must be configured as the transfer MASTER, and all other devices configured as SLAVES. The master drives the transfer clock signal for all SLAVES on the bus. SPI communications can be implemented in any of three different modes:

- MASTER sends data, SLAVES send dummy data
- MASTER sends data, one SLAVE sends data
- MASTER sends dummy data, one SLAVE sends data

In its simplest form, the SPI can be thought of as a programmable shift register. Data is shifted in and out of the SPI through the SPIDAT register. Data to be transmitted is written directly to the SPIDAT register, and received data is latched into the SPIBUF register for reading by the CPU. This allows for double-buffered receive operation, in that the CPU need not read the current received data from SPIBUF before a new receive operation can be started. However, the CPU must read SPIBUF before the new operation is complete of a receiver overrun error will occur. In addition, double-buffered transmit is not supported: the current transmission must be complete before the next data character is written to SPIDAT or the current transmission will be corrupted.

The Master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the Master detects when the Slave is ready to broadcast.

![SPI Data Flow Diagram]

- Simultaneous transmits and receive
- SPI Master provides the clock signal
SPI Transmit / Receive Sequence

1. Slave writes data to be sent to its shift register (SPIDAT)
2. Master writes data to be sent to its shift register (SPIDAT or SPITXBUF)
3. Completing Step 2 automatically starts SPICLK signal of the Master
4. MSB of the Master’s shift register (SPIDAT) is shifted out, and LSB of the Slave’s shift register (SPIDAT) is loaded
5. Step 4 is repeated until specified number of bits are transmitted
6. SPIDAT register is copied to SPIRXBUF register
7. SPI INT Flag bit is set to 1
8. An interrupt is asserted if SPI INT ENA bit is set to 1
9. If data is in SPITXBUF (either Slave or Master), it is loaded into SPIDAT and transmission starts again as soon as the Master’s SPIDAT is loaded
Since data is shifted out of the SPIDAT register MSB first, transmission characters of less than 16 bits must be left-justified by the CPU software prior to be written to SPIDAT.

Received data is shifted into SPIDAT from the left, MSB first. However, the entire sixteen bits of SPIDAT is copied into SPIBUF after the character transmission is complete such that received characters of less than 16 bits will be right-justified in SPIBUF. The non-utilized higher significance bits must be masked-off by the CPU software when it interprets the character. For example, a 9 bit character transmission would require masking-off the 7 MSB’s.

### SPI Data Character Justification

- Programmable data length of 1 to 16 bits
- Transmitted data of less than 16 bits must be left justified
  - MSB transmitted first
- Received data of less than 16 bits are right justified
- User software must mask-off unused MSB’s
SPI Registers

SPI Baud Rate Register

Need to set this only when in master mode!

<table>
<thead>
<tr>
<th>15-7</th>
<th>6-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>SPI BIT RATE</td>
</tr>
</tbody>
</table>

SPICLK signal = \[
\begin{cases}
\frac{LSPCLK}{SPIBRR + 1}, & \text{SPIBRR = 3 to 127} \\
\frac{LSPCLK}{4}, & \text{SPIBRR = 0, 1, or 2}
\end{cases}
\]

Baud Rate Determination: The Master specifies the communication baud rate using its baud rate register (SPIBRR.6-0):

- For SPIBRR = 3 to 127: \(\text{SPI Baud Rate} = \frac{LSPCLK}{SPIBRR + 1}\) bits/sec
- For SPIBRR = 0, 1, or 2: \(\text{SPI Baud Rate} = \frac{LSPCLK}{4}\) bits/sec

From the above equations, one can compute

Maximum data rate = 20 Mbps @ 80 MHz

Character Length Determination: The Master and Slave must be configured for the same transmission character length. This is done with bits 0, 1, 2 and 3 of the configuration control register (SPICCR.3-0). These four bits produce a binary number, from which the character length is computed as binary + 1 (e.g. SPICCR.3-0 = 0010 gives a character length of 3).
Select SPI Registers

- **Configuration Control** `SpiRegs.SPICCR`
  - Reset, Clock Polarity, Loopback, Character Length

- **Operation Control** `SpiRegs.SPICTL`
  - Overrun Interrupt Enable, Clock Phase, Interrupt Enable
  - Master / Slave Transmit enable

- **Status** `SpiRegs.SPIST`
  - RX Overrun Flag, Interrupt Flag, TX Buffer Full Flag

- **FIFO Transmit** `SpiRegs.SPIFFTX`
- **FIFO Receive** `SpiRegs.SPIFFRX`
  - FIFO Enable, FIFO Reset
  - FIFO Over-flow flag, Over-flow Clear
  - Number of Words in FIFO (FIFO Status)
  - FIFO Interrupt Enable, Interrupt Status, Interrupt Clear
  - FIFO Interrupt Level (Number of Words in FIFO)

*Note: refer to the reference guide for a complete listing of registers*

SPI Summary

- **Synchronous serial communications**
  - Two wire transmit or receive (half duplex)
  - Three wire transmit and receive (full duplex)

- **Software configurable as master or slave**
  - C28x provides clock signal in master mode

- **Data length programmable from 1-16 bits**

- **125 different programmable baud rates**
Serial Communications Interface (SCI)

The SCI module is a serial I/O port that permits Asynchronous communication between the C28x and other peripheral devices. The SCI transmit and receive registers are both double-buffered to prevent data collisions and allow for efficient CPU usage. In addition, the C28x SCI is a full duplex interface which provides for simultaneous data transmit and receive. Parity checking and data formatting is also designed to be done by the port hardware, further reducing software overhead.

![SCI Pin Connections Diagram]

(Full Duplex Shown)
The basic unit of data is called a **character** and is 1 to 8 bits in length. Each character of data is formatted with a start bit, 1 or 2 stop bits, an optional parity bit, and an optional address/data bit. A character of data along with its formatting bits is called a **frame**. Frames are organized into groups called blocks. If more than two serial ports exist on the SCI bus, a block of data will usually begin with an address frame which specifies the destination port of the data as determined by the user’s protocol.

The start bit is a low bit at the beginning of each frame which marks the beginning of a frame. The SCI uses a NRZ (Non-Return-to-Zero) format which means that in an inactive state the SCIRX and SCITX lines will be held high. Peripherals are expected to pull the SCIRX and SCITX lines to a high level when they are not receiving or transmitting on their respective lines.

**When configuring the SCICCR, the SCI port should first be held in an inactive state.** This is done using the SW RESET bit of the SCI Control Register 1 (SCICTL1.5). Writing a 0 to this bit initializes and holds the SCI state machines and operating flags at their reset condition. The SCICCR can then be configured. Afterwards, re-enable the SCI port by writing a 1 to the SW RESET bit. At system reset, the SW RESET bit equals 0.
**Serial Communications Interface (SCI)**

**SCI Data Timing**
- Start bit valid if 4 consecutive SCICLK periods of zero bits after falling edge
- Majority vote taken on 4th, 5th, and 6th SCICLK cycles

![SCI Data Timing Diagram]

**Multiprocessor Wake-Up Modes**
- Allows numerous processors to be hooked up to the bus, but transmission occurs between only two of them
- *Idle-line or Address-bit modes*
- **Sequence of Operation**
  1. Potential receivers set SLEEP = 1, which disables RXINT except when an address frame is received
  2. All transmissions begin with an address frame
  3. Incoming address frame temporarily wakes up all SCIs on bus
  4. CPUs compare incoming SCI address to their SCI address
  5. Process following data frames only if address matches
Idle-Line Wake-Up Mode

- Idle time separates blocks of frames
- Receiver wakes up when SCIRXD high for 10 or more bit periods
- Two transmit address methods
  - Deliberate software delay of 10 or more bits
  - Set TXWAKE bit to automatically leave exactly 11 idle bits

Address-Bit Wake-Up Mode

- All frames contain an extra address bit
- Receiver wakes up when address bit detected
- Automatic setting of Addr/Data bit in frame by setting TXWAKE = 1 prior to writing address to SCITXBUF
The SCI interrupt logic generates interrupt flags when it receives or transmits a complete character as determined by the SCI character length. This provides a convenient and efficient way of timing and controlling the operation of the SCI transmitter and receiver. The interrupt flag for the transmitter is TXRDY (SCICTL2.7), and for the receiver RXRDY (SCIRXST.6). TXRDY is set when a character is transferred to TXSHF and SCITXBUF is ready to receive the next character. In addition, when both the SCIBUF and TXSHF registers are empty, the TX EMPTY flag (SCICTL2.6) is set. When a new character has been received and shifted into SCIRXBUF, the RXRDY flag is set. In addition, the BRKDT flag is set if a break condition occurs. A break condition is where the SCIRXD line remains continuously low for at least ten bits, beginning after a missing stop bit. Each of the above flags can be polled by the CPU to control SCI operations, or interrupts associated with the flags can be enabled by setting the RX/BK INT ENA (SCICTL2.1) and/or the TX INT ENA (SCICTL2.0) bits active high.

Additional flag and interrupt capability exists for other receiver errors. The RX ERROR flag is the logical OR of the break detect (BRKDT), framing error (FE), receiver overrun (OE), and parity error (PE) bits. RX ERROR high indicates that at least one of these four errors has occurred during transmission. This will also send an interrupt request to the CPU if the RX ERR INT ENA (SCICTL1.6) bit is set.
**SCI Registers**

**SCI Baud Rate Registers**

\[
\text{SCI baud rate} = \begin{cases} 
\frac{LSPCLK}{(BRR + 1) \times 8}, & \text{BRR = 1 to 65535} \\
\frac{LSPCLK}{16}, & \text{BRR = 0}
\end{cases}
\]

**Baud-Select MSbyte Register (SciRegs.SCIHBAUD)**

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAUD15</td>
<td>BAUD14</td>
<td>BAUD13</td>
<td>BAUD12</td>
<td>BAUD11</td>
<td>BAUD10</td>
<td>BAUD9</td>
<td>BAUD8</td>
</tr>
</tbody>
</table>

**Baud-Select LSbyte Register (SciRegs.SCILBAUD)**

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAUD7</td>
<td>BAUD6</td>
<td>BAUD5</td>
<td>BAUD4</td>
<td>BAUD3</td>
<td>BAUD2</td>
<td>BAUD1</td>
<td>BAUD0 (LSB)</td>
</tr>
</tbody>
</table>

**Baud Rate Determination**: The values in the baud-select registers (SCIHBAUD and SCILBAUD) concatenate to form a 16 bit number that specifies the baud rate for the SCI.

- For BRR = 1 to 65535: \( \text{SCI Baud Rate} = \frac{LSPCLK}{(BRR + 1) \times 8} \) bits/sec
- For BRR = 0: \( \text{SCI Baud Rate} = \frac{LSPCLK}{16} \) bits/sec

Max data rate = 5 Mbps @ 80 MHz

Note that the CLKOUT for the SCI module is one-half the CPU clock rate.
Select SCI Registers

- **Control 1** \texttt{SciRegs.SCICTL1}
  - Reset, Transmitter / Receiver Enable
  - TX Wake-up, Sleep, RX Error Interrupt Enable
- **Control 2** \texttt{SciRegs.SPICLTL2}
  - TX Buffer Full / Empty Flag, TX Ready Interrupt Enable
  - RX Break Interrupt Enable
- **Receiver Status** \texttt{SciRegs.SCIRXST}
  - Error Flag, Ready, Flag Break-Detect Flag, Framing Error Detect Flag, Parity Error Flag, RX Wake-up Detect Flag
- **FIFO Transmit** \texttt{SciRegs.SCIFFTX}
- **FIFO Receive** \texttt{SciRegs.SCIFFRX}
  - FIFO Enable, FIFO Reset
  - FIFO Over-flow flag, Over-flow Clear
  - Number of Words in FIFO (FIFO Status)
  - FIFO Interrupt Enable, Interrupt Status, Interrupt Clear
  - FIFO Interrupt Level (Number of Words in FIFO)

Note: refer to the reference guide for a complete listing of registers

SCI Summary

- **Asynchronous communications format**
- **65,000+ different programmable baud rates**
- **Two wake-up multiprocessor modes**
  - Idle-line wake-up & Address-bit wake-up
- **Programmable data word format**
  - 1 to 8 bit data word length
  - 1 or 2 stop bits
  - even/odd/no parity
- **Error Detection Flags**
  - Parity error; Framing error; Overrun error; Break detection
- **Transmit FIFO and receive FIFO**
- **Individual interrupts for transmit and receive**
Multichannel Buffered Serial Port (McBSP)

McBSP Block Diagram

Definition: Bit, Word, and Frame

Definition: Bit and Word

- “Bit” - one data bit per serial clock period
- “Word” or “channel” contains number of bits (8, 12, 16, 20, 24, 32)
**Definition: Word and Frame**

- **“Frame”** - contains one or multiple words
- **Number of words per frame**: 1-128

---

**Multi-Channel Selection**

- Allows multiple channels (words) to be independently selected for transmit and receive (e.g. only enable Ch0, 5, 27 for receive, then process via CPU)
- The McBSP keeps time sync with all channels, but only “listens” or “talks” if the specific channel is enabled (reduces processing/bus overhead)
- Multi-channel mode controlled primarily via two registers:
  - Multi-channel Control Reg
  - Rec/Xmt Channel Enable Regs
- Up to 128 channels can be enabled/disabled
McBSP Summary

- Independent clocking and framing for transmit and receive
- Internal or external clock and frame sync
- Data size of 8, 12, 16, 20, 24, or 32 bits
- TDM mode - up to 128 channels
  - Used for T1/E1 interfacing
- μ-law and A-law companding
- SPI mode
- Direct Interface to many codecs
- Can be serviced by the DMA
Inter-Integrated Circuit (I2C)

- Philips I2C-bus specification compliant, version 2.1
- Data transfer rate from 10 kbps up to 400 kbps
- Each device can be considered as a Master or Slave
- Master initiates data transfer and generates clock signal
- Device addressed by Master is considered a Slave
- Multi-Master mode supported
- Standard Mode – send exactly n data values (specified in register)
- Repeat Mode – keep sending data values (use software to initiate a stop or new start condition)

I2C Block Diagram
I2C Operating Modes and Data Formats

### I2C Operating Modes

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slave-receiver mode</td>
<td>Module is a slave and receives data from a master (all slaves begin in this mode)</td>
</tr>
<tr>
<td>Slave-transmitter mode</td>
<td>Module is a slave and transmits data to a master (can only be entered from slave-receiver mode)</td>
</tr>
<tr>
<td>Master-receiver mode</td>
<td>Module is a master and receives data from a slave (can only be entered from master-transmit mode)</td>
</tr>
<tr>
<td>Master-transmitter mode</td>
<td>Module is a master and transmits to a slave (all masters begin in this mode)</td>
</tr>
</tbody>
</table>

### I2C Serial Data Formats

#### 7-Bit Addressing Format

```
1 7 1 1 n 1 n 1 1
```

<table>
<thead>
<tr>
<th>S</th>
<th>Slave Address</th>
<th>R/W</th>
<th>ACK</th>
<th>Data</th>
<th>ACK</th>
<th>Data</th>
<th>ACK</th>
<th>P</th>
</tr>
</thead>
</table>

#### 10-Bit Addressing Format

```
1 7 1 1 8 1 n 1 1
```

<table>
<thead>
<tr>
<th>S</th>
<th>11110AA</th>
<th>R/W</th>
<th>ACK</th>
<th>AAAAAAAA</th>
<th>ACK</th>
<th>Data</th>
<th>ACK</th>
<th>P</th>
</tr>
</thead>
</table>

#### Free Data Format

```
1 n 1 n 1 n 1 1
```

<table>
<thead>
<tr>
<th>S</th>
<th>Data</th>
<th>ACK</th>
<th>Data</th>
<th>ACK</th>
<th>Data</th>
<th>ACK</th>
<th>P</th>
</tr>
</thead>
</table>

- **R/W = 0** – master writes data to addressed slave
- **R/W = 1** – master reads data from the slave
- **n = 1 to 8 bits**
- **S = Start** (high-to-low transition on SDA while SCL is high)
- **P = Stop** (low-to-high transition on SDA while SCL is high)
I2C Arbitration

- Arbitration procedure invoked if two or more master-transmitters simultaneously start transmission
  - Procedure uses data presented on serial data bus (SDA) by competing transmitters
  - First master-transmitter which drives SDA high is overruled by another master-transmitter that drives SDA low
  - Procedure gives priority to the data stream with the lowest binary value

![Diagram of I2C Arbitration]

I2C Summary

- Compliance with Philips I2C-bus specification (version 2.1)
- 7-bit and 10-bit addressing modes
- Configurable 1 to 8 bit data words
- Data transfer rate from 10 kbps up to 400 kbps
- Transmit FIFO and receive FIFO
Universal Serial Bus (USB)

Universal Serial Bus (USB) Controller

- Complies with USB 2.0 Implementers Forum certification standards
- Full-speed (12 Mbps) operation in Device mode; Full-/low-speed (12 Mbps / 1.5 Mbps) operation in Host mode
- Integrated PHY
- Efficient transfers using direct memory access controller (DMA)
  - All six endpoints can trigger separate DMA events
  - Channel requests asserted when FIFO contains required amount of data

USB

- Formed by the USB Implementers Forum (USB-IF)
  - http://www.usb.org
- USB-IF has defined standardized interfaces for common USB application, known as Device Classes
  - Human Interface Device (HID)
  - Mass Storage Class (MSC)
  - Communication Device Class (CDC)
  - Device Firmware Upgrade (DFU)
  - Refer to USB-IF Class Specifications for more information

- USB is:
  - Differential
  - Asynchronous
  - Serial
  - NRZI Encoded
  - Bit Stuffed
- USB is a HOST centric bus!
### USB Communication

<table>
<thead>
<tr>
<th><strong>USB Communication</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>♦ A component on the bus is either a…</td>
</tr>
<tr>
<td>♦ Host (the master)</td>
</tr>
<tr>
<td>♦ Device (the slave) – also known as peripheral or function</td>
</tr>
<tr>
<td>♦ Hub (neither master nor slave; allows for expansion)</td>
</tr>
<tr>
<td>♦ Communication model is heavily master/slave</td>
</tr>
<tr>
<td>♦ As opposed to peer-to-peer/networking (i.e. 1394/Firewire)</td>
</tr>
<tr>
<td>♦ Master runs the entire bus</td>
</tr>
<tr>
<td>♦ Only the master keeps track of other devices on bus</td>
</tr>
<tr>
<td>♦ Only the master can initiate transactions</td>
</tr>
<tr>
<td>♦ Slave simply responds to host commands</td>
</tr>
<tr>
<td>♦ This makes USB simpler, and cheaper to implement</td>
</tr>
</tbody>
</table>

### Enumeration

<table>
<thead>
<tr>
<th><strong>Enumeration</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>♦ USB is universal because of <em>Enumeration</em></td>
</tr>
<tr>
<td>♦ Process in which a Host attempts to identify a Device</td>
</tr>
<tr>
<td>♦ If no device attached to a downstream port, then the port sees Hi-Z</td>
</tr>
<tr>
<td>♦ When full-speed device is attached, it pulls up D+ line</td>
</tr>
<tr>
<td>♦ When the Host see a Device, it polls for <em>descriptor</em> information</td>
</tr>
<tr>
<td>♦ Essentially asking, “what are you?”</td>
</tr>
<tr>
<td>♦ Descriptors contain information the host can use to identify a driver</td>
</tr>
</tbody>
</table>
F2806x USB Hardware

The USB controller requires a total of three signals (D+, D-, and VBus) to operate in device mode and two signals (D+, D-) to operate in embedded host mode.

- VBus implemented in software using external interrupt or polling
  - GPIOs are NOT 5V tolerant
  - Make them tolerant using 100k and internal device ESD diode clamps

Note: (1) VBus sensing is only required in self-powered applications
(2) Device pins D+ and D- have special buffers to support the high speed requirements of USB; therefore their position on the device is not user-selectable

USB Controller Summary

- Complies with USB 2.0 specifications
- Full-speed (12 Mbps) Device controller
- Full-/Low-speed (12 Mbps/1.5 Mbps) Host controller
- Can be accessed via DMA
- Full software library with application examples is provided within ControlSUITE™
- Only available on TMS320F2806xU devices
Enhanced Controller Area Network (eCAN)

Controller Area Network (CAN)
A Multi-Master Serial Bus System

- CAN 2.0B Standard
- High speed (up to 1 Mbps)
- Add a node without disturbing the bus (number of nodes not limited by protocol)
- Less wires (lower cost, less maintenance, and more reliable)
- Redundant error checking (high reliability)
- No node addressing (message identifiers)
- Broadcast based signaling

CAN does not use physical addresses to address stations. Each message is sent with an identifier that is recognized by the different nodes. The identifier has two functions – it is used for message filtering and for message priority. The identifier determines if a transmitted message will be received by CAN modules and determines the priority of the message when two or more nodes want to transmit at the same time.
CAN Bus and Node

**CAN Bus**

- Two wire differential bus (usually twisted pair)
- Max. bus length depend on transmission rate
  - 40 meters @ 1 Mbps

![CAN Bus Diagram]

The MCU communicates to the CAN Bus using a transceiver. The CAN bus is a twisted pair wire and the transmission rate depends on the bus length. If the bus is less than 40 meters the transmission rate is capable up to 1 Mbit/second.

**CAN Node**

*Wired-AND Bus Connection*

![CAN Node Diagram]
Principles of Operation

- Data messages transmitted are identifier based, not address based.
- Content of message is labeled by an identifier that is unique throughout the network.
  - (e.g. rpm, temperature, position, pressure, etc.)
- All nodes on network receive the message and each performs an acceptance test on the identifier.
- If message is relevant, it is processed (received); otherwise it is ignored.
- Unique identifier also determines the priority of the message.
  - (lower the numerical value of the identifier, the higher the priority)
- When two or more nodes attempt to transmit at the same time, a non-destructive arbitration technique guarantees messages are sent in order of priority and no messages are lost.

Non-Destructive Bitwise Arbitration

- Bus arbitration resolved via arbitration with wired-AND bus connections.
  - Dominate state (logic 0, bus is high)
  - Recessive state (logic 1, bus is low)

![Diagram showing arbitration process]

- Node A wins arbitration.
- Node B loses arbitration.
- Node C loses arbitration.
Message Format and Block Diagram

**CAN Message Format**

- Data is transmitted and received using Message Frames
- 8 byte data payload per message
- Standard and Extended identifier formats

- **Standard Frame: 11-bit Identifier (CAN v2.0A)**

```
<table>
<thead>
<tr>
<th>Arbitration Field</th>
<th>Control Field</th>
<th>Data Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>11-bit Identifier</td>
<td>R T D E r0</td>
<td>0...8 Bytes Data CRC ACK EOF</td>
</tr>
</tbody>
</table>
```

- **Extended Frame: 29-bit Identifier (CAN v2.0B)**

```
<table>
<thead>
<tr>
<th>Arbitration Field</th>
<th>Control Field</th>
<th>Data Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>11-bit Identifier</td>
<td>S R D I E r1</td>
<td>0...8 Bytes Data CRC ACK EOF</td>
</tr>
</tbody>
</table>
```

The MCU CAN module is a full CAN Controller. It contains a message handler for transmission and reception management, and frame storage. The specification is CAN 2.0B Active – that is, the module can send and accept standard (11-bit identifier) and extended frames (29-bit identifier).
The CAN controller module contains 32 mailboxes for objects of 0 to 8-byte data lengths:
- configurable transmit/receive mailboxes
- configurable with standard or extended identifier

The CAN module mailboxes are divided into several parts:
- MID – contains the identifier of the mailbox
- MCF (Message Control Field) – contains the length of the message (to transmit or receive) and the RTR bit (Remote Transmission Request – used to send remote frames)
- MDL and MDH – contains the data

The CAN module contains registers which are divided into five groups. These registers are located in data memory from 0x006000 to 0x0061FF. The five register groups are:
- Control & Status Registers
- Local Acceptance Masks
- Message Object Time Stamps
- Message Object Timeout
- Mailboxes
Enhanced Controller Area Network (eCAN)

**eCAN Summary**

- Fully compliant with CAN standard v2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Programmable receive mask
  - Uses 32-bit time stamp on messages
  - Programmable interrupt scheme (two levels)
  - Programmable alarm time-out
- Programmable wake-up on bus activity
- Self-test mode
Development Support

Introduction

This module contains various references to support the development process.

Module Objectives

- TI Workshops Download Site
- controlSUITE™
- TI Development Tools
- Additional Resources
  - Product Information Center
  - On-line support
Module Topics

Development Support.........................................................................................................................14-1

Module Topics..................................................................................................................................14-2

TI Support Resources.........................................................................................................................14-3
   C2000 Workshop Download Wiki .................................................................................................14-3
   controlSUITE™ ..........................................................................................................................14-4
   C2000 Experimenter’s Kits ............................................................................................................14-5
   F28335 Peripheral Explorer Kit ....................................................................................................14-6
   C2000 controlSTICK Evaluation Tool .........................................................................................14-7
   C2000 LaunchPad Evaluation Kit .................................................................................................14-8
   C2000 controlCARD Application Kits .........................................................................................14-9
   Product Information Resources ..................................................................................................14-10
At the C2000 Workshop Download Wiki you will find all of the materials for the C2000 One-day and Multi-day Workshops, as well as the C2000 archived workshops, which include support for the F2407, F2812, F2808, and F28335 device families.
controlSUITE™

controlSUITE™ is a single portal for all C2000 software and has been designed to minimize software development time. Included in controlSUITE are device-specific drivers and support software, as well as complete system design examples used in sophisticated applications.

controlSUITE is a one-stop, single centralized location to find all of your C2000 software needs. Download controlSUITE from the TI website.
C2000 Experimenter’s Kits

The C2000 development kits are designed to be modular and robust. These kits are complete, open source, evaluation and development tools where the user can modify both the hardware and software to best fit their needs.

The various Experimenter’s Kits shown on this slide include a specific controlCARD and Docking Station. Most have onboard USB JTAG emulation and no external emulator or power supply is required. However, where noted, the kits based on a DIMM-168 controlCARD include a 5-volt power supply and require an external JTAG emulator.
F28335 Peripheral Explorer Kit

The Peripheral Explorer Kit provides a simple way to learn and interact with all F28335 peripherals. It includes onboard USB JTAG emulation.
C2000 controlSTICK Evaluation Tool

- Low-cost USB evaluation tool
- Onboard JTAG Emulation
  - JTAG emulator not required
- Access to controlSTICK signals
- C2000 Applications Software CD with example code and full hardware details
- Code Composer Studio
- Available through TI authorized distributors and the TI eStore

Part Number:
- TMDX28069USB
- TMDS28027USB

The controlSTICK is an entry-level evaluation kit. It is a simple, stand-alone tool that allows users to learn the device and software quickly and easily.
The LaunchPad is a low-cost evaluation kit. Like the controlSTICK, it is a simple, stand-alone tool that allows users to learn the device and software quickly and easily. Additionally, various BoosterPacks are available.
C2000 controlCARD Application Kits

The controlCARD based Application Kits demonstrate the full capabilities of the C2000 device in an application. All kits are completely open source with full documentation.
Product Information Resources

For More Information . . .

- USA – Product Information Center (PIC)
  - Phone: 800-477-8924 or 512-434-1560
  - E-mail: support@ti.com
- TI E2E Community (videos, forums, blogs)
  - http://e2e.ti.com
- Embedded Processor Wiki
  - http://processors.wiki.ti.com
- TI Training
  - http://www.ti.com/training
- TI eStore
  - http://estore.ti.com
- TI website
  - http://www.ti.com

For more information and support, you can contact the product information center, visit the TI E2E community, embedded processor Wiki, TI training web page, TI eStore, and the TI website.
Module Topics

Appendix A – Experimenter’s Kit

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</table>
F28069 controlCARD

F28069 PCB Outline (Top View)

LD1 / LD2 / LD3

LD1 – Turns on when controlCARD is powered on
LD2 – Controlled by GPIO-31
LD3 – Controlled by GPIO-34

SW1

SW1 – controls the boot options of the F28069 device

<table>
<thead>
<tr>
<th>Position 1 (GPIO-34)</th>
<th>Position 2 (TDO)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Parallel I/O</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Wait mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SCI</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(default) Get mode; the default get mode is boot from FLASH</td>
</tr>
</tbody>
</table>
SW2 - ADC VREF control
The ADC will by default convert from 0 to 3.3V and scale this to 0-4096 ADC counts, however if the ADC (in software) is configured to use external references, the ADC will convert its full range of resolution (0-4096) from VREF-LO to VREF-HI.

Position 1 controls VREF-HI, the value that the ratiometric ADC will convert as the maximum 12-bit value, 0x0FFF. In the downward position, VREF-HI will be connected to 3.3V. In the upward position, VREF-HI will be connected to pin 66 of the DIMM100-socket. This will allow a connecting board to control the ADC-VREFHI value.

Position 2 controls VREF-LO, the value that the ratiometric ADC will convert as the minimum 12-bit value, 0x0000. In the downward position, VREF-LO will be connected to 0V. In the upward position, VREF-LO will be connected to pin 16 of the DIMM100-socket. This will allow a connecting board to control the ADC-VREFLO value.
F28035 controlCARD

F28035 PCB Outline (Top View)

LD1 / LD2 / LD3

LD1 – Turns on when controlCARD is powered on
LD2 – Controlled by GPIO-31
LD3 – Controlled by GPIO-34

SW1

SW1 – controls whether on-card RS-232 connection is enabled or disabled.
- ON – RS-232 transceiver will be enabled and allow communication through a serial cable via pins 2 and 42 of the DIMM-100 socket. Putting SW1 in the “ON” position will allow the F28035 controlCARD to be card compatible with the F2808, F28044, F28335, and F28027 controlCARDs. GPIO-28 will be stuck as logic high in this position.
- OFF – The default option. SW1 in the “OFF” position allows GPIO-28 to be used as a GPIO. Serial communication is still possible, however an external transceiver such as the FTDI – FT2232D chip.
SW2

SW2 – controls the boot options of the F28035 device

<table>
<thead>
<tr>
<th>Position 1 (GPIO-34)</th>
<th>Position 2 (TDO)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Parallel I/O</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Wait mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SCI</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(default) Get mode; the default get mode is boot from FLASH</td>
</tr>
</tbody>
</table>

SW3

SW3 – ADC VREF control

The ADC will by default convert from 0 to 3.3V, however if in the ADC registers the ADC is configured to use external limits the ADC will convert its full range of resolution from VREF-LO to VREF-HI.

Position 1 controls VREF-HI, the value that the ratiometric ADC will convert as the maximum 12-bit value, 0x0FFF. In the downward position, VREF-HI will be connected to 3.3V. In the upward position, VREF-HI will be connected to pin 66 of the DIMM100-socket. This would allow a connecting board to control the ADC-VREFHI value.

Position 2 controls VREF-LO, the value that the ratiometric ADC will convert as the minimum 12-bit value, 0x0000. In the downward position, VREF-LO will be connected to 0V. In the upward position, VREF-LO will be connected to pin 16 of the DIMM100-socket. This would allow a connecting board to control the ADC-VREFLO value.
F28335 controlCARD

F28335 PCB Outline (Top View)

PGF – Release 1.x

SW1  SW2

LD1  LD2  LD3

ZJZ – Release 2.x

SW1  SW2

LD1  LD2  LD3
Note: Older versions of the F28335 controlCARD do not include SW1 or SW2.

**LD1 / LD2 / LD3**

LD1 – Turns on when controlCARD is powered on  
LD2 – Controlled by GPIO-31  
LD3 – Controlled by GPIO-34

**SW1**

SW1 – controls whether on-card RS-232 connection is enabled or disabled. 
- ON – RS-232 transceiver will be enabled and allow communication through a serial cable via pins 2 and 42 of the DIMM-100 socket. Putting SW1 in the “ON” position will allow the F28335 controlCARD to be card compatible with the F2808, F28044, F28035, and F28027 controlCARDs. GPIO-28 will be stuck as logic high in this position.  
- OFF – SW1 in the “OFF” position allows GPIO-28 to be used as a GPIO. Serial communication is still possible, however an external transceiver is needed such as the FTDI – FT2232D chip.  
  - This is primarily used for communicating over the USB to serial bridge included in the onboard XDS100 JTAG emulation on many C2000 development boards.
SW2

SW2 – controls the boot options of the F28335 device.

The boot options used in this workshop are shown below:

<table>
<thead>
<tr>
<th>Position 1 (GPIO-84)</th>
<th>Position 2 (GPIO-85)</th>
<th>Position 3 (GPIO-86)</th>
<th>Position 4 (GPIO-87)</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>SARAM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>FLASH</td>
</tr>
</tbody>
</table>

For a complete list of boot mode options see the F2833x Boot Mode Selection table in the Docking Station section in this appendix.

Some earlier versions of the F28335 controlCARD use the ZJZ (a BGA) package. These are functionally equivalent to versions that use the PFG package.
Docking Station

SW1 / LD1
SW1 – USB: Power from USB; ON – Power from JP1
LD1 – Power-On indicator

JP1 / JP2
JP1 – 5.0 V power supply input
JP2 – USB JTAG emulation port

J1 – ControlCARD 100-pin DIMM socket
J2 – JTAG header connector
J3 – UART communications header connector
J8 – Internal emulation enable/disable jumper (NO jumper for internal emulation)
J9 – User virtual COM port to C2000 device (Note: ControlCARD would need to be modified to disconnect the C2000 UART connection from header J3)

*Note: Jumper Left = 1; Jumper Right = 0
Note: The internal emulation logic on the Docking Station routes through the FT2232 USB device. By default this device enables the USB connection to perform JTAG communication and in parallel create a virtual serial port (SCI/UART). As shipped, the C2000 device is not connected to the virtual COM port and is instead connected to J3.

F2833x Boot Mode Selection

<table>
<thead>
<tr>
<th>MODE</th>
<th>GPIO87/XA15</th>
<th>GPIO86/XA14</th>
<th>GPIO85/XA13</th>
<th>GPIO84/XA12</th>
<th>MODE[1]</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Jump to Flash</td>
</tr>
<tr>
<td>E</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>SCI-A boot</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>SPI-A boot</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>I2C-A boot</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>eCAN-A boot</td>
</tr>
<tr>
<td>A</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>McDSP-A boot</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Jump to XINTF x16</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Jump to XINTF x32</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Jump to OTP</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Parallel GPIO I/O boot</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Parallel XINTF boot</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Jump to SARAM</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Branch to check boot mode</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Branch to Flash, skip ADC calibration</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Branch to SARAM, skip ADC calibration</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Branch to SCI, skip ADC calibration</td>
</tr>
</tbody>
</table>

[1] All four GPIO pins have an internal pullup.

F280xx Boot Mode Selection

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>GPIO18 SPICLK[1]</th>
<th>GPIO29 SCI TXDA</th>
<th>GPIO34</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boot to Flash[2]</td>
<td>Jump to flash address 0x0F 7F08. You must have programmed a branch instruction here prior to reset to redirect code execution as desired.</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SCI-A Boot</td>
<td>Load a data stream from SCI-A.</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>SPI-A Boot</td>
<td>Load from an external SPI EEPROM on SPI-A.</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>PC Boot</td>
<td>Load data from an external EEPROM at address 0x50 on the PC bus.</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>eCAN-A Boot[3]</td>
<td>Call CAN_Boot to load from eCAN-A mailbox 1.</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Boot to M0 SARAM[4]</td>
<td>Jump to M0 SARAM address 0x00 0000.</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Boot to OTP[4]</td>
<td>Jump to OTP address 0x3D 7800.</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Parallel I/O Boot</td>
<td>Load data from GPIO00 - GPIO15.</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

[1] You must take extra care because of any effect toggling SPICLK[1] to select a boot mode may have on external logic.
[2] When booting directly to flash, it is assumed that you have previously programmed a boot statement at 0x0F 7F08 to redirect program flow as desired.
[3] On devices that do not have an eCAN-A module this configuration is reserved. If this is selected, then the eCAN-A bootloader will run and will loop forever waiting for an incoming message.
[4] When booting directly to OTP or M0 SARAM, it is assumed that you have previously programmed or loaded code starting at the entry point location.
**J3 – DB-9 to 4-Pin Header Cable**

*Note:* This cable is NOT included with the Experimenter’s Kit and is only shown for reference.

**Pin-Out Table for Both Ends of the Cable:**

<table>
<thead>
<tr>
<th>DB-9 Male</th>
<th>SIL 0.1” female</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin#</td>
<td>Pin#</td>
</tr>
<tr>
<td>2 (black)</td>
<td>1 (TX)</td>
</tr>
<tr>
<td>3 (red)</td>
<td>4 (RX)</td>
</tr>
<tr>
<td>5 (bare wire)</td>
<td>3 (GND)</td>
</tr>
</tbody>
</table>

*Note: pin 2 on SIL is a no-connect*