C2000™ Piccolo™ 1-Day Workshop

Workshop Guide and Lab Manual
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Workshop Introduction

C2000™ Piccolo™ 1-Day Workshop

Texas Instruments
Technical Training

C2000 Piccolo 1-Day Workshop Outline

- Workshop Introduction
- Architecture Overview
- Programming Development Environment
  - Lab: Linker command file
- Peripheral Register Header Files
- Reset, Interrupts and System Initialization
  - Lab: Watchdog and interrupts
- Control Peripherals
  - Lab: Generate and graph a PWM waveform
- Flash Programming
  - Lab: Run the code from flash memory
- The Next Step…
Introductions

- Name
- Company
- Project Responsibilities
- DSP / Microcontroller Experience
- TI Processor Experience
- Hardware / Software - Assembly / C
- Interests

TI Embedded Processing Portfolio

<table>
<thead>
<tr>
<th>TI Embedded Processors</th>
<th>Microcontrollers (MCUs)</th>
<th>ARM®-Based Processors</th>
<th>Digital Signal Processors (DSPs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2000™ Delfino™ Piccolo™</td>
<td>Up to 25 MHz</td>
<td>32-bit real-time MCUs</td>
<td>32-bit ARM Cortex™-M3 MCUs</td>
</tr>
<tr>
<td>MSP430™</td>
<td>Up to 8 MHz</td>
<td>ARM Cortex-A8 MPUs</td>
<td>DSP DSP+ARM</td>
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<tr>
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<td>Up to 1000 MHz</td>
<td>MSP430™</td>
<td>Multi-core DSP</td>
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<tr>
<td>C6000™ DaVinci™</td>
<td>Up to 250 MHz</td>
<td>OMAP™</td>
<td>Ultra Low power DSP</td>
</tr>
<tr>
<td>C5000™</td>
<td>Up to 1 GHz</td>
<td>OMAP™</td>
<td></td>
</tr>
</tbody>
</table>
**Workshop Introduction**

C2000 Portfolio Expanding with Price/Performance Optimized Derivatives

- **High-Precision Control**
  - C2834x 300 MIPS
- **Control Performance**
  - F2833x/23x 150 MIPS
  - F281x 150 MIPS
  - F280x/xx 100 MIPS
  - F2803x/2x 60 MIPS
- **Multi-Function, Appliance & Consumer Control**
  - F24xx 40 MIPS

**Broad C2000 Application Base**

- **Renewable Energy Generation**
- **Telecom Digital Power**
- **AC Drives, Industrial & Consumer Motor Control**
- **Power Line Communications**
- **Automotive Radar, Electric Power Steering & Digital Power**
- **Consumer, Medical & Non-traditional**
- **LED Lighting**
**Workshop Introduction**

**C2000 Piccolo™ Microcontroller Family**

### F2802x / F2803x

<table>
<thead>
<tr>
<th></th>
<th>MHz</th>
<th>Flash (x16)</th>
<th>RAM (x16)</th>
<th>CLA</th>
<th>Analog Comp*</th>
<th>ADC* (ch)</th>
<th>PWM / (HR)*</th>
<th>CAP</th>
<th>QEP</th>
<th>Communication Ports</th>
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<td>F28020</td>
<td>40</td>
<td>8Kw</td>
<td>3Kw</td>
<td>No</td>
<td>1 / 2</td>
<td>7 / 13</td>
<td>8 (0)</td>
<td>0</td>
<td>0</td>
<td>SPI, SCI, I2C</td>
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<tr>
<td>F28020</td>
<td>40</td>
<td>16Kw</td>
<td>3Kw</td>
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<td>1 / 2</td>
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<td>32Kw</td>
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<td>7 / 13</td>
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<td>50</td>
<td>16Kw</td>
<td>6Kw</td>
<td>No</td>
<td>1 / 2</td>
<td>7 / 13</td>
<td>8 (4)</td>
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<td>0</td>
<td>SPI, SCI, I2C</td>
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<tr>
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<td>50</td>
<td>32Kw</td>
<td>6Kw</td>
<td>No</td>
<td>1 / 2</td>
<td>7 / 13</td>
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<tr>
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<td>60</td>
<td>16Kw</td>
<td>6Kw</td>
<td>No</td>
<td>1 / 2</td>
<td>7 / 13</td>
<td>8 (4)</td>
<td>1</td>
<td>0</td>
<td>SPI, SCI, I2C</td>
</tr>
<tr>
<td>F28027</td>
<td>60</td>
<td>32Kw</td>
<td>6Kw</td>
<td>No</td>
<td>1 / 2</td>
<td>7 / 13</td>
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<tr>
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<td>16Kw</td>
<td>6Kw</td>
<td>No</td>
<td>3</td>
<td>14 / 16</td>
<td>12(0) / 14(0)</td>
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<td>8Kw</td>
<td>No</td>
<td>3</td>
<td>14 / 16</td>
<td>12(0) / 14(0)</td>
<td>1</td>
<td>1</td>
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<td>10Kw</td>
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<td>14 / 16</td>
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<td>1</td>
<td>1</td>
<td>SPI, SCI, I2C, LIN, eCAN</td>
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<tr>
<td>F28033</td>
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<td>32Kw</td>
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<td>Yes</td>
<td>3</td>
<td>14 / 16</td>
<td>12(6) / 14(7)</td>
<td>1</td>
<td>1</td>
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<td>64Kw</td>
<td>10Kw</td>
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<td>3</td>
<td>14 / 16</td>
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<tr>
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<td>64Kw</td>
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<td>12(6) / 14(7)</td>
<td>1</td>
<td>1</td>
<td>SPI, SCI, I2C, LIN, eCAN</td>
</tr>
</tbody>
</table>

* number dependent on package type: F2802x – 38/48 pins, F2803x – 64/80 pins

- All devices have VREG, POR/BOR, Watchdog, OTP, CPU Timers

*For details and information on other C2000 family members refer to the "Embedded Processing Guide" and specific "Data Manuals"*

---

**Piccolo™ controlSTICK**

- LED LD1 (Power)
- LED LD2 (GPIO34)
- TMS320F28027 48-Pin Package
- USB JTAG Interface & Power
- On-board USB JTAG Emulation
- Peripheral Header Pins
Architecture Overview

TMS320F2802x/3x Block Diagram

Available only on TMS320F2803x devices: CLA, QEP, CAN, LIN

TMS320F28027 Memory Map

Dual Mapped: L0

CSM Protected:
L0, OTP
FLASH, ADC CAL,
Flash Regs in PF0
F28x Fast Interrupt Response Manager

- 96 dedicated PIE vectors
- No software decision making required
- Direct access to RAM vectors
- Auto flags update
- Concurrent auto context save

<table>
<thead>
<tr>
<th>Auto Context Save</th>
<th>T</th>
<th>ST0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AH</td>
<td>AL</td>
</tr>
<tr>
<td></td>
<td>PH</td>
<td>PL</td>
</tr>
<tr>
<td></td>
<td>AR1 (L)</td>
<td>AR0 (L)</td>
</tr>
<tr>
<td></td>
<td>DP</td>
<td>ST1</td>
</tr>
<tr>
<td></td>
<td>DBSTAT</td>
<td>IER</td>
</tr>
<tr>
<td></td>
<td>PC(msw)</td>
<td>PC(lsw)</td>
</tr>
</tbody>
</table>

Peripheral interrupts: 12x8 = 96

Interrupts: INT1 to INT12

PIE module
Per 96 interrupts

Auto Context Save

28x CPU Interrupt logic

28x CPU

IFR
IER
INTM
Programming Development Environment

Code Composer Studio

Code Composer Studio: IDE

- **Integrates**: edit, code generation, and debug
- **Single-click access** using buttons
- Powerful **graphing/profiling** tools
- Automated tasks using **Scripts**
- Built-in access to **BIOS** functions
- Based on the **Eclipse** open source software framework

C/C++ and Debug Perspective (CCSv4)

- Each perspective provides a set of functionality aimed at accomplishing a specific task

- **C/C++ Perspective**
  - Displays views used during code development
    - C/C++ project, editor, etc.

- **Debug Perspective**
  - Displays views used for debugging
    - Menus and toolbars associated with debugging, watch and memory windows, graphs, etc.
Programming Development Environment

CCSv4 Project

Project files contain:

- List of files:
  - Source (C, assembly)
  - Libraries
  - DSP/BIOS configuration file
  - Linker command files

- Project settings:
  - Build options (compiler, Linker, assembler, and DSP/BIOS)
  - Build configurations

Creating a New CCSv4 Project

1. File → New → CCS Project
2. Select a type of project
3. Additional Project Settings
4. Project Settings
CCSv4 Build Options – Compiler / Linker

**Compiler**
- 16 categories for code generation tools
- Controls many aspects of the build process, such as:
  - Optimization level
  - Target device
  - Compiler / assembly / link options

**Linker**
- 9 categories for linking
  - Specify various link options
  - `${PROJECT_ROOT}` specifies the current project directory

### Linking Sections in Memory

#### Sections
- All code consists of different parts called **sections**
- All default section names begin with “." 
- The compiler has default section names for *initialized* and *uninitialized* sections

```c
int x = 2;
int y = 7;

void main(void) {
    long z;
    z = x + y;
}
```
Compiler Section Names

**Initialized Sections**

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Link Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>.text</td>
<td>code</td>
<td>FLASH</td>
</tr>
<tr>
<td>.cinit</td>
<td>initialization values for global and static variables</td>
<td>FLASH</td>
</tr>
<tr>
<td>.econst</td>
<td>constants (e.g. const int k = 3;)</td>
<td>FLASH</td>
</tr>
<tr>
<td>.switch</td>
<td>tables for switch statements</td>
<td>FLASH</td>
</tr>
<tr>
<td>.pinit</td>
<td>tables for global constructors (C++)</td>
<td>FLASH</td>
</tr>
</tbody>
</table>

**Uninitialized Sections**

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Link Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>.ebss</td>
<td>global and static variables</td>
<td>RAM</td>
</tr>
<tr>
<td>.stack</td>
<td>stack space</td>
<td>low 64Kw RAM</td>
</tr>
<tr>
<td>.esysmem</td>
<td>memory for far malloc functions</td>
<td>RAM</td>
</tr>
</tbody>
</table>

Note: During development initialized sections could be linked to RAM since the emulator can be used to load the RAM.

Placing Sections in Memory

- M0SARAM (0x400)
- M1SARAM (0x400)
- FLASH (0x8000)

**Sections**

- .ebss
- .stack
- .cinit
- .text
Linking

- Memory description
- How to place s/w into h/w

Link.cmd

.obj → Linker → .out

 Memory description

Linker Command File

MEMORY
{
    PAGE 0:    /* Program Memory */
        FLASH: origin = 0x3F0000, length = 0x8000

    PAGE 1:    /* Data Memory */
        M0SARAM: origin = 0x000000, length = 0x400
        M1SARAM: origin = 0x000400, length = 0x400
}

SECTIONS
{
    .text:>      FLASH      PAGE = 0
    .ebss:>      M0SARAM    PAGE = 1
    .cinit:>     FLASH      PAGE = 0
    .stack:>     M1SARAM    PAGE = 1
}
Lab 1: Linker Command File

Objective

Use a linker command file to link the C program file (Lab1.c) into the system described below.

System Description:
- TMS320F28027
- All internal RAM blocks allocated

Placement of Sections:
- .text into RAM Block L0SARAM on PAGE 0 (program memory)
- .cinit into RAM Block L0SARAM on PAGE 0 (program memory)
- .ebss into RAM Block M0SARAM on PAGE 1 (data memory)
- .stack into RAM Block M1SARAM on PAGE 1 (data memory)

Procedure

Start Code Composer Studio and Open a Workspace

1. Start Code Composer Studio (CCS) by double clicking the icon on the desktop or selecting it from the Windows Start menu. When CCS loads, a dialog box will prompt you for the location of a workspace folder. Use the default location for the workspace and click OK.
This folder contains all CCS custom settings, which includes project settings and views when CCS is closed so that the same projects and settings will be available when CCS is opened again. The workspace is saved automatically when CCS is closed.

2. The first time CCS opens a “Welcome to Code Composer Studio v4” page appears. Close the page by clicking on the CCS icon in the upper right or by clicking the X on the “Welcome” tab. You should now have an empty workbench. The term workbench refers to the desktop development environment. Maximize CCS to fill your screen.

The workbench will open in the “C/C++ Perspective” view. Notice the C/C++ icon in the upper right-hand corner. A perspective defines the initial layout views of the workbench windows, toolbars, and menus which are appropriate for a specific type of task (i.e. code development or debugging). This minimizes clutter to the user interface. The “C/C++ Perspective” is used to create or build C/C++ projects. A “Debug Perspective” view will automatically be enabled when the debug session is started. This perspective is used for debugging C/C++ projects.

Setup Target Configuration

3. Open the emulator target configuration dialog box. On the menu bar click:

Target → New Target Configuration...

In the file name field type F28027_ctrlSTK.ccxml. This is just a descriptive name since multiple target configuration files can be created. Leave the “Use shared location” box checked and select Finish.

4. In the next window that appears, select the emulator using the “Connection” pull-down list and choose “Texas Instruments XDS100v1 USB Emulator”. In the box below, check the box to select “controlSTICK – Piccolo F28027”. Click Save to save the configuration, then close the “Cheat Sheets” and “F28027_ctrlSTK.ccxml” setup window by clicking the X on the tabs.

5. To view the target configurations, click:

View → Target Configurations

and click the plus sign (+) to the left of User Defined. Notice that the F28027_ctrlSTK.ccxml file is listed and set as the default. If it is not set as the default, right-click on the .ccxml file and select “Set as Default”. Close the Target Configurations window by clicking the X on the tab.

Create a New Project

6. A project contains all the files you will need to develop an executable output file (.out) which can be run on the MCU hardware. To create a new project click:

File → New → CCS Project

In the Project name field type Lab1. Uncheck the “Use default location” box. Click the Browse… button and navigate to:
C:\C28x\Labs\Lab1\Project

Click OK and then click Next.

7. The next window that appears selects the platform and configurations. Select the “Project Type” using the pull-down list and choose “C2000”. In the “Configurations” box below, leave the “Debug” and “Release” boxes checked. This will create folders that will hold the output files. Click Next.

8. In the next window, inter-project dependencies (if any) are defined. Select Next.

9. In the last window, the CCS project settings are selected. Change the “Device Variant” using the pull-down list to “TMS320F28027”. Next, using the pull-down list change the “Linker Command File” to “<none>”. We will be using our own linker command file, rather than the one supplied by CCS. The “Runtime Support Library” will be automatically set to “rts2800_ml.lib”. This will select the large memory model runtime support library. Click Finish.

10. A new project has now been created. Notice the C/C++ Projects window contains Lab1. The project is set Active and the output files will be located in the Debug folder. At this point, the project does not include any source files. The next step is to add the source files to the project.

11. To add the source files to the project, right-click on Lab1 in the C/C++ Projects window and select:

Add Files to Project…

or click: Project ➔ Add Files to Active Project…

and make sure you’re looking in C:\C28x\Labs\Lab1\Files. With the “files of type” set to view all files (*.*) select Lab1.c and Lab1.cmd then click OPEN. This will add the files to the project.

12. In the C/C++ Projects window, click the plus sign (+) to the left of Lab1 and notice that the files are listed.

Project Build Options

13. There are numerous build options in the project. Most default option settings are sufficient for getting started. We will inspect a couple of the default options at this time. Right-click on Lab1 in the C/C++ Projects window and select Properties or click:

Project ➔ Properties

14. A “Properties” window will open and in the section on the left be sure that “C/C++ Build” category is selected. In the “Configuration Settings” section make sure that the Tool Settings tab is selected. Next, under “C2000 Linker” select the “Basic Options”. Notice that .out and .map files are being specified. The .out file is the executable code that will be loaded into the MCU. The .map file will contain a linker report showing memory usage and section addresses in memory.
15. Next in the “Basic Options” set the Stack Size to 0x200.

16. Under “C2000 Compiler” select the “Runtime Model Options”. Notice the “Use large memory model” and “Unified memory” boxes are checked. Select OK to save and close the Properties window.

**Linker Command File – Lab1.cmd**

17. Open and inspect Lab1.cmd by double clicking on the filename in the project window. Notice that the `Memory{}` declaration describes the system memory shown on the “Lab1: Linker Command File” slide in the objective section of this lab exercise. Memory block L0SARAM has been placed in program memory on page 0, and the other memory blocks have been placed in data memory on page 1.

18. In the `Sections{}` area notice that the sections defined on the slide have been “linked” into the appropriate memories. Also, notice that a section called .reset has been allocated. The .reset section is part of the rts2800_ml.lib, and is not needed. By putting the `TYPE = DSECT` modifier after its allocation, the linker will ignore this section and not allocate it. Close the inspected file.

**Build and Load the Project**

19. Three buttons on the horizontal toolbar control code generation. Hover your mouse over each button as you read the following descriptions:

<table>
<thead>
<tr>
<th>Button</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Build</td>
<td>Incremental build and link of only modified source files</td>
</tr>
<tr>
<td>2</td>
<td>Rebuild</td>
<td>Full build and link of all source files</td>
</tr>
<tr>
<td>3</td>
<td>Debug</td>
<td>Automatically build, link, load and launch debug-session</td>
</tr>
</tbody>
</table>

20. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window (we have deliberately put an error in Lab1.c). When you get an error, you will see the error message (in red) in the Problems window, and simply double-click the error message. The editor will automatically open to the source file containing the error, and position the mouse cursor at the correct code line.

21. Fix the error by adding a semicolon at the end of the “z = x + y” statement. For future knowledge, realize that a single code error can sometimes generate multiple error messages at build time. This was not the case here.

22. Build the project again. There should be no errors this time.

23. CCS can automatically save modified source files, build the program, open the debug perspective view, connect and download it to the target, and then run the program to the beginning of the main function. Click on the “Debug” button (green bug) or click Target → Debug Active Project.
Notice the Debug icon in the upper right-hand corner indicating that we are now in the “Debug Perspective” view. The program ran through the C-environment initialization routine in the rts2800_ml.lib and stopped at main() in Lab1.c.

**Debug Environment Windows**

It is standard debug practice to watch local and global variables while debugging code. There are various methods for doing this in Code Composer Studio. We will examine two of them here: memory windows, and watch windows.

24. Open a “Memory” window to view the global variable “z”.

   Click: View → Memory on the menu bar.

   Type &z into the address field and select “Data” memory page. Note that you must use the ampersand (meaning “address of”) when using a symbol in a memory window address box. Also note that Code Composer Studio is case sensitive.

   Set the properties format to “Hex 16 Bit – TI Style Hex” in the window. This will give you more viewable data in the window. You can change the contents of any address in the memory window by double-clicking on its value. This is useful during debug.

25. Notice the “Local(1)” window automatically opened and the local variables x and y are present. The local window will always contain the local variables for the code function currently being executed.

   (Note that local variables actually live on the stack. You can also view local variables in a memory window by setting the address to “SP” after the code function has been entered).

26. We can also add global variables to the watch window if desired. Let’s add the global variable “z”.

   Click the “Watch (1)” tab at the top of the watch window. In the empty box in the “Name” column, type z and then enter. An ampersand is not used here. The watch window knows you are specifying a symbol. (Note that the watch window can be manually opened by clicking: View → Watch Window on the menu bar).

   Check that the watch window and memory window both report the same value for “z”. Trying changing the value in one window, and notice that the value also changes in the other window.

**Single-stepping the Code**

27. Click the “Local (1)” tab at the top of the watch window. Single-step through main() by using the <F5> key (or you can use the Step Into button on the horizontal toolbar). Check to see if the program is working as expected. What is the value for “z” when you get to the end of the program?
**Terminate Debug Session and Close Project**

28. The **Terminate All** button will terminate the active debug session, close the debugger and return CCS to the “C/C++ Perspective” view.

Click: Target ➔ Terminate All or use the Terminate All icon: 🗑️

Close the Terminate Debug Session “Cheat Sheet” by clicking on the X on the tab.

29. Next, close the project by right-clicking on Lab1 in the C/C++ Projects window and select Close Project.

**End of Exercise**
Peripheral Register Header Files

Traditional Approach to C Coding

```c
#define ADCCTL1 (volatile unsigned int *)0x00007100

void main(void)
{
    *ADCCTL1 = 0x1234; //write entire register
    *ADCCTL1 |= 0x4000; //enable ADC module
}
```

Advantages
- Simple, fast and easy to type
- Variable names exactly match register names (easy to remember)

Disadvantages
- Requires individual masks to be generated to manipulate individual bits
- Cannot easily display bit fields in debugger window
- Will generate less efficient code in many cases

Structure Approach to C Coding

```c
void main(void)
{
    AdcRegs.ADCCTL1.all = 0x1234; //write entire register
    AdcRegs.ADCCTL1.bit.ADCENABLE = 1; //enable ADC module
}
```

Advantages
- Easy to manipulate individual bits
- Watch window is amazing! (next slide)
- Generates most efficient code (on C28x)

Disadvantages
- Can be difficult to remember the structure names (Editor Auto Complete feature to the rescue!)
- More to type (again, Editor Auto Complete feature to the rescue)
Structure Naming Conventions

- The DSP2802x header files define:
  - All of the peripheral structures
  - All of the register names
  - All of the bit field names
  - All of the register addresses

<table>
<thead>
<tr>
<th>Access Method</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PeripheralName.RegisterName.all</td>
<td>Access full 16 or 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.half.LSW</td>
<td>Access low 16-bits of 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.half.MSW</td>
<td>Access high 16-bits of 32-bit register</td>
</tr>
<tr>
<td>PeripheralName.RegisterName.bit.FieldName</td>
<td>Access specified bit fields of register</td>
</tr>
</tbody>
</table>

Notes:
1. “PeripheralName” are assigned by TI and found in the DSP2802x header files. They are a combination of capital and small letters (i.e. CpuTimer0Regs).
2. “RegisterName” are the same names as used in the data sheet. They are always in capital letters (i.e. TCR, TIM, TPR,...).
3. “FieldName” are the same names as used in the data sheet. They are always in capital letters (i.e. POL, TOG, TSS,...).

Editor Auto Complete to the Rescue!
**DSP2802x Header File Package**  
(http://www.ti.com, literature # SPRC832)

- Contains everything needed to use the structure approach
- Defines all peripheral register bits and register addresses
- Header file package includes:
  - `\DSP2802x_headers\include \rightarrow .h files`
  - `\DSP2802x_headers\cmd \rightarrow linker .cmd files`
  - `\DSP2802x_headers\gel \rightarrow .gel files for CCS`
  - `\DSP2802x_examples \rightarrow CCS3 examples`
  - `\DSP2802x_examples_ccsv4 \rightarrow CCS4 examples`
  - `\doc \rightarrow documentation`

### Peripheral Structure .h files (1 of 2)

- Contain bits field structure definitions for each peripheral register

**DSP2802x_Adc.h**

```c
#include "DSP2802x_Device.h"

Void InitAdc(void)
{
    /* Reset the ADC module */
    AdcRegs.ADCCTL1.bit.RESET = 1;
    /* configure the ADC register */
    AdcRegs.ADCCTL1.all = 0x00E4;
}
```

**Your C-source file (e.g., Adc.c)**

```c
#include "DSP2802x_Device.h"

Void InitAdc(void)
{
    /* Reset the ADC module */
    AdcRegs.ADCCTL1.bit.RESET = 1;
    /* configure the ADC register */
    AdcRegs.ADCCTL1.all = 0x00E4;
}
```

// ADC Individual Register Bit Definitions:
struct ADCCTL1_BITS {         // bits description
    Uint16  TEMPCONV:1;       // 0 Temperature sensor connection
    Uint16  VREFLOCONV:1;   // 1 VSSA connection
    Uint16  INTPULSEPOS:1;   // 2 INT pulse generation control
    Uint16  ADCREFSEL:1;      // 3 Internal/external reference select
    Uint16  rsvd1:1;                  // 4 reserved
    Uint16  ADCREFPWD:1;     // 5 Reference buffers powerdown
    Uint16  ADCBGPWD:1;       // 6 ADC bandgap powerdown
    Uint16  ADCPWDN:1;        // 7 ADC powerdown
    Uint16  ADCBSYCHN:5;      // 12:8 ADC busy on a channel
    Uint16  ADCBSY:1;        // 13 ADC busy signal
    Uint16  ADCENABLE:1;     // 14 ADC enable
    Uint16  RESET:1;                 // 15 ADC master reset
};

// Allow access to the bit fields or entire register:
union ADCCTL1_REG {
    Uint16  all;
    struct ADCCTL1_BITS  bit;
};

// ADC External References & Function Declarations:
extern volatile struct ADC_REGS AdcRegs;
```
Peripheral Structure .h files (2 of 2)

- The header file package contains a .h file for each peripheral in the device

<table>
<thead>
<tr>
<th>File</th>
<th>File</th>
<th>File</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP2802x_Adc.h</td>
<td>DSP2802x_BootVars.h</td>
<td>DSP2802x_Comp.h</td>
</tr>
<tr>
<td>DSP2802x_CpuTimers.h</td>
<td>DSP2802x_DevEmu.h</td>
<td>DSP2802x_Device.h</td>
</tr>
<tr>
<td>DSP2802x_ECap.h</td>
<td>DSP2802x_EPwm.h</td>
<td>DSP2802x_Gpio.h</td>
</tr>
<tr>
<td>DSP2802x_I2c.h</td>
<td>DSP2802x_NmiIntrupt.h</td>
<td>DSP2802x_PieCtrl.h</td>
</tr>
<tr>
<td>DSP2802x_PieVect.h</td>
<td>DSP2802x_Sci.h</td>
<td>DSP2802x_Spi.h</td>
</tr>
<tr>
<td>DSP2802x_SysCtrl.h</td>
<td>DSP2802x_SysCtrl.h</td>
<td></td>
</tr>
<tr>
<td>DSP2802x_XIntrupt.h</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **DSP2802x_Device.h**
  - Main include file
  - Will include all other .h files
  - Include this file (*directly or indirectly*) in each source file:
    ```
    #include "DSP2802x_Device.h"
    ```

Global Variable Definitions File

**DSP2802x_GlobalVariableDefs.c**

- Declares a global instantiation of the structure for each peripheral
- Each structure is placed in its own section using a DATA_SECTION pragma to allow linking to the correct memory (see next slide)

```
DSP2802x_GlobalVariableDefs.c
```

```c
#include "DSP2802x_Device.h"
...
#pragma DATA_SECTION(AdcRegs,"AdcRegsFile");
volatile struct ADC_REGS AdcRegs;
...
```

- Add this file to your CCS project:
  ```
  DSP2802x_GlobalVariableDefs.c
  ```
Peripheral Register Header Files

**Linker Command Files for the Structures**

**DSP2802x_nonBIOS.cmd**

```
#include "DSP2802x_Device.h"
...
#pragma DATA_SECTION(AdcRegs,"AdcRegsFile");
volatile struct ADC_REGS AdcRegs;
...
```

**AdcRegsFile: > ADC PAGE = 1**

- Links each structure to the address of the peripheral using the structures named section
- Add this file to your CCS project:
  **DSP2802x_nonBIOS.cmd**

**DSP2802x_Headers_nonBIOS.cmd**

```
MEMORY {
    PAGE1:
    ...
    ADC: origin=0x007100, length=0x000080
    ...
} SECTIONS {
    ...
    AdcRegsFile: > ADC PAGE = 1
    ...
}
```

**Peripheral Specific Examples**

- Example projects for each peripheral
- Helpful to get you started

- adc_soc
- adc_temp_sensor
- csiu_timer
- ecap_apwm
- ecap_capture_pwm
- epwm_blanking_window
- epwm_dcevent_trip
- epwm_dcevent_trip_comp
- epwm_dcband
- epwm_timer_interrups
- epwm_trig_zone
- epwm_up_eq
- epwm_updown_eq
- external_interrupt
- flash
- gpio_setup
- gpio_toggle
- hps
- hps_duty_sfo_v6
- hps_prd_up_sfo_v6
- hps_prd_down_sfo_v6
- hps_slider
- i2c_eeprom
- ibn_halikewake
- ilpm_idlewake
- ilpm_standbywake
- iso_echoback
- scia_loopback
- scia_loopback_interrups
- spi_loopback
- spi_loopback_interrups
- siw prioritized_interrups
- timedLed_blink
- watchdog
Peripheral Register Header Files

Summary

◆ Easier code development
◆ Easy to use
◆ Generates most efficient code
◆ Increases effectiveness of CCS watch window
◆ TI has already done all the work!

• Use the correct header file package for your device:

<table>
<thead>
<tr>
<th>Device</th>
<th>Literature Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2802x</td>
<td>SPRC832</td>
</tr>
<tr>
<td>F2803x</td>
<td>SPRC892</td>
</tr>
<tr>
<td>F2833x and F2823x</td>
<td>SPRC530</td>
</tr>
<tr>
<td>F280x and F2801x</td>
<td>SPRC191</td>
</tr>
<tr>
<td>F2804x</td>
<td>SPRC324</td>
</tr>
<tr>
<td>F281x</td>
<td>SPRC097</td>
</tr>
</tbody>
</table>

Go to http://www.ti.com and enter the literature number in the keyword search box.
**Reset, Interrupts and System Initialization**

**Reset**

**Reset Sources**

- POR – *Power-on Reset* generates a device reset during power-up conditions
- BOR – *Brown-out Reset* generates a device reset if the power supply drops below specification for the device

**Note:** Devices support an on-chip voltage regulator (VREG) to generate the core voltage.

**Reset – Bootloader**

- **Emulation Boot**
  - Boot determined by 2 RAM locations: EMU_KEY and EMU_BMODE

- **Stand-alone Boot**
  - Boot determined by 2 GPIO pins and 2 OTP locations: OTP_KEY and OTP_BMODE

TRST = JTAG Test Reset

EMU_KEY & EMU_BMODE located in PIE at 0x0D00 & 0x0D01, respectively

OTP_KEY & OTP_BMODE located in OTP at 0x3D78FE & 0x3D78FF, respectively
Emulation Boot Mode \((\text{TRST} = 1)\)

**Emulator Connected**

**Emulation Boot**

Boot determined by 2 RAM locations: 
EMU_KEY and EMU_BMODE

- EMU_KEY = 0x55AA ?
  - NO: Boot Mode
  - YES: Wait

<table>
<thead>
<tr>
<th>EMU_BMODE</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>Parallel I/O</td>
</tr>
<tr>
<td>0x0001</td>
<td>SCI</td>
</tr>
<tr>
<td>0x0003</td>
<td>GetMode</td>
</tr>
<tr>
<td>0x0004</td>
<td>SPI</td>
</tr>
<tr>
<td>0x0005</td>
<td>I2C</td>
</tr>
<tr>
<td>0x0006</td>
<td>OTP</td>
</tr>
<tr>
<td>0x000A</td>
<td>M0 SARAM</td>
</tr>
<tr>
<td>0x00BB</td>
<td>FLASH</td>
</tr>
<tr>
<td>other</td>
<td>Wait</td>
</tr>
</tbody>
</table>

If either EMU_KEY or EMU_BMODE are invalid, the "wait" boot mode is used. These values can then be modified using the debugger and a reset issued to restart the boot process.

**Stand-Alone Boot Mode \((\text{TRST} = 0)\)**

**Emulator Not Connected**

**Stand-alone Boot**

Boot determined by 2 GPIO pins and 2 OTP locations: OTP_KEY and OTP_BMODE

- OTP_KEY = 0x55AA ?
  - NO: Boot Mode
  - YES: FLASH

<table>
<thead>
<tr>
<th>OTP_BMODE</th>
<th>Boot Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0001</td>
<td>SCI</td>
</tr>
<tr>
<td>0x0004</td>
<td>SPI</td>
</tr>
<tr>
<td>0x0005</td>
<td>I2C</td>
</tr>
<tr>
<td>0x0006</td>
<td>OTP</td>
</tr>
<tr>
<td>other</td>
<td>FLASH</td>
</tr>
</tbody>
</table>

Note that the boot behavior for unprogrammed OTP is the "FLASH" boot mode.

**GPIO**

<table>
<thead>
<tr>
<th>GPIO 37</th>
<th>GPIO 34</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Boot Mode**

- Parallel I/O
- SCI
- I2C
- OTP
- FLASH
- Wait

Note that the boot behavior for unprogrammed OTP is the "FLASH" boot mode.
**Reset Code Flow - Summary**

[Diagram showing memory map and reset code flow]

**Interrupts**

**Interrupt Sources**

- **Internal Sources**
  - TINT2
  - TINT1
  - TINT0
  - PIE (Peripheral Interrupt Expansion)
  - ePWM, eCAP, ADC, SCI, SPI, I2C, WD

- **External Sources**
  - XINT1 – XINT3
  - TZx
  - XRS

**Execution Entry**
- Determined by Emulation Boot Mode or Stand-Alone Boot Mode

**Bootloading Routines**
- (SCI, SPI, I2C, Parallel I/O)
A valid signal on a specific interrupt line causes the latch to display a “1” in the appropriate bit.

If the individual and global switches are turned “on” the interrupt reaches the core.

**Core Interrupt Registers**

**Interrupt Flag Register (IFR)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>RTOSINT</th>
<th>DLOGINT</th>
<th>INT14</th>
<th>INT13</th>
<th>INT12</th>
<th>INT11</th>
<th>INT10</th>
<th>INT9</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>INT8</td>
<td>INT7</td>
<td>INT6</td>
<td>INT5</td>
<td>INT4</td>
<td>INT3</td>
<td>INT2</td>
<td>INT1</td>
</tr>
<tr>
<td>14</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Interrupt Enable Register (IER)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>RTOSINT</th>
<th>DLOGINT</th>
<th>INT14</th>
<th>INT13</th>
<th>INT12</th>
<th>INT11</th>
<th>INT10</th>
<th>INT9</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>INT8</td>
<td>INT7</td>
<td>INT6</td>
<td>INT5</td>
<td>INT4</td>
<td>INT3</td>
<td>INT2</td>
<td>INT1</td>
</tr>
<tr>
<td>14</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Interrupt Global Mask Bit (INTM)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>INTM</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Bit 0</td>
</tr>
</tbody>
</table>

---

```c
/* Interrupt Enable Register */
extern cregister volatile unsigned int IER;
IER |= 0x0008;  //enable INT4 in IER
IER &= 0xFFF7;  //disable INT4 in IER

.asm(" CLRC  INTM");  //enable global interrupts
.asm(" SETC  INTM");  //disable global interrupts
```
Peripheral Interrupt Expansion (PIE)

Peripheral Interrupt Expansion - PIE

F2802x PIE Interrupt Assignment Table

<table>
<thead>
<tr>
<th>INT</th>
<th>INTx.8</th>
<th>INTx.7</th>
<th>INTx.6</th>
<th>INTx.5</th>
<th>INTx.4</th>
<th>INTx.3</th>
<th>INTx.2</th>
<th>INTx.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT1</td>
<td>WAKEINT</td>
<td>TINT0</td>
<td>ADCINT9</td>
<td>XINT2</td>
<td>XINT1</td>
<td>ADCINT2</td>
<td>ADCINT1</td>
<td></td>
</tr>
<tr>
<td>INT2</td>
<td></td>
<td></td>
<td></td>
<td>EPWM4_TZINT</td>
<td>EPWM3_TZINT</td>
<td>EPWM2_TZINT</td>
<td>EPWM1_TZINT</td>
<td></td>
</tr>
<tr>
<td>INT3</td>
<td></td>
<td></td>
<td></td>
<td>EPWM4_INT</td>
<td>EPWM3_INT</td>
<td>EPWM2_INT</td>
<td>EPWM1_INT</td>
<td></td>
</tr>
<tr>
<td>INT4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ECAP1_INT</td>
</tr>
<tr>
<td>INT5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SPIRX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I2CINT2A</td>
<td>I2CINT1A</td>
<td></td>
</tr>
<tr>
<td>INT9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SCINTX</td>
<td>INTA</td>
<td></td>
</tr>
<tr>
<td>INT10</td>
<td>ADCINT8</td>
<td>ADCINT7</td>
<td>ADCINT6</td>
<td>ADCINT5</td>
<td>ADCINT4</td>
<td>ADCINT3</td>
<td>ADCINT2</td>
<td>ADCINT1</td>
</tr>
<tr>
<td>INT11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>XINT3</td>
</tr>
</tbody>
</table>
### PIE Registers

**PIEIFRx register**  
(x = 1 to 12)

<table>
<thead>
<tr>
<th>15-8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>INTx.8</td>
<td>INTx.7</td>
<td>INTx.6</td>
<td>INTx.5</td>
<td>INTx.4</td>
<td>INTx.3</td>
<td>INTx.2</td>
<td>INTx.1</td>
</tr>
</tbody>
</table>

**PIEIERx register**  
(x = 1 to 12)

<table>
<thead>
<tr>
<th>15-8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>INTx.8</td>
<td>INTx.7</td>
<td>INTx.6</td>
<td>INTx.5</td>
<td>INTx.4</td>
<td>INTx.3</td>
<td>INTx.2</td>
<td>INTx.1</td>
</tr>
</tbody>
</table>

**PIE Interrupt Acknowledge Register (PIEACK)**

<table>
<thead>
<tr>
<th>15-12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>PIEACKx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PIECTRL register**

<table>
<thead>
<tr>
<th>15-1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIEVECT</td>
<td>ENPIE</td>
</tr>
</tbody>
</table>

### Default Interrupt Vector Table at Reset

<table>
<thead>
<tr>
<th>Vector</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>00</td>
</tr>
<tr>
<td>INT1</td>
<td>02</td>
</tr>
<tr>
<td>INT2</td>
<td>04</td>
</tr>
<tr>
<td>INT3</td>
<td>06</td>
</tr>
<tr>
<td>INT4</td>
<td>08</td>
</tr>
<tr>
<td>INT5</td>
<td>0A</td>
</tr>
<tr>
<td>INT6</td>
<td>0C</td>
</tr>
<tr>
<td>INT7</td>
<td>0E</td>
</tr>
<tr>
<td>INT8</td>
<td>10</td>
</tr>
<tr>
<td>INT9</td>
<td>12</td>
</tr>
<tr>
<td>INT10</td>
<td>14</td>
</tr>
<tr>
<td>INT11</td>
<td>16</td>
</tr>
<tr>
<td>INT12</td>
<td>18</td>
</tr>
<tr>
<td>INT13</td>
<td>1A</td>
</tr>
<tr>
<td>INT14</td>
<td>1C</td>
</tr>
<tr>
<td>DATALOG</td>
<td>1E</td>
</tr>
<tr>
<td>RTOSINT</td>
<td>20</td>
</tr>
<tr>
<td>EMUINTR</td>
<td>22</td>
</tr>
<tr>
<td>NMI</td>
<td>24</td>
</tr>
<tr>
<td>ILLEGAL</td>
<td>26</td>
</tr>
<tr>
<td>USER 1-12</td>
<td>28-3E</td>
</tr>
</tbody>
</table>
Oscillator / PLL Clock Module

F2802x Oscillator / PLL Clock Module
(lab file: SysCtrl.c)

- Internal OSC 1 (10 MHz)
- Internal OSC 2 (10 MHz)
- XCLKIN
- XTAL
- X2
- EXTCLK
- OSCCLKSRC2
- OSC1CLK
- OSC2CLK
- SYSCLKOUT
- TMR2CLKSRCSEL
- WDCLKSRCSEL
- WDCLK
- Watchdog Module
- PLL
- VCOCLK
- OSCCLK
- C28x Core
- SYSCLKOUT
- CPU
- Timer 2
- SCI, SPI
- All other peripherals clocked by SYSCLKOUT

DIVSEL n
0x /4 *
10 /2
11 /1
* default

Note: /1 mode can only be used when PLL is bypassed

Diagrams:

- Oscillator / PLL Clock Module Diagram
- F2802x PLL and LOSPCP Diagram

Input Clock Fail Detect Circuitry
PLL will issue a "limp mode" clock (1-4 MHz) if input clock is removed after PLL has locked.
An internal device reset will also be issued (XRSn pin not driven).
Watchdog Timer Module

Watchdog Timer

- Resets the C28x if the CPU crashes
  - Watchdog counter runs independent of CPU
  - If counter overflows, a reset or interrupt is triggered (user selectable)
  - CPU must write correct data key sequence to reset the counter before overflow
- Watchdog must be serviced or disabled within 131,072 WDCLK cycles after reset
- This translates to 13.11 ms with a 10 MHz WDCLK

Watchdog Timer Module
(lab file: Watchdog.c)
GPIO

F2802x GPIO Grouping Overview
(lab file: Gpio.c)

GPIO Port A Mux1 Register (GPAMUX1) [GPIO 0 to 15]
GPIO Port A Mux2 Register (GPAMUX2) [GPIO 16 to 31]
GPIO Port B Mux1 Register (GPBMUX1) [GPIO 32 to 38]
GPIO Port B Mux2 Register (GPBMUX2) [GPIO 32 to 38]
ANALOG I/O Mux1 Register (AIOMUX1) [AIO 0 to 15]
ANALOG Port Direction Register (AIODIR) [AIO 0 to 15]

Input Qual
Input Qual
Input Qual

Internal Bus

F2802x GPIO Pin Block Diagram
(lab file: Gpio.c)

I/O DIR Bit
0 = Input
1 = Output

GPxDIR

GPxSET
GPxCLEAR
GPxTOGGLE

GPxDAT

I/O DAT Bit (R/W)

Out
In

Input Qualification (GPIO 0-38)

Peripheral 1
Peripheral 2
Peripheral 3

MUX Control Bits *
00 = GPIO
01 = Peripheral 1
10 = Peripheral 2
11 = Peripheral 3

GPxMUX1
GPxMUX2

GPxQSEL1
GPxQSEL2
GPxCCTRL

* See device datasheet for pin function selection matrices

••

01
00

Pin

Internal Pull-Up
0 = enable (default GPIO 12-38)
1 = disable (default GPIO 0-11)
F2802x GPIO Input Qualification

- Qualification available on ports A & B (GPIO 0 - 38) only
- Individually selectable per pin
  - no qualification (peripherals only)
  - sync to SYSCLKOUT only
  - qualify 3 samples
  - qualify 6 samples
- AIO pins are fixed as 'sync to SYSCLKOUT'

Lab 2: System Initialization

- LAB2 files have been provided
- LAB2 consists of two parts:
  Part 1
  - Test behavior of watchdog when disabled and enabled
  Part 2
  - Initialize peripheral interrupt expansion (PIE) vectors and use watchdog to generate an interrupt
- Modify, build, and test code using Code Composer Studio
Lab 2: System Initialization

Objective

The objective of this lab is to perform the processor system initialization. Additionally, the peripheral interrupt expansion (PIE) vectors will be initialized and tested. The system initialization for this lab will consist of the following:

- Setup the clock module – PLL, LOSPCP = /4, low-power modes to default values, enable all module clocks
- Disable the watchdog – clear WD flag, disable watchdog, WD prescale = 1
- Setup watchdog system control register – DO NOT clear WD OVERRIDE bit, WD generate a CPU reset
- Setup shared I/O pins – set all GPIO pins to GPIO function (e.g. a "00" setting for GPIO function, and a “01”, “10”, or “11” setting for peripheral function.)

The first part of the lab exercise will setup the system initialization and test the watchdog operation by having the watchdog cause a reset. In the second part of the lab exercise the PIE vectors will be tested by using the watchdog to generate an interrupt. This lab will make use of the DSP2802x C-code header files to simplify the programming of the device, as well as take care of the register definitions and addresses. Please review these files, and make use of them in the future, as needed.

Procedure

Open the Project

1. A project named Lab2 has been created for this lab. Open the project by clicking on Project ➔ Import Existing CCS/CCE Eclipse Project. The “Import” window will open then click Browse... next to the “Select root directory” box. Navigate to: C:\C28x\Labs\Lab2\Project and click OK. Then click Finish to import the project.

2. In the C/C++ Projects window, click the plus sign (+) to the left of Lab2 to view the project files. All Build Options have been configured for this lab. The files used in this lab are:

   CodeStartBranch.asm Lab_2_3.cmd
   DefaultIsr_2.c Main_2.c
   DelayUs.asm PieCtrl.c
   DSP2802x_GlobalVariableDefs.c PieVect.c
   DSP2802x_Headers_nonBIOS.cmd SysCtrl.c
   Gpio.c Watchdog.c
Modified Memory Configuration

3. Open and inspect the linker command file `Lab_2_3.cmd`. Notice that the user defined section “codestart” is being linked to a memory block named `BEGIN_M0`. The codestart section contains code that branches to the code entry point of the project. The bootloader must branch to the codestart section at the end of the boot process. Recall that the emulation boot mode "M0 SARAM" branches to address 0x000000 upon bootloader completion.

The linker command file (`Lab_2_3.cmd`) has a new memory block named `BEGIN_M0`: origin = 0x000000, length = 0x0002, in program memory. Additionally, the existing memory block `M0SARAM` in data memory has been modified to avoid overlaps with this new memory block.

System Initialization

4. Open and inspect `SysCtrl.c`. Notice that the PLL and module clocks have been enabled.

5. Open and inspect `Watchdog.c`. Notice that the watchdog control register (WDCR) is configured to disable the watchdog, and the system control and status register (SCSR) is configured to generate a reset.

6. Open and inspect `Gpio.c`. Notice that the shared I/O pins have been set to the GPIO function, except for GPIO0 which will be used in the next lab exercise. Close the inspected files.

Build and Load

7. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.

8. Click the “Debug” button (green bug). The “Debug Perspective” view should open, the program will load automatically, and you should now be at the start of `main()`.

9. After CCS loaded the program in the previous step, it set the program counter (PC) to point to `_c_int00`. It then ran through the C-environment initialization routine in the `rts2800_ml.lib` and stopped at the start of `main()`. CCS did not do a device reset, and as a result the bootloader was bypassed.

In the remaining parts of this lab exercise, the device will be undergoing a reset due to the watchdog timer. Therefore, we must configure the device by loading values into `EMU_KEY` and `EMU_BMODE` so the bootloader will jump to “M0 SARAM” at address 0x000000. Set the bootloader mode using the menu bar by clicking:

```
Scripts ➔ EMU Boot Mode Select ➔ EMU_BOOT_SARAM
```

If the device is power cycled between lab exercises, or within a lab exercise, be sure to re-configure the boot mode to `EMU_BOOT_SARAM`. 
Run the Code – Watchdog Reset

10. Place the cursor in the “main loop” section (on the `asm(" NOP")`; instruction line) and right click the mouse key and select Run To Line. This is the same as setting a breakpoint on the selected line, running to that breakpoint, and then removing the breakpoint.

11. Place the cursor on the first line of code in `main()` and set a breakpoint by right clicking the mouse key and select Toggle Breakpoint. Notice that line is highlighted with a blue dot indicating that the breakpoint has been set. Alternately, you can double-click in the line number field to the left of the code line to set the breakpoint. The breakpoint is set to prove that the watchdog is disabled. If the watchdog causes a reset, code execution will stop at this breakpoint.

12. Run your code for a few seconds by using the Run button on the toolbar, or using Target ➔ Run on the menu bar. After a few seconds halt your code by using the Halt button on the toolbar, or by using Target ➔ Halt. Where did your code stop? Are the results as expected? If things went as expected, your code should be in the “main loop”.

13. Switch to the “C/C++ Perspective” view by clicking the C/C++ icon in the upper right-hand corner. Modify the `InitWatchdog()` function to enable the watchdog (WDCR). In Watchdog.c change the WDCR register value to `0x00A8`. This will enable the watchdog to function and cause a reset. Save the file.

14. Click the “Build” button. Select Yes to “Reload the program automatically”. Switch back to the “Debug Perspective” view by clicking the Debug icon in the upper right-hand corner.

15. Like before, place the cursor in the “main loop” section (on the `asm(" NOP")`; instruction line) and right click the mouse key and select Run To Line.

16. Run your code. Where did your code stop? Are the results as expected? If things went as expected, your code should have stopped at the breakpoint. What happened is as follows. While the code was running, the watchdog timed out and reset the processor. The reset vector was then fetched and the ROM bootloader began execution. Since the device is in emulation boot mode (i.e. the emulator is connected) the bootloader read the EMU_KEY and EMU_BMODE values from the PIE RAM. These values were previously set for boot to M0 SARAM bootmode by CCS. Since these values did not change and are not affected by reset, the bootloader transferred execution to the beginning of our code at address 0x000000 in the M0SARAM, and execution continued until the breakpoint was hit in main().

Setup PIE Vector for Watchdog Interrupt

The first part of this lab exercise used the watchdog to generate a CPU reset. This was tested using a breakpoint set at the beginning of `main()`. Next, we are going to use the watchdog to generate an interrupt. This part will demonstrate the interrupt concepts learned in this module.
17. Switch to the “C/C++ Perspective” view by clicking the C/C++ icon in the upper right-hand corner. Notice that the following files are included in the project:

DefaultIsr_2.c
PieCtrl.c
PieVect.c

18. In Main_2.c, uncomment the code used to call the InitPieCtrl() function. There are no passed parameters or return values, so the call code is simply:

InitPieCtrl();

19. Using the “PIE Interrupt Assignment Table” shown in the slides find the location for the watchdog interrupt, “WAKEINT”. This is used in the next step.

PIE group #:__________  # within group:__________

20. In main() notice the code used to enable global interrupts (INTM bit), and in InitWatchdog() the code used to enable the “WAKEINT” interrupt in the PIE (using the PieCtrlRegs structure) and to enable core INT1 (IER register).

21. Modify the system control and status register (SCSR) to cause the watchdog to generate a WAKEINT rather than a reset. In Watchdog.c change the SCSR register value to 0x0002. Save the modified files.

22. Open and inspect DefaultIsr_2.c. This file contains interrupt service routines. The ISR for WAKEINT has been trapped by an emulation breakpoint contained in an inline assembly statement using “ESTOP0”. This gives the same results as placing a breakpoint in the ISR. We will run the lab exercise as before, except this time the watchdog will generate an interrupt. If the registers have been configured properly, the code will be trapped in the ISR.

23. Open and inspect PieCtrl.c. This file is used to initialize the PIE RAM and enable the PIE. The interrupt vector table located in PieVect.c is copied to the PIE RAM to setup the vectors for the interrupts. Close the modified and inspected files.

**Build and Load**

24. Click the “Build” button and select Yes to “Reload the program automatically”.

Switch to the “Debug Perspective” view by clicking the Debug icon in the upper right-hand corner.

**Run the Code – Watchdog Interrupt**

25. Place the cursor in the “main loop” section, right click the mouse key and select Run To Line.

26. Run your code. Where did your code stop? Are the results as expected? If things went as expected, your code should stop at the “ESTOP0” instruction in the WAKEINT ISR.
Terminate Debug Session and Close Project

27. Terminate the active debug session using the Terminate All button. This will close
the debugger and return CCS to the “C/C++ Perspective” view.

28. Next, close the project by right-clicking on Lab2 in the C/C++ Projects window
and select Close Project.

End of Exercise

Note: By default, the watchdog timer is enabled out of reset. Code in the file
CodeStartBranch.asm has been configured to disable the watchdog. This can be
important for large C code projects (ask your instructor if this has not already been
explained). During this lab exercise, the watchdog was actually re-enabled (or disabled
again) in the file Watchdog.c.
Control Peripherals

ADC Module

ADC Module Block Diagram

ADC full-scale input range is 0 to 3.3V

ADC full-scale input range is 0 to 3.3V

Example – ADC Triggering (1 of 2)

Sample $A_2 \to B_3 \to A_7$ when ePWM1 SOC$_B$ is generated and then generate ADCINT1$n$:

As above, but also sample $A_0 \to B_0 \to A_5$ continuously and generate ADCINT2$n$:
Example – ADC Triggering (2 of 2)

Sample all channels continuously and provide Ping-Pong interrupts to CPU/system:

- **Channel A0**: Sample 7 cycles → Result0
  - ADCINT2n
  - no interrupt

- **Channel A1**: Sample 7 cycles → Result1
  - ADCINT2n
  - no interrupt

- **Channel A2**: Sample 7 cycles → Result2
  - SOC0
  - no interrupt

- **Channel A3**: Sample 7 cycles → Result3
  - SOC2
  - no interrupt

- **Channel A4**: Sample 7 cycles → Result4
  - SOC4
  - no interrupt

- **Channel A5**: Sample 7 cycles → Result5
  - SOC6
  - no interrupt

- **Channel A6**: Sample 7 cycles → Result6
  - SOC8
  - no interrupt

- **Channel A7**: Sample 7 cycles → Result7
  - SOC10
  - no interrupt

- **Channel A8**: Sample 7 cycles → Result8
  - SOC12
  - no interrupt

- **Channel A9**: Sample 7 cycles → Result9
  - SOC14
  - no interrupt

- **Channel A10**: Sample 7 cycles → Result10
  - ADCINT1n
  - no interrupt

- **Channel A11**: Sample 7 cycles → Result11
  - no interrupt

- **Channel A12**: Sample 7 cycles → Result12
  - no interrupt

- **Channel A13**: Sample 7 cycles → Result13
  - no interrupt

- **Channel A14**: Sample 7 cycles → Result14
  - no interrupt

- **Channel A15**: Sample 7 cycles → Result15
  - no interrupt

---

Comparator

Comparator 3 available only on TMS320F2803x devices
ADC Control Registers (file: Adc.c)

- **ADCTRL1** (ADC Control Register 1)
  - module reset, ADC enable
  - busy/busy channel
  - reference select
  - Interrupt generation control
- **ADCSOCxCTL** (SOC0 to SOC15 Control Registers)
  - trigger source
  - channel
  - acquisition sampling window
- **ADCIINTSOCSELx** (Interrupt SOC Selection 1 and 2 Registers)
  - selects ADCINT1 / ADCINT2 trigger for SOCx
- **ADCSAMPLEMODE** (Sampling Mode Register)
  - sequential sampling / simultaneous sampling
- **INTSELxNy** (Interrupt x and y Selection Registers)
  - EOC0 – EOC15 source select for ADCINT1-9
- **ADCRESULTx** (ADC Result 0 to 15 Registers)

Note: refer to the reference guide for a complete listing of registers

Pulse Width Modulation

What is Pulse Width Modulation?

- **PWM** is a scheme to represent a signal as a sequence of pulses
  - fixed carrier frequency
  - fixed pulse amplitude
  - pulse width proportional to instantaneous signal amplitude
  - PWM energy $\approx$ original signal energy
Why use PWM with Power Switching Devices?

- Desired output currents or voltages are known
- Power switching devices are transistors
  - Difficult to control in proportional region
  - Easy to control in saturated region
- PWM is a digital signal ⇒ easy for DSP to output

DC Supply

Unknown Gate Signal

Desired signal to system

Gate Signal Known with PWM

PWM approx. of desired signal

ePWM

ePWM Module Signals and Connections
ePWM Block Diagram

16-Bit Time-Base Counter → Compare Logic → Action Qualifier → Dead Band

Period Register → PWM Chopper → Trip Zone

Digital Compare

ePWM Time-Base Sub-Module

16-Bit Time-Base Counter → Compare Logic → Action Qualifier → Dead Band

Period Register → PWM Chopper → Trip Zone

Digital Compare
ePWM Time-Base Count Modes

- **Count Up Mode**
- **Count Down Mode**
- **Count Up and Down Mode**

**Asymmetrical Waveform**

**Symmetrical Waveform**

---

**ePWM Phase Synchronization**

- **Phase φ=0°**
- **Phase φ=120°**
- **Phase φ=240°**

- **Ext. SyncIn (optional)**
- **SyncIn**
- **SyncOut**
- **EPWM1A**
- **EPWM1B**
- **EPWM2A**
- **EPWM2B**
- **EPWM3A**
- **EPWM3B**

- **φ=120°**
- **φ=240°**
ePWM Compare Sub-Module

Clock Prescaler

16-Bit Time-Base Counter

Compare Logic

Action Qualifier

Dead Band

Period Register

PWM Chopper

Trip Zone

Digital Compare

EPWMxSYNCI EPWMxSYNCO

TBCLK

SYSCLKOUT

ePWM Compare Event Waveforms

Count Up Mode

Asymmetrical Waveform

Count Down Mode

Asymmetrical Waveform

Count Up and Down Mode

Symmetrical Waveform

= compare events are fed to the Action Qualifier Sub-Module
**ePWM Action Qualifier Sub-Module**

- **Clock Prescaler**
- **16-Bit Time-Base Counter**
- **Compare Logic**
- **Period Register**
- **Compare Register**
- **Action Qualifier**
- **Dead Band**
- **PWM Chopper**
- **Trip Zone**
- **Digital Compare**

**ePWM Action Qualifier Actions**
for EPWMA and EPWMB

<table>
<thead>
<tr>
<th>S/W Force</th>
<th>Time-Base Counter equals:</th>
<th>EPWM Output Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Zero CMPA CMPB TBPRD</td>
<td></td>
</tr>
<tr>
<td>SW X</td>
<td>Z X CA X CB X P X</td>
<td>Do Nothing</td>
</tr>
<tr>
<td>SW ↓</td>
<td>Z ↓ CA ↓ CB ↓ P ↓</td>
<td>Clear Low</td>
</tr>
<tr>
<td>SW ↑</td>
<td>Z ↑ CA ↑ CB ↑ P ↑</td>
<td>Set High</td>
</tr>
<tr>
<td>SW T</td>
<td>Z T CA T CB T P T</td>
<td>Toggle</td>
</tr>
</tbody>
</table>
ePWM Count Up Asymmetric Waveform
with Independent Modulation on EPWMA / B

TBCTR
TBPRD

Z ↑ P X CB X CA ↓ Z ↑ P X CB X CA ↓ Z ↑ P X

EPWMA

Z ↑ P X CB ↓ CA X Z ↑ P X CB ↓ CA X Z ↑ P X

EPWMB

ePWM Count Up Asymmetric Waveform
with Independent Modulation on EPWMA

TBCTR
TBPRD

CA ↑ CB ↓ CA ↑ CB ↓ CA ↑ CB ↓

EPWMA

Z T Z T Z T

EPWMB
ePWM Count Up-Down Symmetric Waveform

with Independent Modulation on EPWMA / B

---

---
ePWM Dead-Band Sub-Module

Motivation for Dead-Band

- Transistor gates turn on faster than they shut off
- Short circuit if both gates are on at the same time!
ePWM PWM Chopper Sub-Module

- Clock Prescaler
- 16-Bit Time-Base Counter
- Compare Logic
- Action Qualifier
- Dead Band
- Period Register
- PWM Chopper
- Trip Zone
- Digital Compare

SYCLKOUT

- EPWMxSYNCI
- EPWMxSYNCO
- EPWMxA
- EPWMxB
- TZy
- TZ1-TZ3
- COMPxOUT

ePWM Chopper Waveform

- Allows a high frequency carrier signal to modulate the PWM waveform generated by the Action Qualifier and Dead-Band modules
- Used with pulse transformer-based gate drivers to control power switching elements
The Digital Compare sub-module compares signals external to the ePWM module to directly generate events which are then fed to the Event-Trigger, Trip-Zone, and Time-Base sub-modules.
Trip-Zone Features

- Trip-Zone has a fast, clock independent logic path to high-impedance the EPWMxA/B output pins
- Interrupt latency may not protect hardware when responding to over current conditions or short-circuits through ISR software
- Supports:
  1) one-shot trip for major short circuits or over current conditions
  2) cycle-by-cycle trip for current limiting operation
Hi-Resolution PWM (HRPWM)

- Significantly increases the resolution of conventionally derived digital PWM
- Uses 8-bit extensions to Compare registers (CMPxHR), Period register (TBPRDHR) and Phase register (TBPHSHR) for edge positioning control
- Typically used when PWM resolution falls below ~9-10 bits which occurs at frequencies greater than ~120 kHz (with system clock of 60 MHz)
- Not all ePWM outputs support HRPWM feature (see device datasheet)

**ePWM Control Registers** (file: EPwm.c)

- **TBCTL** (Time-Base Control)
  - counter mode (up, down, up & down, stop); clock prescale; period shadow load; phase enable/direction; sync select
- **CMPCTL** (Compare Control)
  - compare load mode; operating mode (shadow / immediate)
- **AQCTLA/B** (Action Qualifier Control Output A/B)
  - action on up/down CTR = CMPA/B, PRD, 0 (nothing/set/clear/toggle)
- **DBCTL** (Dead-Band Control)
  - in/out-mode (disable / delay PWMxA/B); polarity select
- **PCCTL** (PWM-Chopper Control)
  - enable / disable; chopper CLK freq. & duty cycle; 1-shot pulse width
- **DCTRIPSEL** (Digital Compare Trip Select)
  - Digital compare A/B high/low input source select
- **TZCTL** (Trip-Zone Control)
  - enable /disable; action (force high / low / high-Z /nothing)
- **ETSEL** (Event-Trigger Selection)
  - interrupt & SOCA/B enable / disable; interrupt & SOCA/B select

*Note: refer to the reference guide for a complete listing of registers*
**eCAP**

Capture Module (eCAP)

- The eCAP module timestamps transitions on a capture input pin

---

**eCAP Module Block Diagram – Capture Mode**

- 32-Bit Time-Stamp Counter
- SYSCLKOUT
- Event Logic
- CAP1POL
  - Polarity Select 1
- CAP2POL
  - Polarity Select 2
- CAP3POL
  - Polarity Select 3
- CAP4POL
  - Polarity Select 4
- PRESCALE
  - Event Prescale
- ECAPx pin
eCAP Module Block Diagram – APWM Mode

**eQEP**

**What is an Incremental Quadrature Encoder?**

A digital (angular) position sensor

- photo sensors spaced $\theta/4$ deg. apart
- slots spaced $\theta$ deg. apart
- light source (LED)
- shaft rotation

Incremental Optical Encoder

Quadrature Output from Photo Sensors

Note: eQEP available only on the TMS320F2803x devices
How is Position Determined from Quadrature Signals?

Position resolution is $\theta/4$ degrees

\[(A,B) = (00), (10), (01), (11)\]

Quadrature Decoder State Machine

Quadrature Decoder Connections

Ch. A

Quadrature Capture

QEP Watchdog

32-Bit Unit

Time-Base

QEPxS

EQEPxI

EQEPxB/XDIR

EQEPxA/XCLK

Position/Counter Compare

Quadrature Decoder

Ch. B

Quadrature Capture

QEP Watchdog

32-Bit Unit

Time-Base

QEPxS

EQEPxI

EQEPxB/XDIR

EQEPxA/XCLK

Position/Counter Compare

Quadrature Decoder

Index

Strobe

from homing sensor
Lab 3: Control Peripherals

Objective

The objective of this lab is to demonstrate and become familiar with the operation of the on-chip analog-to-digital converter and ePWM. ePWM1A will be setup to generate a 2 kHz, 25% duty cycle symmetric PWM waveform. The waveform will then be sampled with the on-chip analog-to-digital converter and displayed using the graphing feature of Code Composer Studio. The ADC has been setup to sample a single input channel at a 50 kHz sampling rate and store the conversion result in a buffer in the MCU memory. This buffer operates in a circular fashion, such that new conversion data continuously overwrites older results in the buffer.

Two ePWM modules have been configured for this lab exercise:

- **ePWM1A – PWM Generation**
  - Used to generate a 2 kHz, 25% duty cycle symmetric PWM waveform

- **ePWM2 – ADC Conversion Trigger**
  - Used as a timebase for triggering ADC samples (period match trigger SOCA)

The software in this exercise configures the ePWM modules and the ADC. It is entirely interrupt driven. The ADC end-of-conversion interrupt will be used to prompt the CPU to copy the results of the ADC conversion into a results buffer in memory. This buffer pointer will be managed in a circular fashion, such that new conversion results will continuously overwrite older conversion results in the buffer. The ADC interrupt service routine (ISR) will also toggle LED LD2 on the Piccolo™ controlSTICK as a visual indication that the ISR is running.
Notes

- ePWM1A is used to generate a 2 kHz PWM waveform
- Program performs conversion on ADC channel A0 (ADCINA0 pin)
- ADC conversion is set at a 50 kHz sampling rate
- ePWM2 is triggering the ADC on period match using SOCA trigger
- Data is continuously stored in a circular buffer
- Data is displayed using the graphing feature of Code Composer Studio
- ADC ISR will also toggle the LED LD2 as a visual indication that it is running

Procedure

Open the Project

1. A project named Lab3 has been created for this lab. Open the project by clicking on Project ➔ Import Existing CCS/CCE Eclipse Project. The “Import” window will open then click Browse... next to the “Select root directory” box. Navigate to: C:\C28x\Labs\Lab3\Project and click OK. Then click Finish to import the project.

2. In the C/C++ Projects window, click the plus sign (+) to the left of Lab3 to view the project files. All Build Options have been configured for this lab. The files used in this lab are:

   - Adc.c
   - CodeStartBranch.asm
   - DefaultIsr_3_4.c
   - DelayUs.asm
   - DSP2802x_GlobalVariableDefs.c
   - DSP2802x_Headers_nonBIOS.cmd
   - EPwm.c
   - Watchdog.c

   Gpio.c
   Lab_2_3.cmd
   Main_3.c
   PieCtrl.c
   PieVect.c
   SysCtrl.c

Setup of Shared I/O, General-Purpose Timer1 and Compare1

Note:  **DO NOT** make any changes to Gpio.c and EPwm.c - **ONLY INSPECT**

3. Open and inspect Gpio.c by double clicking on the filename in the project window. Notice that the shared I/O pin in GPIO0 has been set for the ePWM1A function. Next, open and inspect EPwm.c and see that the ePWM1 has been setup to implement the PWM waveform as described in the objective for this lab. Notice the values used in the following registers: TBCTL (set clock prescales to divide-by-1, no software force, sync and phase disabled), TBPRD, CMPA, CMPCTL (load on 0 or PRD), and AQCTLA (set on up count and clear on down count for output A). Software force, deadband, PWM chopper and trip action has been disabled. (Note that the last steps enable the timer count mode and enable the clock to the ePWM module). See the global variable names and values that have been set using #define in the beginning of the Lab.h file. Notice that ePWM2 has been initialized earlier in the code for the ADC. Close the inspected files.
Build and Load

4. Click the “Build” button and watch the tools run in the Console window. Check for errors in the Problems window.

5. Click the “Debug” button (green bug). The “Debug Perspective” view should open, the program load automatically, and you should now be at the start of `Main()`. If the device has been power cycled since the last lab exercise, be sure to configure the boot mode to `EMU_BOOT_SARAM` using the Scripts menu.

Run the Code – PWM Waveform

6. Open a memory window to view some of the contents of the ADC results buffer. To open a memory window click: View → Memory on the menu bar. The address label for the ADC results buffer is `AdcBuf` in the “Data” memory page.

Note: Exercise care when connecting any wires, as the power to the controlSTICK is on, and we do not want to damage the controlSTICK! Details of pin assignments can be found on the last page of this lab exercise.

7. Using a connector wire provided, connect the PWM1A (pin # 17) to ADCINA0 (pin # 3) on the controlSTICK.

8. Run your code for a few seconds by using the Run button on the toolbar, or using Target → Run on the menu bar. After a few seconds halt your code by using the Halt button on the toolbar, or by using Target → Halt. Verify that the ADC result buffer contains the updated values.

9. Open and setup a graph to plot a 50-point window of the ADC results buffer. Click: Tools → Graph → Single Time and set the following values:

<table>
<thead>
<tr>
<th>Acquisition Buffer Size</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Data Type</td>
<td>16-bit unsigned integer</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address</td>
<td><code>AdcBuf</code></td>
</tr>
<tr>
<td>Display Data Size</td>
<td>50</td>
</tr>
<tr>
<td>Time Display Unit</td>
<td>μs</td>
</tr>
</tbody>
</table>

Select OK to save the graph options.

10. The graphical display should show the generated 2 kHz, 25% duty cycle symmetric PWM waveform. The period of a 2 kHz signal is 500 μs. You can confirm this by measuring the period of the waveform using the “measurement marker mode” graph feature. Right-click on the graph and select Measurement Marker Mode. Move
the mouse to the first measurement position and left-click. Again, right-click on the
graph and select **Measurement Marker Mode**. Move the mouse to the second
measurement position and left-click. The graph will automatically calculate the
difference between the two values taken over a complete waveform period. When done,
clear the measurement points by right-clicking on the graph and select **Remove All Measurement Marks**.

### Frequency Domain Graphing Feature of Code Composer Studio

11. Code Composer Studio also has the ability to make frequency domain plots. It does this
by using the PC to perform a Fast Fourier Transform (FFT) of the DSP data. Let's make
a frequency domain plot of the contents in the ADC results buffer (i.e. the PWM
waveform).

Click: **Tools → Graph → FFT Magnitude** and set the following values:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition Buffer Size</td>
<td>50</td>
</tr>
<tr>
<td>DSP Data Type</td>
<td>16-bit unsigned integer</td>
</tr>
<tr>
<td>Sampling Rate (Hz)</td>
<td>50000</td>
</tr>
<tr>
<td>Start Address</td>
<td>AdcBuf</td>
</tr>
<tr>
<td>Data Plot Style</td>
<td>Bar</td>
</tr>
<tr>
<td>FFT Order</td>
<td>10</td>
</tr>
</tbody>
</table>

Select **OK** to save the graph options.

12. On the plot window, hold the mouse left-click key and move the marker line to observe
the frequencies of the different magnitude peaks. Do the peaks occur at the expected
frequencies?

### Using Real-time Emulation

Real-time emulation is a special emulation feature that allows the windows within Code
Composer Studio to be updated at up to a 10 Hz rate while the MCU is running. This not
only allows graphs and watch windows to update, but also allows the user to change values in
watch or memory windows, and have those changes affect the MCU behavior. This is very
useful when tuning control law parameters on-the-fly, for example.

13. The memory and single time graph windows displaying **AdcBuf** should still be open. The
connector wire between PWM1A (pin # 17) and ADCINA0 (pin # 3) should still be
connected. In real-time mode, we will have our window continuously refresh at the
default rate. To view the refresh rate click:

**Window → Preferences...**
and in the section on the left select the “CCS” category. Click the plus sign (+) to the left of “CCS” and select “Debug”. In the section on the right notice the default setting:

- “Continuous refresh interval (milliseconds)” = 1000

Click OK.

Note: Increasing the “Continuous refresh interval” causes all enabled continuous refresh windows to refresh at a faster rate. This can be problematic when a large number of windows are enabled, as bandwidth over the emulation link is limited. Updating too many windows can cause the refresh frequency to bog down. In this case you can just selectively enable continuous refresh for the individual windows of interest.

14. Next we need to enable the graph window for continuous refresh. In the upper right-hand corner of the graph window, left-click on the yellow icon with the arrows rotating in a circle over a pause sign. Note when you hover your mouse over the icon, it will show “Enable Continuous Refresh”. This will allow the graph to continuously refresh in real-time while the program is running.

15. Enable the memory window for continuous refresh using the same procedure as the previous step.

16. Run the code and watch the windows update in real-time mode. Click:

Scripts ➔ Realtime Emulation Control ➔ Run_Realtime_with_Reset

17. Carefully remove and replace the connector wire from ADCINA0 (pin # 3). Are the values updating as expected?

18. Fully halt the CPU in real-time mode. Click:

Scripts ➔ Realtime Emulation Control ➔ Full_Halt

**Terminate Debug Session and Close Project**

19. Terminate the active debug session using the Terminate All button. This will close the debugger and return CCS to the “C/C++ Perspective” view.

20. Next, close the project by right-clicking on Lab2 in the C/C++ Projects window and select Close Project.

**Optional Exercise**

You might want to experiment with this code by changing some of the values or just modify the code. Try generating another waveform of a different frequency and duty cycle. Also, try to generate complementary pair PWM outputs. Next, try to generate additional simultaneous waveforms by using other ePWM modules. Hint: don’t forget to setup the proper shared I/O pins, etc. (This optional exercise requires some further working knowledge of the ePWM. Additionally, it may require more time than is allocated for this lab. Therefore, you may want to try this after the class).

**End of Exercise**
### Lab Reference: Piccolo™ controlSTICK Header Pin Diagram

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ADC-A7</td>
<td>2</td>
<td>ADC-A2</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>COMP1 (+VE)</td>
<td></td>
<td></td>
<td>Vref-HI</td>
</tr>
<tr>
<td>4</td>
<td>3V3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ADC-A4</td>
<td>6</td>
<td>ADC-B1</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>COMP2 (+VE)</td>
<td></td>
<td></td>
<td>GPIO-07</td>
</tr>
<tr>
<td>8</td>
<td>TZ1</td>
<td>9</td>
<td>SCL</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>GPIO-12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>ADC-A1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>SDA</td>
<td>14</td>
<td>ADC-B7</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>GPIO-32</td>
<td></td>
<td></td>
<td>GPIO-05</td>
</tr>
<tr>
<td>16</td>
<td>5V0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>EPWM-1A</td>
<td>18</td>
<td>ADC-B4</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td>GPIO-00</td>
<td></td>
<td>COMP2 (-VE)</td>
<td>GPIO-04</td>
</tr>
<tr>
<td>20</td>
<td>SPISOMI</td>
<td></td>
<td></td>
<td>GPIO-17</td>
</tr>
<tr>
<td>21</td>
<td>EPWM-1B</td>
<td>22</td>
<td>ADC-B3</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>GPIO-01</td>
<td></td>
<td></td>
<td>GPIO-03</td>
</tr>
<tr>
<td>24</td>
<td>SPISIMO</td>
<td></td>
<td></td>
<td>GPIO-16</td>
</tr>
<tr>
<td>25</td>
<td>SPISTE</td>
<td>26</td>
<td>ADC-B2</td>
<td>27</td>
</tr>
<tr>
<td></td>
<td>GPIO-19</td>
<td></td>
<td>COMP1 (-VE)</td>
<td>GPIO-02</td>
</tr>
<tr>
<td>28</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>SPICLK</td>
<td>30</td>
<td>GPIO-34</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>GPIO-18</td>
<td></td>
<td>(LED)</td>
<td>(Filtered)</td>
</tr>
<tr>
<td>32</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Flash Programming Basics

- The DSP CPU itself performs the flash programming
- The CPU executes Flash utility code from RAM that reads the Flash data and writes it into the Flash
- We need to get the Flash utility code and the Flash data into RAM

**Sequence of steps for Flash programming:**

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Erase</td>
<td>- Set all bits to zero, then to one</td>
</tr>
<tr>
<td>2. Program</td>
<td>- Program selected bits with zero</td>
</tr>
<tr>
<td>3. Verify</td>
<td>- Verify flash contents</td>
</tr>
</tbody>
</table>

- Minimum Erase size is a sector (4Kw or 8Kw)
- Minimum Program size is a bit!
- Important not to lose power during erase step: If CSM passwords happen to be all zeros, the CSM will be permanently locked!
- Chance of this happening is quite small! (Erase step is performed sector by sector)
Programming Utilities and CCS Flash Programmer

Flash Programming Utilities

- **JTAG Emulator Based**
  - Code Composer Studio on-chip Flash programmer
  - BlackHawk Flash utilities (requires Blackhawk emulator)
  - Elprotronic FlashPro2000
  - Spectrum Digital SDFlash JTAG (requires SD emulator)
  - Signum System Flash utilities (requires Signum emulator)

- **SCI Serial Port Bootloader Based**
  - Code-Skin (http://www.code-skin.com)
  - Elprotronic FlashPro2000

- **Production Test/Programming Equipment Based**
  - BP Micro programmer
  - Data I/O programmer

- **Build your own custom utility**
  - Can use any of the ROM bootloader methods
  - Can embed flash programming into your application
  - Flash API algorithms provided by TI

* TI web has links to all utilities (http://www.ti.com/c2000)

CCS On-Chip Flash Programmer

- On-Chip Flash programmer is integrated into the CCS debugger
Code Security Module and Password

**Code Security Module (CSM)**

- Access to the following on-chip memory is restricted:
  - Flash Registers
  - L0 SARAM (4Kw)
  - L0 SARAM (1Kw)
  - User OTP (1Kw)
  - ADC / OSC cal. data
  - FLASH (32Kw)
  - PASSWORDS (8w)
  - L0 SARAM (1Kw)

- Data reads and writes from restricted memory are only allowed for code running from restricted memory
- All other data read/write accesses are blocked:
  - JTAG emulator/debugger, ROM bootloader, code running in external memory or unrestricted internal memory

**CSM Password**

- 128-bit user defined password is stored in Flash
- 128-bit KEY registers are used to lock and unlock the device
  - Mapped in memory space 0x00 0AE0 – 0x00 0AE7
  - Registers “EALLOW” protected
CSM Password Match Flow

Start

Flash device secure after reset or runtime

Do dummy reads of PWL 0x3F 7FF8 – 0x3F 7FFF

Is PWL = all 0s?

Yes

Device permanently locked

No

Is PWL = all Fs?

Yes

Write password to KEY registers 0x00 0AE0 – 0x00 0AE7 (EALLOW) protected

Correct password?

Yes

Device unlocked User can access on-chip secure memory

No

No

No
Lab 4: Programming the Flash

Objective

The objective of this lab is to program and execute code from the on-chip flash memory. The TMS320F28027 device has been designed for standalone operation in an embedded system. Using the on-chip flash eliminates the need for external non-volatile memory or a host processor from which to bootload. In this lab, the steps required to properly configure the software for execution from internal flash memory will be covered.

Objective:
- Program system into Flash Memory
- Learn use of CCS Flash Programmer
- DO NOT PROGRAM PASSWORDS

Procedure

Open the Project

1. A project named Lab4 has been created for this lab. Open the project by clicking on Project ➔ Import Existing CCS/CCE Eclipse Project. The “Import” window will open then click Browse... next to the “Select root directory” box. Navigate to: C:\C28x\Labs\Lab4\Project and click OK. Then click Finish to import the project.

2. In the C/C++ Projects window, click the plus sign (+) to the left of Lab4 to view the project files. All Build Options have been configured for this lab. The files used in this lab are:
Link Initialized Sections to Flash

Initialized sections, such as code and constants, must contain valid values at device power-up. Stand-alone operation of an F28077 embedded system means that no emulator is available to initialize the device RAM. Therefore, all initialized sections must be linked to the on-chip flash memory.

Each initialized section actually has two addresses associated with it. First, it has a LOAD address which is the address to which it gets loaded at load time (or at flash programming time). Second, it has a RUN address which is the address from which the section is accessed at runtime. The linker assigns both addresses to the section. Most initialized sections can have the same LOAD and RUN address in the flash. However, some initialized sections need to be loaded to flash, but then run from RAM. This is required, for example, if the contents of the section needs to be modified at runtime by the code.

3. Open and inspect the linker command file Lab_4.cmd. Notice that a memory block named FLASH_ABCD has been created at origin = 0x3F0000, length = 0x007F80 on Page 0. This flash memory block length has been selected to avoid conflicts with other required flash memory spaces. See the reference slide at the end of this lab exercise for further details showing the address origins and lengths of the various memory blocks used.

4. In Lab_4.cmd the following compiler sections have been linked to on-chip flash memory block FLASH_ABCD:

   Compiler Sections:

   | .text | .cinit | .const | .econst | .pinit | .switch |

Copying Interrupt Vectors from Flash to RAM

The interrupt vectors must be located in on-chip flash memory and at power-up needs to be copied to the PIE RAM as part of the device initialization procedure. The code that performs this copy is located in InitPieCtrl(). The C-compiler runtime support library contains a memory copy function called memcpy() which will be used to perform the copy.

5. Open and inspect InitPieCtrl() in PieCtrl.c. Notice the memcpy() function used to initialize (copy) the PIE vectors. At the end of the file a structure is used to enable the PIE.
Initializing the Flash Control Registers

The initialization code for the flash control registers cannot execute from the flash memory (since it is changing the flash configuration!). Therefore, the initialization function for the flash control registers must be copied from flash (load address) to RAM (run address) at runtime. The memory copy function `memcpy()` will again be used to perform the copy. The initialization code for the flash control registers `InitFlash()` is located in the `Flash.c` file.

6. Open and inspect `Flash.c`. The C compiler CODE_SECTION pragma is used to place the `InitFlash()` function into a linkable section named “secureRamFuncs”.

7. The “secureRamFuncs” section will be linked using the user linker command file `Lab_4.cmd`. Open and inspect `Lab_4.cmd`. The “secureRamFuncs” will load to flash (load address) but will run from `L0SARAM` (run address). Also notice that the linker has been asked to generate symbols for the load start, load end, and run start addresses.

   While not a requirement from a MCU hardware or development tools perspective (since the C28x MCU has a unified memory architecture), historical convention is to link code to program memory space and data to data memory space. Therefore, notice that for the `L0SARAM` memory we are linking “secureRamFuncs” to, we are specifying “PAGE = 0” (which is program memory).

8. Open and inspect `Main_4.c`. Notice that the memory copy function `memcpy()` is being used to copy the section “secureRamFuncs”, which contains the initialization function for the flash control registers.

9. The following line of code in `main()` is used call the `InitFlash()` function. Since there are no passed parameters or return values the code is just:

   ```c
   InitFlash();
   ```

   at the desired spot in `main()`.

Code Security Module and Passwords

The CSM module provides protection against unwanted copying (i.e. pirating!) of your code from flash, OTP memory, and the L0SARAM block. The CSM uses a 128-bit password made up of 8 individual 16-bit words. They are located in flash at addresses 0x3F7FF8 to 0x3F7FFF. During this lab, dummy passwords of 0xFFFF will be used – therefore only dummy reads of the password locations are needed to unsecure the CSM. **DO NOT PROGRAM ANY REAL PASSWORDS INTO THE DEVICE.** After development, real passwords are typically placed in the password locations to protect your code. We will not be using real passwords in the workshop.

The CSM module also requires programming values of 0x0000 into flash addresses 0x3F7F80 through 0x3F7FF5 in order to properly secure the CSM. Both tasks will be accomplished using a simple assembly language file `Passwords.asm`. 
10. Open and inspect `Passwords.asm`. This file specifies the desired password values *(DO NOT CHANGE THE VALUES FROM 0xFFFF)* and places them in an initialized section named “passwords”. It also creates an initialized section named “csm_rsvd” which contains all 0x0000 values for locations 0x3F7F80 to 0x3F7FF5 (length of 0x76).

11. Open `Lab_4.cmd` and notice that the initialized sections for “passwords” and “csm_rsvd” are linked to memories named PASSWORDS and CSM_RSVD, respectively.

**Executing from Flash after Reset**

The F28027 device contains a ROM bootloader that will transfer code execution to the flash after reset. When the boot mode selection is set for “Jump to Flash” mode, the bootloader will branch to the instruction located at address 0x3F7FF6 in the flash. An instruction that branches to the beginning of your program needs to be placed at this address. Note that the CSM passwords begin at address 0x3F7FF8. There are exactly two words available to hold this branch instruction, and not coincidentally, a long branch instruction “LB” in assembly code occupies exactly two words. Generally, the branch instruction will branch to the start of the C-environment initialization routine located in the C-compiler runtime support library. The entry symbol for this routine is `_c_int00`. Recall that C code cannot be executed until this setup routine is run. Therefore, assembly code must be used for the branch. We are using the assembly code file named `CodeStartBranch.asm`.

12. Open and inspect `CodeStartBranch.asm`. This file creates an initialized section named “codestart” that contains a long branch to the C-environment setup routine. This section has been linked to a block of memory named BEGIN_FLASH.

13. In the earlier lab exercises, the section “codestart” was directed to the memory named BEGIN_M0. Open and inspect `Lab_4.cmd` and notice that the section “codestart” will now be directed to BEGIN_FLASH. Close the inspected files.

On power up the reset vector will be fetched and the ROM bootloader will begin execution. If the emulator is connected, the device will be in emulator boot mode and will use the EMU_KEY and EMU_BMODE values in the PIE RAM to determine the bootmode. This mode was utilized in an earlier lab. In this lab, we will be disconnecting the emulator and running in stand-alone boot mode (but do not disconnect the emulator yet!). The bootloader will read the OTP_KEY and OTP_BMODE values from their locations in the OTP. The behavior when these values have not been programmed (i.e., both 0xFFFF) or have been set to invalid values is boot to flash bootmode.

**Build – Lab.out**

14. Click the “Build” button to generate the `Lab.out` file to be used with the CCS Flash Programmer. Check for errors in the Problems window.

**CCS Flash Plug-in**

In CCS (version 4.x) the on-chip flash programmer is integrated into the debugger. When the program is loaded CCS will automatically determine which sections reside in flash memory based
on the linker command file. CCS will then program these sections into the on-chip flash memory. Additionally, in order to effectively debug with CCS, the symbolic debug information (e.g., symbol and label addresses, source file links, etc.) will automatically load so that CCS knows where everything is in your code.

Clicking the “Debug” button in the C/C++ Perspective will automatically launch the debugger, connect to the target, and program the flash memory in a single step.

15. Program the flash memory by clicking the “Debug” button (green bug). (If needed, when the “Progress Information” box opens select “Details >>” in order to watch the programming operation and status). After successfully programming the flash memory the “Progress Information” box will close.

16. Flash programming options are configured with the “On-Chip Flash” control panel. Open the control panel by clicking:

Tools → On-Chip Flash

Scroll the control panel and notice the various options that can be selected. You will see that specific actions such as “Erase Flash” can be performed.

The CCS on-chip flash programmer was automatically configured to use the Piccolo™ 10 MHz internal oscillator as the device clock during programming. Notice the “Clock Configuration” settings has the OSCCLK set to 10 MHz, the DIVSEL set to /2, and the PLLCR value set to 12. Recall that the PLL is divided by two, which gives a SYSCLKOUT of 60 MHz.

The flash programmer should be set for “Erase, Program, Verify” and all boxes in the “Erase Sector Selection” should be checked. We want to erase all the flash sectors.

We will not be using the on-chip flash programmer to program the “Code Security Password”. *Do not modify the Code Security Password fields.* They should remain as all 0xFFFF.

17. Close the “On-Chip Flash” control panel by clicking the X on the tab.

**Running the Code – Using CCS**

18. Reset the CPU using the “Reset CPU” button or click:

Target → Reset → Reset CPU

The program counter should now be at address 0x3FF7BB in the “Disassembly” window, which is the start of the bootloader in the Boot ROM.

19. Under **Scripts** on the menu bar click:

EMU Boot Mode Select → EMU_BOOT_FLASH.

This has the debugger load values into EMU_KEY and EMU_BMODE so that the bootloader will jump to "FLASH" at address 0x3F7FF6.
20. Single-Step by using the <F5> key (or you can use the Step Into button on the horizontal toolbar) through the bootloader code until you arrive at the beginning of the codestart section in the `CodeStartBranch.asm` file. (Be patient, it will take about 125 single-steps). Notice that we have placed some code in `CodeStartBranch.asm` to give an option to first disable the watchdog, if selected.

21. Step a few more times until you reach the start of the C-compiler initialization routine at the symbol `_c_int00`.

22. Now do Target → Go Main. The code should stop at the beginning of your main() routine. If you got to that point succesfully, it confirms that the flash has been programmed properly, that the bootloader is properly configured for jump to flash mode, and that the codestart section has been linked to the proper address.

23. You can now RUN the CPU, and you should observe the LED on the controlSTICK blinking. Try resetting the CPU, select the `EMU_BOOT_FLASH` boot mode, and then hitting RUN (without doing all the stepping and the Go Main procedure). The LED should be blinking again.

24. HALT the CPU.

**Terminate Debug Session and Close Project**

25. Terminate the active debug session using the Terminate All button. This will close the debugger and return CCS to the “C/C++ Perspective” view.

26. Next, close the project by right-clicking on Lab4 in the C/C++ Projects window and select Close Project.

**Running the Code – Stand-alone Operation (No Emulator)**

27. Close Code Composer Studio.

28. Disconnect the controlSTICK from the computer USB port.

29. Re-connect the controlSTICK to the computer USB port.

30. The LED should be blinking, showing that the code is now running from flash memory.

**End of Exercise**
Lab 4 Reference: Programming the Flash

Flash Memory Section Blocks

```
<table>
<thead>
<tr>
<th>Block</th>
<th>Origin</th>
<th>Length</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEGIN_FLASH</td>
<td>0x3F 0000</td>
<td>0x2</td>
<td>0</td>
</tr>
<tr>
<td>CSM_RSVD</td>
<td>0x3F 7FF6</td>
<td>0x76</td>
<td>0</td>
</tr>
<tr>
<td>PASSWORDS</td>
<td>0x3F 7FF8</td>
<td>0x8</td>
<td>0</td>
</tr>
<tr>
<td>FLASH</td>
<td></td>
<td>0x7E0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

Startup Sequence from Flash Memory

```
0x3F 0000
0x3F 7FF6
0x3F E000
0x3F FFC0

FLASH (32Kw)

Boot ROM (8Kw)

Passwords (8w)

Boot Code
0x3F F7BB
{SCAN GPIO}

BROM vector (32w)
0x3F F7BB

LAB

"rts2800_ml.lib"

"user" code sections
main()
{
    ......
    ......
}
```

Lab_4.cmd

```
SECTIONS
{
    codestart  : BEGIN_FLASH, PAGE = 0
    passwords   : PASSWORDS, PAGE = 0
    csm_rsvd    : CSM_RSVD, PAGE = 0
}
```
The Next Step…

Training

F28x Multi-day Training Course

TMS320F2803x Workshop Outline
- Architectural Overview
- Programming Development Environment
- Peripheral Register Header Files
- Reset and Interrupts
- System Initialization
- Analog-to-Digital Converter
- Control Peripherals
- Numerical Concepts and IQmath
- Control Law Accelerator (CLA)
- System Design
- Communications
- DSP/BIOS
- Support Resources

In-depth hands-on TMS320F28035 Design and Peripheral Training

controlSUITE

controlSUITE™
Development Tools

**C2000 Experimenter’s Kits**
F28027, F28035, F2808, F28335

- Experimenter Kits include
  - F28027, F28035, F2808 or F28335 controlCARD
  - USB docking station
  - C2000 Applications Software CD with example code and full hardware details
  - Code Composer Studio v3.3 with code size limit of 32KB

- Docking station features
  - Access to controlCARD signals
  - Breadboard areas
  - Onboard USB JTAG Emulation
    - JTAG emulator not required

- Available through TI authorized distributors and the TI eStore

**C2834x Experimenter’s Kits**
C28343, C28346

- Experimenter Kits include
  - C2834x controlCARD
  - Docking station
  - C2000 Applications Software CD with example code and full hardware details
  - Code Composer Studio v3.3 with code size limit of 32KB
  - 5V power supply

- Docking station features
  - Access to controlCARD signals
  - Breadboard areas
  - JTAG emulator required – sold separately

- Available through TI authorized distributors and the TI eStore
**F28335 Peripheral Explorer Kit**

- **Experimenter Kit includes**
  - F28335 controlCARD
  - Peripheral Explorer baseboard
  - C2000 Applications Software CD with example code and full hardware details
  - Code Composer Studio v3.3 with code size limit of 32KB
  - 5V DC power supply

- **Peripheral Explorer features**
  - ADC input variable resistors
  - GPIO hex encoder & push buttons
  - eCAP infrared sensor
  - GPIO LEDs, I2C & CAN connection
  - Analog I/O (AIC+McBSP)

- JTAG emulator required – sold separately

- Available through TI authorized distributors and the TI eStore

**C2000 controlCARD Application Kits**

- **Kits includes**
  - controlCARD and application specific baseboard
  - Full version of Code Composer Studio v3.3 with 32KB code size limit

- **Software download includes**
  - Complete schematics, BOM, gerber files, and source code for board and all software
  - Quickstart demonstration GUI for quick and easy access to all board features
  - Fully documented software specific to each kit and application

- See www.ti.com/c2000 for more details

- Available through TI authorized distributors and the TI eStore
The Next Step…

C2000 Signal Processing Libraries

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Available from TI Website ⇒ http://www.ti.com/c2000

C2000 Workshop Download Wiki

C2000 Workshop Download Wiki

Hands-On Training for TI Embedded Processors

The Hands-On Training Program conducts hands-on training for TI embedded processors at various worldwide locations. You can find complete course descriptions, locations, dates, and enrollment information here.

On the TI training site, you can find specific workshop locations/cities using the left hand navigation links. Select "By Type" and then select either "1-Day Workshops" or "Multi-Day Workshops" to get a complete list of training available. Click on the ‘Register Now’ button, or one of the individual ‘Register’ buttons to enroll in a workshop.

If you’d like to review specific workshop materials on your own, you can download the files using the links below.

C2000™ 32-bit Real-time MCU Training

C2000™ Piccolo™ One-Day Workshop

C2000™ Piccolo™ Multi-Day Workshop agenda, locations, and schedule

Online materials and links

C2000™ Piccolo™ Multi-Day Workshop

C2000™ Piccolo™ Multi-Day Workshop agenda, locations, and schedule

Online materials and links

C2000™ Delfino™ Multi-Day Workshop

TMS320C28x™ MCU Workshop agenda, locations, and schedule

Online materials and links

C2000™ Archival Workshops

The archived workshops are for F2807, F2802, and F2808 one-day and multi-day workshops. The F28336 xC28 one-day workshop is also found here.


C2000 Piccolo 1-Day Workshop
Development Support

For More Information . . .

Internet
Website: http://www.ti.com

FAQ: http://www-k.ext.ti.com/sc/technical_support/knowledgebase.htm
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