

# **DSP/BIOS VPORT Device Driver**

**Release Version: 1.10.03**

## **Release Notes**

**April 16, 2009**

This is a release/code drop of VPORT **DSP/BIOS** Device Driver for applications based on DSP family. The product has been built and tested over TI's DM648 EVM development boards.

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## **1 General information**

The VPORT device driver included in this release package supports h/w capabilities of **DSP** video port peripheral device.

The driver is compliant with DSP/BIOS IOM device driver model. The driver supports multiple video ports handling simultaneously.

### **1.1 Sample Application**

The sample **DSP/ BIOS** application <sample\_apps> is a representative test program. Initialization of VPORT driver is done by calling initialization function from BIOS.

Refer DSP/BIOS VPORT User Guide (*BIOS\_VPORT\_Driver\_UserGuide.pdf*) for details of the sample applications provided with this package.

## **2 New In This Release**

- The pragma definitions, macro definitions and compiler switches used are documented in the user guide .

## **3 System Requirements**

Details about the tools and the BIOS version that the driver is compatible with can be found in the system Release Notes.

## 4 Installation and Usage

- ❖ Install BIOS and XDC package as per instructions provided along with the package. Kindly refer PSP top level release notes for details - *PSP\_Release\_Notes.pdf*.

- ❖ **Build procedure and hardware setup for DM648 Video Sample Application**

Refer DSP/BIOS VPORT User Guide (*BIOS\_VPORT\_Driver\_UserGuide.pdf*) for the build procedure and hardware setup for the sample applications provided with this package.

- ❖ **Changes done in Sample Applications from Previous Release**

- Configuration macro (*CFG\_ENABLE\_HDCAPTURE\_WORKAROUND*) is provided in *psp\_bios\_vport\_hd\_loopback.c* file to enable or disable HD capture software workaround for proper HD capture operation in production EVM.

Define this macro to 1/0 to enable or disable software workaround for 1080i and 720p capture in production EVM.

For proper 1080i capture, TVP7000 HSYNC polarity is inverted (active low) and hence a horizontal shift is required in the field1 and field2 HSTART.

For 720p capture, DM648 VPORT detects the progressive input from TVP7000 as interlaced video. Hence VPORT driver is configured to capture both fields so that two 720p frames are captured per FVID call. These changes are illustrated in *psp\_bios\_vport\_hd\_loopback.c* file.

*CAP\_PARAMS\_CHAN\_720P\_60HZ\_DEFAULT\_FIX*,  
*CAP\_PARAMS\_CHAN\_1080I\_60HZ\_DEFAULT\_FIX* and  
*CAP\_PARAMS\_CHAN\_1080I\_50HZ\_DEFAULT\_FIX* macro are provided in *psp\_bios\_vport\_capParams.h* file. These macros contains the modified VPORT capture driver setting for proper HD capture operation in production EVM.

**Note:**

1. For proper HD capture "*CFG\_ENABLE\_HDCAPTURE\_WORKAROUND*" in files *psp\_bios\_vport\_hd\_loopback.c* and *\_tvp7000.c* (part of EDC driver) should be set the same and the EDC driver should be recompiled after the change. By default both these macros are set as 1. So no recompilation is required.
2. Before running HD loopback sample application make sure that a proper HD input is given to TVP7000 decoder. This is because by default TVP7000 doesn't generate blank data/clocks if there is no input given to it. Hence dequeue call to VPORT driver will hang because of no valid data coming to VPORT. For the same reason the HD video input should not be removed while HD capture is going on.

So always connect a valid input to TVP7000 before performing HD capture operation. And don't unplug the HD video input during testing.

### ❖ **Other Changes from Previous Release**

- Configuration macro (*CFG\_ENABLE\_THS7353*) is provided in TVP7000 EDC driver (*tv7000.c* file) to enable or disable THS7353 HD filter configuration.

In production EVM THS7353 HD filter is removed. Hence this option is provided to facilitate the use of TVP7000 driver both in pre-production EVMs and production EVMs. By default this macro is disabled – library is built for production EVM. If the EDC driver has to be used for HD capture operation in pre-production EVMs, then this macro should be set to 1 and the EDC library should be recompiled.

### ❖ **Recommended Cache Operation in Application**

In a simple loopback scenario, the application doesn't have to do any cache operations to ensure cache coherency if buffers are exchanged between drivers. But when the application access the video buffers through CPU, say to run an algorithm or to copy capture buffer to display buffer using CPU, then the below cache operations are recommended for proper operation.

#### ➤ **Capture driver**

Before providing a buffer to capture driver, the entire buffer should be invalidated. Below code snippet illustrate this.

```
/* Invalidate the buffer before giving to capture driver */  
BCACHE_inv((Uint8 *)frame->frame.iFrm.y1, FRAME_SIZE, TRUE);  
  
/* Give the old capture frame buffer back to driver and get the  
recently captured frame buffer */  
status = FVID_exchange(chanHandle, &frame);
```

#### ➤ **Display driver**

Before providing a buffer to display driver, the entire buffer should be flushed and invalidated. Below code snippet illustrate this.

```
/* Flush and invalidate the processed buffer so that the EDMA reads  
the processed data */  
BCACHE_wbInv((Uint8 *) frame->frame.iFrm.y1, FRAME_SIZE, TRUE);  
  
/* Give the captured frame buffer to display driver and get a  
free frame buffer for next capture */  
status = FVID_exchange(chanHandle, &frame);
```

## 5 Un-installation

Un-install the Driver package as per instructions provided with the package.

## 6 Adding instance of the device driver

To have VPORT device driver included in the application, it is required to add the TCI file for each of the video port instances. i.e. "dm648\_vport0.tci", "dm648\_vport1.tci", "dm648\_vport2.tci", "dm648\_vport3.tci" and "dm648\_vport4.tci" in the TCF file of the application. These files are present in the directory  
 "<root>\packages\ti\sdo\pspdrivers\system\dm648\bios\evmDM648\video\sample"

## 7 Fixed In This Release

- None

## 8 Known Issues/Limitations

<b>1.</b>	In production EVM, very mild horizontal fluctuations is seen in the image for VESA display. These horizontal fluctuations are more prominent for higher VESA resolution and refresh rates.
<b>Workaround</b>	
None	
<b>2.</b>	In production EVM, very mild fluctuations is seen in captured image for 1080i and 720p resolutions especially in vertical image boundaries. These fluctuations are not seen in a single frame – visible only in continuous frame capture.
<b>Workaround</b>	
None	

<b>3.</b>	Intermittent Jerk observed in SAA7105 display
Intermittent jerk observed in SAA7105 display. This is more prominently seen in Hitachi TV (32LD9800TA) than Sony TV. Suspected to be clock issues in the EVM.	
<b>Workaround</b>	
None	

<b>4.</b>	Black wave like display (very faint) seen in light background video in SAA7105 SD display
Black wave like display (very faint) seen in light background video in SAA7105 SD display. This artifact will move continuously from bottom to top at regular interval. This can be clearly seen in bright background. Suspected to be clock issues in the EVM.	
<b>Workaround</b>	
None	

<b>5.</b>	Grainy display observed in captured image
Due to the this issue the following artifacts are observed	
<ol style="list-style-type: none"> <li>1. Grainy display observed in portion of image having sharp edges in captured image</li> <li>2. Due to this issue lot of flickers are observed in SMPTE RP 133 test pattern. This effect is more prominent in the text. The alphabets in the pattern are closely placed and the noise in one alphabet is overlapping to the next alphabet and hence the text in this pattern is not clearly readable.</li> <li>3. Flickering is also observed with the patterns. This is clearly visible with patterns 6, 7 of title 12 (chapter display patterns) of Digital Video Essential DVD. Also dotted line like effect is seen at the sharp edges.</li> </ol>	
With further analysis it is found that this issue is due to TVP5154 capture using composite cable. If S-Video cable is used, the captured image is clear without these artifacts. For this setup, TVP5154 has to be configured for S-Video input and Y-luminance signal of S-Video should be connected to DM648 EVM using S-Video to Y/C splitter cable, Chrominance signal is not connected and is grounded in DM648 EVM.	
<b>Workaround</b>	
None	

<b>6.</b>	One of the TVP5154 decoder fails to power up sometimes.
<p>Due to this <i>FVID_create</i> returns error. This issue is very rare and if it occurs the problem persist until the EVM is reset. According to TVP5154 datasheet, a value of 0x54 should be read from register 0x81 from each of the four decoder of TVP5154. When this error occurs, 0x00 is read and the TVP5154 returns error.</p> <p><b>Workaround</b></p> <p>Power cycle the EVM and re-run the application</p>	

<b>7.</b>	Slow frame rate observed in SD/HD compositor, HD loopback, VESA color bar and RAW capture loopback sample application if run in DEBUG mode. This is because of unoptimized frame copy, 8 byte swap functions and no optimization compile option
<p>Due to slow frame rates in debug mode, chroma artifacts, as explained in Issue 10, is more prominent.</p> <p>For HD capture sample application, due to software workaround, memcopy of the entire frame is done along with the byte swap functions. Due to this the frames rates are lower in release mode as well.</p> <p><b>Workaround</b></p> <p>HD capture application only:</p> <p>If byteswap function is disabled (when VPORT byte-swap bug is fixed), then frame rates will be as expected.</p> <p>All other application:</p> <p>Frame rates and chroma will improve if run in RELEASE mode</p>	

<b>8.</b>	Colors are not proper in VESA display when viewed in DELL 1707FP LCD monitor.
<p>This is observed only in that particular LCD monitor. VESA display is proper in other CRT and LCD monitors. Suspected to be issue with the specific monitor.</p> <p><b>Workaround</b></p> <p>None</p>	

<b>9.</b>	Frame merging observed while capturing a <b>single</b> frame video (during screensaver display and not during actual movie display) from DVD player and observing the single frame in CCS or any image viewer. This is not observed in continuous video capturing
<p><b>Workaround</b></p> <p>This is observed only when capturing a frame from a DVD player. We suspect that the DVD player may not be delivering the screen saver in proper frames. When a frame is captured from another embedded device like DM642 EVM or DM648 EVM, this frame merging issue is not seen.</p>	

<b>10.</b>	Chroma artifacts observed while capturing a <b>single</b> frame video and observing the single frame in CCS or any image viewer or in video monitor.
<b>Workaround</b> None	

<b>11.</b>	8 Byte swapping problem due to big endian mode operation of video port in DM648.
<p>This issue is fixed in DM648 chip version 1.1 and above. The below mentioned workaround is not required if this version of chip is used.</p> <p><b>Workaround</b></p> <p>1) Before FVID exchange in display driver, swap each 8 bytes in the entire display buffer. For instance, exchange byte 0 with byte 7; exchange byte 1 with byte 6; exchange byte 2 with byte 5; exchange byte 3 with byte 4; exchange byte 8 with byte 15; exchange byte 9 with byte 14 and so on.</p> <p>B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15</p> <p>Should be changed to,</p> <p>B7 B6 B5 B4 B3 B2 B1 B0 B15 B14 B13 B12 B11 B10 B9 B8</p> <p>Where B represents a byte</p> <p>2) After FID exchange capture driver, swap each 8 bytes in the entire display buffer. Swap sequence is same as that mentioned for display buffer.</p>	

<b>12.</b>	<i>EDC_START, EDC_STOP, VPORT_CMD_RESET</i> IOCTLS not supported in the current driver
<b>Workaround</b> None	

<b>13.</b>	Vertical lines at the top portion of the SAA7105 video display (NTSC/PAL) appears zigzag and not straight
<p>Zigzag vertical lines observed in top portion of the displayed image. This effect gradually decreases as we move down the image and at the bottom portion the vertical lines are straight. Suspected to be clock issues in EVM</p> <p><b>Workaround</b></p> None	

<b>14.</b>	1080i 50Hz HD capture is not supported as proper testing of this mode is not done
<b>Workaround</b> None	

<b>15.</b>	In some of the production EVM, intermittent jerks and diagonal lines are observed. Where as some production EVMs does not exhibits this issue.
<b>Workaround</b> None	

## 9 Revision history

<b>Date</b>	<b>Author</b>	<b>Comments</b>	<b>Version</b>
March 23, 2007	Grishma Parikh\ Sivaraj R	Pre-silicon DSP/BIOS vport driver release	0.1
April 25, 2007	Sivaraj R	SD one to one loop back (VP0/A to VP1) release tested in EVMDM648	0.4.21 (Next release to 0.1)
May 2, 2007	Sivaraj R	SD D1 resolution simultaneous 8 channel capture to 1 channel display	0.5
June 14, 2007	Sivaraj R	HD Display and New FVID implementation	0.6
June 18, 2007	Sivaraj R	Updated for patch 1.10.00.00	0.7
July 16, 2007	Sivaraj R	Updated for patch 1.10.00.02	0.8
August 30, 2007	Sivaraj R	Updated for patch 1.10.00.04	0.9
September 17, 2007	Sivaraj R	Updated for MRs	0.10
September 20, 2007	Sivaraj R	Updated for patch 1.10.00.05	0.11
October 23, 2007	Sivaraj R	Updated for patch 1.10.00.06	0.12
November 19, 2007	Sivaraj R	Updated known issue section for THS7353 removal from production EVM	0.13
November 29, 2007	Sivaraj R	Updated for patch 1.10.00.08	0.14
January 14, 2008	Sivaraj R	Added THS7353 enable/disable macro in EDC driver. Error handling bugs fixed	0.15
February 20, 2008	Sivaraj R	Updated for patch 1.10.00.09	0.16
February 29, 2008	Sivaraj R	Updated release notes for HD capture known issues	0.17

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May 28, 2008	M Sriram	Updated for release 1.10.01	0.18
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