DSP\BIOS TSIP Device Driver

Release Notes

Release 1.10.03

April 16, 2009

The product release notes in this document are for C6452 BIOS TSIP Device Driver

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1 General information

The TSIP device driver included in this release package supports h/w capabilities of DSP TSIP peripheral device. The driver supports asynchronous I/O. The driver is based on an architecture that allows for easy customization/extension. The driver is multi-instantiable and re-entrant safe for use in multi-threaded environment.

1.1 Sample Application

The sample DSP/ BIOS application (sample folder) is a representative test program. This sample application demonstrates TSIP TX/RX data transfer in loop-back mode.

1.2 Test Setup for TSIP

To test the TSIP sample application in C6452 EVM, the user has to do the following setup before using the sample application.

1.2.1 Testing using external clock and frame sync sources

To use external clock, the "testClk" field of SIU configuration parameter (see the psp_bios_tsip_sample.c) to be set to external clock. (Note: The sample application shall only demonstrate loop back mode (DLB). However if the user wants to interface TSIP with TEMUX device or any other external devices, he/she can set "loopBack" to NONE and modify the sample application to his/her needs.)

```
tsip0DevParams.siu.loopBack = PSP_TSIP_LOOP_BACK_DLB;
tsip0DevParams.siu.testClk  = PSP_TSIP_TEST_CLK_EXTERNAL
```

To allow the external clock and frame sync into TSIP module some of the MUX configurations to be done. The following configurations to be done when using external clock sources for TSIP:

a) TSIP HW requires two external clock inputs, the clock signal and the frame sync signal in order to work. The user has to ensure that these clock signals have been derived from the proper external source. The parameters of the clock signals are as follows

Clock signal should be

8.192 MHz for 8.192 Mbps data rate and 1X mode

16.384 MHz for 8.192 Mbps data rate and 2X mode (Default)

16.384 MHz for 16.384 Mbps data rate and 1X mode

32.768 MHz for 16.384Mbps data rate and 2X mode

Frame sync signal/pulse 8 KHz (If it is a pulse the pulse width should be minimum of 2 or 3 clock cycles of the clock signal. Please see the TSIP functional specifications for clock requirements and polarity)

b) The voltage amplitude for Clock/Frame sync should not exceed 3.3 V.

c) Physical setup of clock signals: If the user wants to use TSIP0 instance, the clock, frame sync and ground should be given to CLK_A, FS_A and Ground terminals of TSIP0 in the daughter card interface and vice-versa for TSIP1.

d) In the EVM, TSIP clock signals are muxed with McASP signals. By default TSIP signals are disabled. So the user has to configure the TSIP/McASP mux on the

EVM to allow TSIP clock/frame sync signal to reach TSIP module. The MUX on the EVM is controlled by ECP (MSP430) through I2C.

- The MUX selection can be done using GEL file (got along with CCS or from EVM manufacturer), by running function "Set_Muxes_For_Mcasp_Dcc" from GEL menu of CCS.
- For those who do not use the GEL file option and try to communicate to ECP by alternate method (e.g. psp i2c driver) can use these parameters of ECP to change mux state.
    1) I2C Slave address: 0x70
    2) Offset: 0x13
    3) Data: 0x02

e) Ensure that SOC level pin muxing is taken care

f) Also refer to EVM reference guide from EVM manufacturer for further information.

1.3 Build Macros

TSIP driver uses the following functional build macros to enable/disable the particular functionality of the driver while building the driver library.

- PSP_TSIP_USE_FRAME_ISR when this is defined, this enables the TSIP driver to support frame ISR handling. This should be enabled if the application would like to register frame callback function. By default this macro is defined.
- PSP_TSIP_CACHEABLE_FRAMEBUFFER this macro should be defined if the D-cache is enabled and application uses IO buffers (Memory frame buffer) from a cacheable region. By default this is defined.

2 New In This Release

The user guide has been updated for the various pragma directives, macro definitions and compiler switches used in the driver.

3 System Requirements

Details about the tools and the BIOS version that the driver is compatible with can be found in the system Release Notes.

4 Installation and Usage

1. Install C6452 package as per instructions provided along with the package.
2. BIOS TSIP Device driver sources are available in <root>/drivers/tsip folder.
3. Build the TSIP project file in build directory to build the debug/release library.
4. Sample application /test code is provided in C6452 BIOS package.

5 Uninstallation

1. Un-install the C6452 BIOS package as per instructions provided with the package.

6 Fixed In This Release:

7 Known Issues:

1	
Workaround: None	