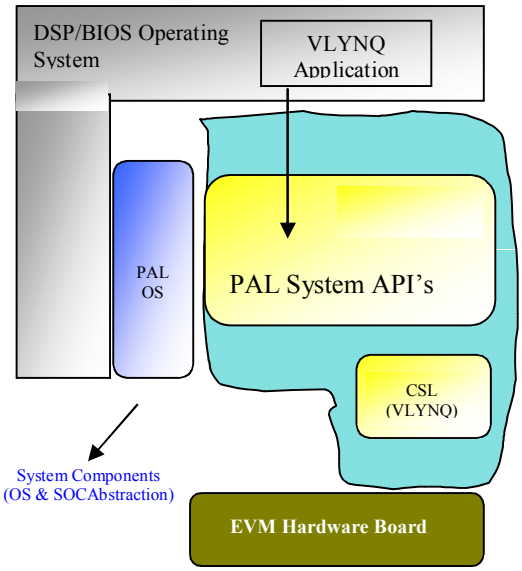
- **Re-entrant safe driver**




## Description

Refer system level release notes for tools and BIOS versions.

**Capabilities**

The PAL SYS VLYNQ DSP/BIOS device driver adopts a scalable architecture that eases customization/extension

- Isolates H/W and OS Accesses, Easy to maintain & re-target to new platforms
- Can stack custom-functions along control/data-path to realize “driver filters”

The driver is constituted of following sub components:

- VLYNQ – OS Independent part of VLYNQ Driver Core. This also includes CSL.
- System components – PALOS: BIOS Abstraction

The following table gives a quick overview of the supported API services. For help on interfaces refer to the PAL SYS VLYNQ Driver Help File:

| | |
|---|---|
| PAL_sysVlynqInit( ) | Initialize the VLYNQ control module. |
| PAL_sysVlynqInitSoc | Initialize the VLYNQ control module. |
| PAL_sysVlynqCleanUp( ) | Un-Initialize the VLYNQ control module. |
| PAL_sysVlynqDevCreate( ) | Creates a device reference. |
| PAL_sysVlynqDevDestroy( ) | Destroys the device reference. |
| PAL_sysVlynqMapRegion( ) | Map the memory regions of the device. |
| PAL_sysVlynqMappedRegion( ) | Return the Mapped Region configuration for Local/Peer. |
| PAL_sysVlynqUnMapRegion( ) | Unmap the memory regions of the De vice. |
| PAL_sysVlynqMapIrq( ) | Maps the IRQ hardware line onto the VLYNQ. |
| PAL_sysVlynqUnMapIrq( ) | Unmap the IRQ hardware line. |
| PAL_sysVlynqChainAppend( ) | Append to the VLYNQ chain. |
| PAL_sysVlynqAddDevice( ) | Add the device reference into VLYNQ. |
| PAL_sysVlynqRemoveDevice( ) | Removes the device reference from VLYNQ. |
| PAL_sysVlynqChainUnAppend( ) | Remove (the tail) from the VLYNQ chain. |
| PAL_sysVlynqRootIsr( ) | The Root ISR; register it with the system. |
| PAL_sysVlynqDevFind( ) | Get the handle for the device. |
| PAL_sysVlynqDevGetVlynq( ) | Get the VLYNQ for this device. |
| PAL_sysVlynqGetDevBase( ) | Get the physical base address of the device. |
| PAL_sysVlynqDevFindIrq( ) | Get the mapped interrupts of the device. |
| PAL_sysVlynqAddIsr( ) | Install the ISR for the device. |
| PAL_sysVlynqDevGetResetBit( ) | Get the reset bit of the device. |
| PAL_sysVlynqDevCbRegister( ) | Register for the callbacks. |
| PAL_sysVlynqDevCbUnregister( ) | Unregisters the callbacks. |
| PAL_sysVlynqIoctl( ) | Read/Write register of the VLYNQ module. |

| | |
|---|---|
| PAL_sysVlynqClockConfig( ) | Configures the Clock for the VLYNQ bridge. |
| PAL_sysVlynqGetForIrq( ) | Get the VLYNQ for the IRQ. |
| PAL_sysVlynqSetIrqPol( ) | Set the polarity of the hardware IRQ line. |
| PAL_sysVlynqSetIrqType( ) | Set the type of the hardware IRQ line. |
| PAL_sysVlynqGetIrqPol ( ) | Get the polarity of the hardware IRQ line. |
| PAL_sysVlynqGetIrqType( ) | Get the type of the hardware IRQ type. |
| PAL_sysVlynqGetIrqCount( ) | Get the number of times this IRQ occurred. |
| PAL_sysVlynqDisableIrq( ) | Disable the IRQ. |
| PAL_sysVlynqEnableIrq( ) | Enable the IRQ. |
| PAL_sysVlynqGetLinkStatus( ) | Get the status of the of the VLYNQ module. |
| PAL_sysVlynqGetNumRoot( ) | Get the number of the root VLYNQ(s) |
| PAL_sysVlynqGetRoot( ) | Get the handle to the specified root VLYNQ. |
| PAL_sysVlynqGetRootVLYNQ( ) | Get root for the given VLYNQ. |
| PAL_sysVlynqGetRootAtBase( ) | Get the root VLYNQ at the base address. |
| PAL_sysVlynqGetBaseAddr( ) | Returns the base address of the VLYNQ. |
| PAL_sysVlynqGetNext( ) | Get the next VLYNQ module in the chain. |
| PAL_sysVlynqIsLast( ) | Is this VLYNQ module the last one in the chain. |
| PAL_sysVlynqGetChainLength( ) | Get the length of the VLYNQ chain. |
| PAL_sysVlynqDump( ) | Dumps vital VLYNQ information into the buffer. |

**Driver Performance Characteristics:**

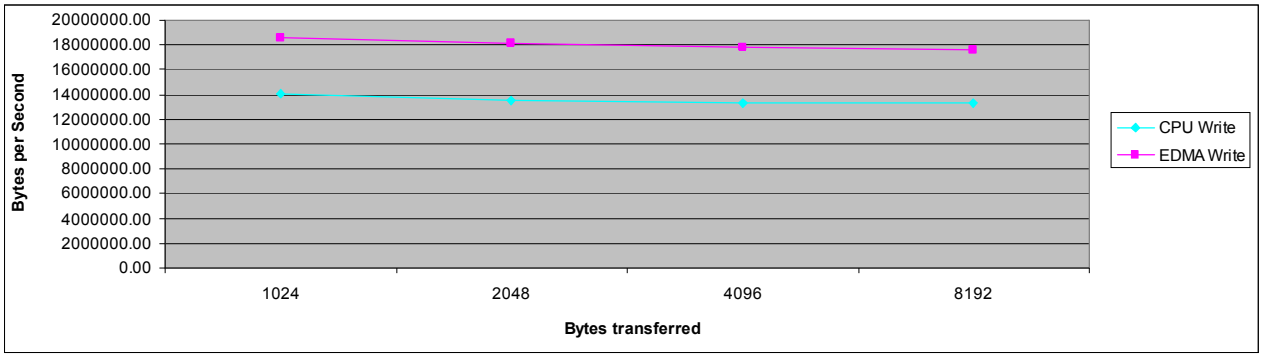
| VLYNQ DEVICE DRIVER SUB-COMPONENT | PROGRAM MEMORY (IN BYTES) | DATA MEMORY (IN BYTES) | | |
|---|---|---|---|---|
| | | MEMORY TYPE | | TOTAL |
| | | INITIALIZED | UN INITIALIZED | |
| <TOTAL> | 25408 | 2871 | 3180 | **31459** |

- System Components Total Memory (Code & Data): **31834** Bytes

**Driver Profiling characteristics**

| API Profiled | Trial-1 | Trial-2 | Trial-3 | Trial-4 | Trial-5 | Average (usec) | Maximum (usec) | Minimum (usec) |
|---|---|---|---|---|---|---|---|---|
| PAL_sysVlynqInitSoc | 23472.00 | 23472.00 | 23472.00 | 23472.00 | 23472.00 | 23472.00 | 23472.00 | 23472.00 |
| PAL_sysVlynqDevCreate | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqAddDevice | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqMapRegion | 1.00 | 0.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| PAL_sysVlynqMappedRegion | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| PAL_sysVlynqIoctl | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 |
| PAL_sysVlynqDump | 147.00 | 146.00 | 147.00 | 145.00 | 147.00 | 146.00 | 147.00 | 145.00 |
| PAL_sysVlynqDevGetVlynq | 35.00 | 34.00 | 35.00 | 33.00 | 35.00 | 34.00 | 35.00 | 33.00 |
| PAL_sysVlynqGetDevBase | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqGetLinkStatus | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqGetNumRoot | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqGetRoot | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqGetBaseAddr | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqGetRootVlynq | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqDevGetResetBit | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqUnMapRegion | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqRemoveDevice | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqDevDestroy | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 |
| PAL_sysVlynqCleanUp | 14.00 | 14.00 | 14.00 | 14.00 | 14.00 | 14.00 | 14.00 | 14.00 |

## Driver Performance Characteistics




| Test Setup Information | Buffer Size (Bytes) | CPU Write | | EDMA Write | |
|---|---|---|---|---|---|
| | | Time(usec) | Bytes/Sec | Time (usec) | Bytes/Sec |
| Kailash EVM inserted in PCI slot of Linux Host | 1024 | 73.00 | 14027397.26 | 55 | 18618181.82 |
| | 2048 | 151.00 | 13562913.91 | 113 | 18123893.81 |
| | 4096 | 307.00 | 13342019.54 | 230 | 17808695.65 |
| | 8192 | 618.00 | 13255663.43 | 465 | 17617204.30 |

Comments:

| |
|---|
| Input clock to Vlynq Module = 891/6 (PLL1/6) = 148.5MHZ |
| Clk divisor value = 3 (Set in Testcode) |
| Vlynq Clock = 148.5/3 = 49.5MHz |
| Number of lines connected - 4 TX and 4 RX |
| Number of bits transmitted \ clock = 4 bits |
| Write Theoretical Data rate = 4 bits * 49.5 MHZ = 198 Mbits/sec |

## References

[1] PAL SYS VLYNQ Module Hardware Specifications

[2] BIOS Documentation from TI

[3] PAL SYS VLYNQ Device Driver Documentation

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