




# **MSP432® Peripheral Driver Library**

## **USER'S GUIDE**

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## Revision Information

This is version of this document, last updated on Wed Aug 10 2016 3:07:52 PM.

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# 1 DriverLib Introduction

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## 1.1 What DriverLib is

The Texas Instruments MSP432 Driver Library (DriverLib) is a set of fully functional APIs used to configure, control, and manipulate the hardware peripherals of the MSP432 platform. In addition to being able to control the MSP432 peripherals, DriverLib also gives the user the ability to use common ARM peripherals such as the Interrupt (NVIC) and Memory Protection Unit (MPU) as well as MSP430 peripherals such as the eUSCI Serial peripherals and Watchdog Timer (WDT).

DriverLib for MSP432 Series has been tested and compiled under a variety of different toolchains. Subsequently, for each toolchain a specific debugger was used for testing validation. Below is a list that contains the supported toolchain and corresponding hardware debugger used.

- **Texas Instruments Code Composer Studio 6.1** (XDS100v3)
- **IAR Embedded Workbench for ARM 7.30** (SEGGER J-LINK)
- **GNU C Compiler 4.8 (gcc)** (SEGGER J-LINK)
- **Keil Embedded Development Tools for ARM 5.13** (KEIL U-LINK Pro)

The DriverLib is meant to provide a "software" layer to the programmer in order to facilitate higher level of programming compared to direct register accesses. Nearly every aspect of a MSP432 device can be configured and driven using the DriverLib APIs. By using the high level software APIs provided by DriverLib, users can create powerful and intuitive code which is highly portable between not only devices within the MSP432 platform, but between different families in the MSP430/MSP432 platforms.

Writing code in DriverLib will make user code more legible and easier to share among a group. For example, examine the following pair of code snippets. Both sets of code set MCLK to be sourced from VLO with a divider of four:

### Traditional Register Access

```
CSKEY = 0x695A;
CSCTL1 |= SELM_1 | DIVM_2;
CSKEY = 0;
```

### DriverLib Equivalent

```
CS_initClockSignal(CS_MCLK, CS_VLOCLK_SELECT, CS_CLOCK_DIVIDER_32);
```

As can be seen, the DriverLib API is readable, sensible, and easy to program for the software engineer. Additionally, DriverLib APIs for other platforms such as MSP430 will use very similar (if not identical) APIs giving code written with DriverLib APIs a boost in portability.

## 1.2 What DriverLib is not

The Driver Library is not meant to provide a layer of intelligence on the level of a user application. It is meant to be an aid to the programmer to be part of the larger solution- not the solution itself.

Interrupt handlers are also not included with the DriverLib APIs. APIs to manage/enable/disable interrupts are included, however the actual authoring of the interrupt service routine is left up to the programmer. For reference, A typical interrupt handler that takes advantage of DriverLib APIs can be seen in the following code snippet:

```
void port6_isr(void)
{
    uint32_t status = GPIO_getEnabledInterruptStatus(GPIO_PORT_P6);

    GPIO_clearInterruptFlag(GPIO_PORT_P6, status);

    if (status & GPIO_PIN7)
    {
        if (powerStates[curPowerState] == PCM_LPM3)
        {
            curPowerState = 0;
        }
        stateChange = true;
    }
}
```

## 1.3 Cross Module Considerations

Each DriverLib module will, for the most part, only interact and configure the module that it is designed for. Any cross-module interaction is left up to the user. For example, when changing power modes to a low frequency mode with the PCM module, the user will have to ensure that the proper frequency requirements are configured with the CS module (low frequency requires that the system frequency be no greater than 128Khz).

Calling the following API alone while MCLK is greater than 128Khz will result in a system error:

```
PCM_setPowerState(PCM_AM_LF_VCORE1);
```

This is because the DriverLib module will not account for the overall system frequency of the system. Instead, similar APIs to the following must be called in conjunction:

```
CS_setReferenceOscillatorFrequency(CS_REF0_128KHZ);
CS_initClockSignal(CS_MCLK, CS_REFCLK_SELECT, CS_CLOCK_DIVIDER_1);
PCM_setPowerState(PCM_AM_LF_VCORE1);
```

Cross-module considerations such as these must be taken when programming with DriverLib APIs as DriverLib was not designed to account for high level system requirements.

## 1.4 DriverLib in ROM

With all MSP432 devices, a copy of DriverLib is included within the device's ROM space. This allows programmers to take advantage of using high level APIs without having to worry about additional memory overhead of a flash library. In addition to a more optimized execution, the user can drastically cut down the memory footprint requirement of their application when using the software Driver Libraries available in ROM.

Accessing Driver Library APIs in ROM is as easy as including the rom.h header file, and then replacing normal API calls with a *ROM\_* prefix. For example, take the following API from the pcm.c module that changes the power state to PCM\_AM\_DCDC\_VCORE1:

```
PCM_setPowerState(PCM_AM_DCDC_VCORE1);
```

After including the rom.h file, all that would have to be done to switch to the ROM equivalent of the API would be add the *ROM\_* prefix to the API:

```
ROM_PCM_setPowerState(PCM_AM_DCDC_VCORE1);
```

While the majority of DriverLib APIs are available in ROM, due to architectural limitations some APIs are omitted from being included in ROM. In addition, if any bug fixes were added to the API after the device ROM was programmed, it is desirable to use the flash version of the API. An "intelligence" has been created to account for this problem. If the user includes the rom\_map.h header file and uses the *MAP\_* prefix in front of the API, the header file will automatically use preprocessor macros to decide whether to use a ROM or flash version of the API.

```
MAP_PCM_setPowerState(PCM_AM_DCDC_VCORE1);
```

## 1.5 MSP430 Legacy APIs

Since the MSP432 platform is built with many modules from Texas Instruments' MSP430 platform, many shared modules exist between MSP430 and MSP432. For this reason, a "compatibility" layer is provided to provide between the MSP430 Driver Library and the MSP430 Driver Library. The following modules are shared between MSP432 and MSP430:

- AES256
- COMP\_E
- CRC32
- GPIO
- EUSCI\_A\_SPI (SPI)
- EUSCI\_A\_UART (UART)
- EUSCI\_B\_I2C (I2C)
- EUSCI\_B\_SPI (SPI)
- PMAP
- REF\_A
- RTC\_C



- TIMER\_A
- WDT\_A

To use these legacy APIs, no additional work is needed. All that is needed is to include the header file of the module you want to use and both the old and the new APIs will be available. For example, for WDT\_A:

```
#include <wdt_a.h>
```

By including this header file, the user is granted access to all of the legacy DriverLib APIs from MSP430 Driver Library verbatim. For additional documentation on the MSP430 implementation of DriverLib, please refer to the [MSP430Ware Website](#).

Many of the APIs were simplified and refactored for the MSP432 version of Driver Library. For example, to halt the watchdog module for a 5xx MSP430 device, the following API is used:

```
WDT_A_hold(WDT_A_BASE);
```

For MSP432 Driver Library, this same API has been simplified to the following API:

```
WDT_A_holdTimer();
```

Note that while many Driver Library APIs are shared between MSP430 and MSP432, there are a few underlying differences between the two architectures. Interrupts, for example, are a bit difference on MSP432 compared to MSP430 due to integration with ARM's interrupt controller (the NVIC). While each module will still have individual status (IFG), enable/disable, and clear bits, interrupt service routines now have to be associated with the ARM NVIC before usage.

## 1.6 Quick Start

Getting started using DriverLib for MSP432 Series is very simple regardless of the chosen development environment.

An empty "skeleton" project is provided in the examples directory of the MSPWare release. This project includes links to the DriverLib library as well as everything that is needed for the programmer to immediately start writing a DriverLib application. A user can import this project in CCS using the TI Resource Explorer, or open the workspace with IAR Embedded Workbench for ARM or KEIL uVision 5. All of the include paths and compiler options are set up to allow the user to seamlessly start development on their MSP432 DriverLib application.

The GNU compiler tools for ARM are fully supported by the MSP432 Series DriverLib. While no IDE in specific is supported, Makefiles are provided for both the library and all of the code examples. Vector table definitions that are compatible with the GCC compiler are also provided for code examples in the `startup_gcc.c` file for each individual code example. For the GNU tools, separate header files are included in the `inc` directory of the root installation of DriverLib. These header files are the latest that are available at the time of DriverLib release, however newer header files may be downloaded as a part of the CCS installation.

## 2 14-Bit Analog-to-Digital Converter (ADC14)

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### 2.1 Module Operation

The ADC14 module for Driver Library is designed to allow the user to make simple analog to digital conversions as well make complex and simultaneous conversions across multiple channels.

### 2.2 Conversion Modes

With Single Conversion Mode, the user will sample only a single ADC channel which will be stored in a single ADC memory location. This is the most basic ADC sample/convert mode and allows for very simple measurements on a single channel. To configure single sample mode, only a single destination is configured for the sample/conversion result. The following is a code snippet for configuring/initializing the ADC module in single conversion mode as well as kicking off the start of conversion/sampling.

```

/* Initializing ADC (MCLK/1/4) */
MAP_ADC14_enableModule();
MAP_ADC14_initModule(ADC_CLOCKSOURCE_MCLK, ADC_PREDIVIDER_1, ADC_DIVIDER_4,
0);

/* Configuring GPIOs (5.5 A0) */
MAP_GPIO_setAsPeripheralModuleFunctionInputPin(GPIO_PORT_P5, GPIO_PIN5,
GPIO_TERTIARY_MODULE_FUNCTION);

/* Configuring ADC Memory */
MAP_ADC14_configureSingleSampleMode(ADC_MEM0, true);
MAP_ADC14_configureConversionMemory(ADC_MEM0, ADC_VREFPOS_AVCC_VREFNEG_VSS,
ADC_INPUT_A0, false);

/* Configuring Sample Timer */
MAP_ADC14_enableSampleTimer(ADC_MANUAL_ITERATION);

/* Enabling/Toggling Conversion */
MAP_ADC14_enableConversion();
MAP_ADC14_toggleConversionTrigger();

```

When using single sample mode, only one memory location will be written for a conversion/sample cycle. To access the result of this conversion, the ADC14\_getResult API is used with the corresponding memory location specified. This is usually done within the interrupt service routine of the ADC module.

```

/* ADC Interrupt Handler. This handler is called whenever there is a conversion
 * that is finished for ADC_MEM0.
 */
void ADC14_IRQHandler(void)
{
    uint64_t status = MAP_ADC14_getEnabledInterruptStatus();
    MAP_ADC14_clearInterruptFlag(status);

    if (ADC_INT0 & status)
    {
        curADCResult = MAP_ADC14_getResult(ADC_MEM0);
        normalizedADCRes = (curADCResult * 3.3) / 16384;

        MAP_ADC14_toggleConversionTrigger();
    }
}

```

The ADC14 APIs also support the setup/configuration of multiple conversion mode. With multiple conversion mode, multiple ADC channels are sampled and stored in multiple ADC memory addresses in a single sweep. This is particularly useful when the user wants to take a sample of multiple channels over a period of time (also known as scan mode). The ADC14\_getMultiSequenceResult function is used to populate the given array pointer with the result over a wide memory arrange (setup with ADC14\_configureMultiSequenceMode ).

## 2.3 Repeat Modes

When configuring the ADC module to use multiple or single sample/conversion mode, a boolean argument is provided to signal whether the DriverLib ADC module should work in "repeat" mode. With repeat mode, once a conversion/sample is completed and read by the API, a new conversion happens until the user manually stops conversion using the ADC14\_toggleConversionTrigger command. Repeat mode is useful when the user wants to continuously sample an ADC channel over an extended period of time.

When repeat mode is specified to be false, whenever a conversion/sample is finished and read from the result register, the module will stop conversion until called by the ADC14\_toggleConversionTrigger function.

## 2.4 Conversion of Results

When reading a result of an ADC14 conversion, it is important to note that the result will be relevant to the current resolution of the ADC14 device. For example, say the ADC14 module is setup with a 14-bit resolution and a positive reference of 2.5v (and a negative of 0v). In this case, if the conversion result of 16383 would signify a value of 2.5v (if in unsigned) mode. A snippet of code that converts the conversion result in the ADC register to a real life value can be seen in the following:

```

/* Converts the ADC result (14-bit) to a float with respect to a 3.3v reference
*/
static float convertToFloat(uint16_t result)
{
    int32_t temp;

    if(0x8000 & result)
    {
        temp = (result >> 2) | 0xFFFFC000;
        return ((temp * 3.3f) / 8191);
    }
    else
        return ((result >> 2)*3.3f) / 8191;
}

```

It is important to note that when using floating point arithmetic, it is important to enable the devices FPU (if available) to save CPU cycles and energy consumption.

## 2.5 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the ADC14 module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the ADC14 module in single sample mode. For a set of more detailed code examples, please refer to the code examples in the examples/ directory of the MSPWare release:

```

/* Initializing ADC (MCLK/1/1) */
ADC14_enableModule();
ADC14_initModule(ADC_CLOCKSOURCE_MCLK, ADC_PREDIVIDER_1, ADC_DIVIDER_1,
0);

/* Configuring ADC Memory (ADC_MEM0 A0/A1) in repeat mode
 * with use of external references */
ADC14_configureSingleSampleMode(ADC_MEM0, true);
ADC14_configureConversionMemory(ADC_MEM0,
ADC_VREFPOS_EXTPOS_VREFNEG_EXTNEG,
ADC_INPUT_A0, false);

/* Setting up GPIO pins as analog inputs (and references) */
GPIO_setAsPeripheralModuleFunctionInputPin(GPIO_PORT_P5,
GPIO_PIN7 | GPIO_PIN6 | GPIO_PIN5 | GPIO_PIN4, GPIO_TERTIARY_MODULE_FUNCTION);

/* Enabling sample timer in auto iteration mode and interrupts*/
ADC14_enableSampleTimer(ADC_AUTOMATIC_ITERATION);
ADC14_enableInterrupt(ADC_INT0);

/* Enabling Interrupts */
Interrupt_enableInterrupt(INT_ADC14);

```

```
Interrupt_enableMaster();  
  
/* Triggering the start of the sample */  
ADC14_enableConversion();  
ADC14_toggleConversionTrigger();
```

## 2.6 Definitions

### Functions

- void [ADC14\\_clearInterruptFlag](#) (uint\_fast64\_t mask)
- bool [ADC14\\_configureConversionMemory](#) (uint32\_t memorySelect, uint32\_t refSelect, uint32\_t channelSelect, bool differentialMode)
- bool [ADC14\\_configureMultiSequenceMode](#) (uint32\_t memoryStart, uint32\_t memoryEnd, bool repeatMode)
- bool [ADC14\\_configureSingleSampleMode](#) (uint32\_t memoryDestination, bool repeatMode)
- bool [ADC14\\_disableComparatorWindow](#) (uint32\_t memorySelect)
- void [ADC14\\_disableConversion](#) (void)
- void [ADC14\\_disableInterrupt](#) (uint\_fast64\_t mask)
- bool [ADC14\\_disableModule](#) (void)
- bool [ADC14\\_disableReferenceBurst](#) (void)
- bool [ADC14\\_disableSampleTimer](#) (void)
- bool [ADC14\\_enableComparatorWindow](#) (uint32\_t memorySelect, uint32\_t windowSelect)
- bool [ADC14\\_enableConversion](#) (void)
- void [ADC14\\_enableInterrupt](#) (uint\_fast64\_t mask)
- void [ADC14\\_enableModule](#) (void)
- bool [ADC14\\_enableReferenceBurst](#) (void)
- bool [ADC14\\_enableSampleTimer](#) (uint32\_t multiSampleConvert)
- uint\_fast64\_t [ADC14\\_getEnabledInterruptStatus](#) (void)
- uint\_fast64\_t [ADC14\\_getInterruptStatus](#) (void)
- void [ADC14\\_getMultiSequenceResult](#) (uint16\_t \*res)
- uint\_fast32\_t [ADC14\\_getResolution](#) (void)
- uint\_fast16\_t [ADC14\\_getResult](#) (uint32\_t memorySelect)
- void [ADC14\\_getResultArray](#) (uint32\_t memoryStart, uint32\_t memoryEnd, uint16\_t \*res)
- bool [ADC14\\_initModule](#) (uint32\_t clockSource, uint32\_t clockPredivider, uint32\_t clockDivider, uint32\_t internalChannelMask)
- bool [ADC14\\_isBusy](#) (void)
- void [ADC14\\_registerInterrupt](#) (void(\*intHandler)(void))
- bool [ADC14\\_setComparatorWindowValue](#) (uint32\_t window, int16\_t low, int16\_t high)
- bool [ADC14\\_setPowerMode](#) (uint32\_t powerMode)
- void [ADC14\\_setResolution](#) (uint32\_t resolution)
- bool [ADC14\\_setResultFormat](#) (uint32\_t resultFormat)
- bool [ADC14\\_setSampleHoldTime](#) (uint32\_t firstPulseWidth, uint32\_t secondPulseWidth)
- bool [ADC14\\_setSampleHoldTrigger](#) (uint32\_t source, bool invertSignal)
- bool [ADC14\\_toggleConversionTrigger](#) (void)
- void [ADC14\\_unregisterInterrupt](#) (void)

### 2.6.1 Detailed Description

The code for this module is contained in `driverlib/adc14.c`, with `driverlib/adc14.h` containing the API declarations for use by applications.

## 2.6.2 Function Documentation

### 2.6.2.1 void ADC14\_clearInterruptFlag ( uint\_fast64\_t mask )

Clears the indicated ADCC interrupt sources.

#### Parameters

<i>mask</i>	<p>is the bit mask of interrupts to clear. The ADC_INT0 through ADC_INT31 parameters correspond to a completion event of the corresponding memory location. For example, when the ADC_MEM0 location finishes a conversion cycle, the ADC_INT0 interrupt will be set. Valid values are a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_INT0</b> through ADC_INT31</li> <li>■ <b>ADC_IN_INT</b> - Interrupt enable for a conversion in the result register is either greater than the ADCLO or lower than the ADCHI threshold.</li> <li>■ <b>ADC_LO_INT</b> - Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the result register.</li> <li>■ <b>ADC_HI_INT</b> - Interrupt enable for the exceeding the upper limit of the window comparator for the result register.</li> <li>■ <b>ADC_OV_INT</b> - Interrupt enable for a conversion that is about to save to a memory buffer that has not been read out yet.</li> <li>■ <b>ADC_TOV_INT</b> -Interrupt enable for a conversion that is about to start before the previous conversion has been completed.</li> <li>■ <b>ADC_RDY_INT</b> -Interrupt enable for the local buffered reference ready signal.</li> </ul>
-------------	--

#### Returns

NONE

### 2.6.2.2 bool ADC14\_configureConversionMemory ( uint32\_t memorySelect, uint32\_t refSelect, uint32\_t channelSelect, bool differentialMode )

Configures an individual memory location for the ADC module.



**Parameters**

<i>memorySelect</i>	is the individual ADC memory location to configure. If multiple memory locations want to be configured with the same configuration, this value can be logically ORed together with other values.  <ul style="list-style-type: none"> <li>■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b></li> </ul>
<i>refSelect</i>	is the voltage reference to use for the selected memory spot. Possible values include:  <ul style="list-style-type: none"> <li>■ <b>ADC_VREFPOS_AVCC_VREFNEG_VSS</b> [DEFAULT]</li> <li>■ <b>ADC_VREFPOS_INTBUF_VREFNEG_VSS</b></li> <li>■ <b>ADC_VREFPOS_EXTPOS_VREFNEG_EXTNEG</b></li> <li>■ <b>ADC_VREFPOS_EXTBUF_VREFNEG_EXTNEG</b></li> </ul>
<i>channelSelect</i>	selects the channel to be used for ADC sampling. Note if differential mode is enabled, the value sampled will be equal to the difference between the corresponding even/odd memory locations. Possible values are:  <ul style="list-style-type: none"> <li>■ <b>ADC_INPUT_A0</b> through <b>ADC_INPUT_A31</b></li> </ul>
<i>differentialMode</i>	selects if the channel selected by the channelSelect will be configured in differential mode. If this parameter is given as true, the configured channel will be paired with its neighbor in differential mode. for example, if channel A0 or A1 is selected, the channel configured will be the difference between A0 and A1. If A2 or A3 are selected, the channel configured will be the difference between A2 and A3 (and so on). Users can enter true or false, or one of the following values:  <ul style="list-style-type: none"> <li>■ <b>ADC_NONDIFFERENTIAL_INPUTS</b></li> <li>■ <b>ADC_DIFFERENTIAL_INPUTS</b></li> </ul>

**Returns**

false if setting fails due to an in progress conversion

### 2.6.2.3 bool ADC14\_configureMultiSequenceMode ( uint32\_t *memoryStart*, uint32\_t *memoryEnd*, bool *repeatMode* )

Configures the ADC module to use a multiple memory sample scheme. This means that multiple samples will consecutively take place and be stored in multiple memory locations. The first sample/conversion will be placed in *memoryStart*, while the last sample will be stored in *memoryEnd*. Each memory location should be configured individually using the `ADC14_configureConversionMemory` function.

The ADC module can be started in "repeat" mode which will cause the ADC module to resume sampling once the initial sample/conversion set is executed. For multi-sample mode, this means that the sampling of the entire memory provided.

**Parameters**

<i>memoryStart</i>	Memory location to store first sample/conversion value. Possible values include: ■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b>
<i>memoryEnd</i>	Memory location to store last sample. Possible values include: ■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b>
<i>repeatMode</i>	Specifies whether or not to repeat the conversion/sample cycle after the first round of sample/conversions. Valid values are true or false.

**Returns**

false if setting fails due to an in progress conversion

#### 2.6.2.4 bool ADC14\_configureSingleSampleMode ( uint32\_t *memoryDestination*, bool *repeatMode* )

Configures the ADC module to use a a single ADC memory location for sampling/conversion. This is used when only one channel might be needed for conversion, or where using a multiple sampling scheme is not important.

The ADC module can be started in "repeat" mode which will cause the ADC module to resume sampling once the initial sample/conversion set is executed. In single sample mode, this will cause the ADC module to continuously sample into the memory destination provided.

**Parameters**

<i>memoryDestination</i>	Memory location to store sample/conversion value. Possible values include: ■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b>
<i>repeatMode</i>	Specifies whether or not to repeat the conversion/sample cycle after the first round of sample/conversions

**Returns**

false if setting fails due to an in progress conversion

#### 2.6.2.5 bool ADC14\_disableComparatorWindow ( uint32\_t *memorySelect* )

Disables the comparator window on the specified memory channels

**Parameters**

<i>memorySelect</i>	is the mask of memory locations to disable the comparator window for. This can be a bitwise OR of the following values: ■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b>
---------------------	---

**Returns**

false if setting fails due to an in progress conversion

## 2.6.2.6 void ADC14\_disableConversion ( void )

Halts conversion conversion of the ADC module. Note that the software bit for triggering conversions will also be cleared with this function.

If multi-sequence conversion mode was enabled, the position of the last completed conversion can be retrieved using ADCLastConversionMemoryGet

**Returns**

none

2.6.2.7 void ADC14\_disableInterrupt ( uint\_fast64\_t *mask* )

Disables the indicated ADCC interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. The ADC\_INT0 through ADC\_INT31 parameters correspond to a completion event of the corresponding memory location. For example, when the ADC\_MEM0 location finishes a conversion cycle, the ADC\_INT0 interrupt will be set.

**Parameters**

<i>mask</i>	<p>is the bit mask of interrupts to disable. Valid values are a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_INT0</b> through ADC_INT31</li> <li>■ <b>ADC_IN_INT</b> - Interrupt enable for a conversion in the result register is either greater than the ADCLO or lower than the ADCHI threshold.</li> <li>■ <b>ADC_LO_INT</b> - Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the result register.</li> <li>■ <b>ADC_HI_INT</b> - Interrupt enable for the exceeding the upper limit of the window comparator for the result register.</li> <li>■ <b>ADC_OV_INT</b> - Interrupt enable for a conversion that is about to save to a memory buffer that has not been read out yet.</li> <li>■ <b>ADC_TOV_INT</b> -Interrupt enable for a conversion that is about to start before the previous conversion has been completed.</li> <li>■ <b>ADC_RDY_INT</b> -Interrupt enable for the local buffered reference ready signal.</li> </ul>
-------------	--

**Returns**

NONE

## 2.6.2.8 bool ADC14\_disableModule ( void )

Disables the ADC block.

This will disable operation of the ADC block.

**Returns**

false if user is trying to disable during active conversion

## 2.6.2.9 bool ADC14\_disableReferenceBurst ( void )

Disables the "on-demand" activity of the voltage reference register.

**Returns**

false if setting fails due to an in progress conversion

## 2.6.2.10 bool ADC14\_disableSampleTimer ( void )

Disables SAMPCON from being sourced from the sample timer.

**Returns**

false if the initialization fails due to an in progress conversion

2.6.2.11 bool ADC14\_enableComparatorWindow ( uint32\_t *memorySelect*, uint32\_t *windowSelect* )

Enables the specified mask of memory channels to use the specified comparator window. The ADC module has two different comparator windows that can be set with this function.

**Parameters**

<i>memorySelect</i>	is the mask of memory locations to enable the comparator window for. This can be a bitwise OR of the following values: <ul style="list-style-type: none"> <li>■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b></li> </ul>
<i>windowSelect</i>	Memory location to store sample/conversion value. Possible values include: <b>ADCOMP_WINDOW0</b> [DEFAULT] <b>ADCOMP_WINDOW1</b>

**Returns**

false if setting fails due to an in progress conversion

## 2.6.2.12 bool ADC14\_enableConversion ( void )

Enables conversion of ADC data. Note that this only enables conversion. To trigger the conversion, you will have to call the ADC14\_toggleConversionTrigger or use the source trigger configured in ADC14\_setSampleHoldTrigger.

**Returns**

false if setting fails due to an in progress conversion

### 2.6.2.13 void ADC14\_enableInterrupt ( uint\_fast64\_t mask )

Enables the indicated ADCC interrupt sources. The ADC\_INT0 through ADC\_INT31 parameters correspond to a completion event of the corresponding memory location. For example, when the ADC\_MEM0 location finishes a conversion cycle, the ADC\_INT0 interrupt will be set.

#### Parameters

<i>mask</i>	<p>is the bit mask of interrupts to enable. Valid values are a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_INT0</b> through ADC_INT31</li> <li>■ <b>ADC_IN_INT</b> - Interrupt enable for a conversion in the result register is either greater than the ADCLO or lower than the ADCHI threshold.</li> <li>■ <b>ADC_LO_INT</b> - Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the result register.</li> <li>■ <b>ADC_HI_INT</b> - Interrupt enable for the exceeding the upper limit of the window comparator for the result register.</li> <li>■ <b>ADC_OV_INT</b> - Interrupt enable for a conversion that is about to save to a memory buffer that has not been read out yet.</li> <li>■ <b>ADC_TOV_INT</b> - Interrupt enable for a conversion that is about to start before the previous conversion has been completed.</li> <li>■ <b>ADC_RDY_INT</b> - Interrupt enable for the local buffered reference ready signal.</li> </ul>
-------------	---

#### Returns

NONE

### 2.6.2.14 void ADC14\_enableModule ( void )

Enables the ADC block.

This will enable operation of the ADC block.

#### Returns

none.

### 2.6.2.15 bool ADC14\_enableReferenceBurst ( void )

Enables the "on-demand" activity of the voltage reference register. If this setting is enabled, the internal voltage reference buffer will only be updated during a sample or conversion cycle. This is used to optimize power consumption.

#### Returns

false if setting fails due to an in progress conversion

2.6.2.16 `bool ADC14_enableSampleTimer ( uint32_t multiSampleConvert )`

Enables SAMPCON to be sourced from the sampling timer and to configures multi sample and conversion mode.

**Parameters**

<i>multiSample-Convert</i>	<p>- Switches between manual and automatic iteration when using the sample timer. Valid values are:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_MANUAL_ITERATION</b> The user will have to manually set the SHI signal ( usually by <code>ADC14_toggleConversionTrigger</code> ) at the end of each sample/conversion cycle.</li> <li>■ <b>ADC_AUTOMATIC_ITERATION</b> After one sample/convert is finished, the ADC module will automatically continue on to the next sample</li> </ul>
----------------------------	--

**Returns**

false if the initialization fails due to an in progress conversion

### 2.6.2.17 `uint_fast64_t ADC14_getEnabledInterruptStatus ( void )`

Returns the status of a the ADC interrupt register masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR. The `ADC_INT0` through `ADC_INT31` parameters correspond to a completion event of the corresponding memory location. For example, when the `ADC_MEM0` location finishes a conversion cycle, the `ADC_INT0`

**Returns**

The interrupt status. Value is a bitwise OR of the following values:

- **ADC\_INT0** through **ADC\_INT31**
- **ADC\_IN\_INT** - Interrupt enable for a conversion in the result register is either greater than the `ADCLO` or lower than the `ADCHI` threshold.
- **ADC\_LO\_INT** - Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the result register.
- **ADC\_HI\_INT** - Interrupt enable for the exceeding the upper limit of the window comparator for the result register.
- **ADC\_OV\_INT** - Interrupt enable for a conversion that is about to save to a memory buffer that has not been read out yet.
- **ADC\_TOV\_INT** -Interrupt enable for a conversion that is about to start before the previous conversion has been completed.
- **ADC\_RDY\_INT** -Interrupt enable for the local buffered reference ready signal.

References [ADC14\\_getInterruptStatus\(\)](#).

### 2.6.2.18 `uint_fast64_t ADC14_getInterruptStatus ( void )`

Returns the status of a the ADC interrupt register. The `ADC_INT0` through `ADC_INT31` parameters correspond to a completion event of the corresponding memory location. For example, when the `ADC_MEM0` location finishes a conversion cycle, the `ADC_INT0` interrupt will be set.

**Returns**

The interrupt status. Value is a bitwise OR of the following values:

- **ADC\_INT0** through ADC\_INT31
- **ADC\_IN\_INT** - Interrupt enable for a conversion in the result register is either greater than the ADCLO or lower than the ADCHI threshold.
- **ADC\_LO\_INT** - Interrupt enable for the falling short of the lower limit interrupt of the window comparator for the result register.
- **ADC\_HI\_INT** - Interrupt enable for the exceeding the upper limit of the window comparator for the result register.
- **ADC\_OV\_INT** - Interrupt enable for a conversion that is about to save to a memory buffer that has not been read out yet.
- **ADC\_TOV\_INT** - Interrupt enable for a conversion that is about to start before the previous conversion has been completed.
- **ADC\_RDY\_INT** - Interrupt enable for the local buffered reference ready signal.

Referenced by [ADC14\\_getEnabledInterruptStatus\(\)](#).

### 2.6.2.19 void ADC14\_getMultiSequenceResult ( uint16\_t \* res )

Returns the conversion results of the currently configured multi-sequence conversion. If a multi-sequence conversion has not happened, this value is unreliable. Note that it is up to the user to verify the integrity of and proper size of the array being passed. If there are 16 multi-sequence results, and an array with only 4 elements allocated is passed, invalid memory settings will occur

**Parameters**

<i>res</i>	conversion result of the last multi-sequence sample in an array of unsigned 16-bit integers
------------	---

**Returns**

None

### 2.6.2.20 uint\_fast32\_t ADC14\_getResolution ( void )

Gets the resolution of the ADC module.

**Returns**

Resolution of the ADC module

- **ADC\_8BIT** (10 clock cycle conversion time)
- **ADC\_10BIT** (12 clock cycle conversion time)
- **ADC\_12BIT** (14 clock cycle conversion time)
- **ADC\_14BIT** (16 clock cycle conversion time)

### 2.6.2.21 uint\_fast16\_t ADC14\_getResult ( uint32\_t *memorySelect* )

Returns the conversion result for the specified memory channel in the format assigned by the ADC14\_setResultFormat (unsigned binary by default) function.



**Parameters**

<i>memorySelect</i>	is the memory location to get the conversion result. Valid values are: <ul style="list-style-type: none"> <li>■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b></li> </ul>
---------------------	--

**Returns**

conversion result of specified memory channel

2.6.2.22 void ADC14\_getResultArray ( uint32\_t *memoryStart*, uint32\_t *memoryEnd*, uint16\_t \* *res* )

Returns the conversion results of the specified ADC memory locations. Note that it is up to the user to verify the integrity of and proper size of the array being passed. If there are 16 multi-sequence results, and an array with only 4 elements allocated is passed, invalid memory settings will occur. This function is inclusive.

**Parameters**

<i>memoryStart</i>	is the memory location to get the conversion result. Valid values are: <ul style="list-style-type: none"> <li>■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b></li> </ul>
<i>memoryEnd</i>	is the memory location to get the conversion result. Valid values are: <ul style="list-style-type: none"> <li>■ <b>ADC_MEM0</b> through <b>ADC_MEM31</b></li> </ul>
<i>res</i>	conversion result of the last multi-sequence sample in an array of unsigned 16-bit integers

**Returns**

None

2.6.2.23 bool ADC14\_initModule ( uint32\_t *clockSource*, uint32\_t *clockPredivider*, uint32\_t *clockDivider*, uint32\_t *internalChannelMask* )

Initializes the ADC module and sets up the clock system divider/pre-divider. This initialization function will also configure the internal/external signal mapping.

**Note**

A call to this function while active ADC conversion is happening is an invalid case and will result in a false value being returned.

**Parameters**

<i>clockSource</i>	<p>The clock source to use for the ADC module.</p> <ul style="list-style-type: none"> <li>■ <b>ADC_CLOCKSOURCE_ADCOSC</b> [DEFAULT]</li> <li>■ <b>ADC_CLOCKSOURCE_SYSOSC</b></li> <li>■ <b>ADC_CLOCKSOURCE_ACLK</b></li> <li>■ <b>ADC_CLOCKSOURCE_MCLK</b></li> <li>■ <b>ADC_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>ADC_CLOCKSOURCE_HSMCLK</b></li> </ul>
<i>clockPredivider</i>	<p>Divides the given clock source before feeding it into the main clock divider. Valid values are:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_PREDIVIDER_1</b> [DEFAULT]</li> <li>■ <b>ADC_PREDIVIDER_4</b></li> <li>■ <b>ADC_PREDIVIDER_32</b></li> <li>■ <b>ADC_PREDIVIDER_64</b></li> </ul>
<i>clockDivider</i>	<p>Divides the pre-divided clock source Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>ADC_DIVIDER_1</b> [Default value]</li> <li>■ <b>ADC_DIVIDER_2</b></li> <li>■ <b>ADC_DIVIDER_3</b></li> <li>■ <b>ADC_DIVIDER_4</b></li> <li>■ <b>ADC_DIVIDER_5</b></li> <li>■ <b>ADC_DIVIDER_6</b></li> <li>■ <b>ADC_DIVIDER_7</b></li> <li>■ <b>ADC_DIVIDER_8</b></li> </ul>

<i>internalChannelMask</i>	<p>Configures the internal/external pin mappings for the ADC modules. This setting determines if the given ADC channel or component is mapped to an external pin (default), or routed to an internal component. This parameter is a bit mask where a logical high value will switch the component to the internal routing. For a list of internal routings, please refer to the device specific data sheet. Valid values are a logical OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>ADC_MAPINTCH3</b></li> <li>■ <b>ADC_MAPINTCH2</b></li> <li>■ <b>ADC_MAPINTCH1</b></li> <li>■ <b>ADC_MAPINTCH0</b></li> <li>■ <b>ADC_TEMPSENSEMAP</b></li> <li>■ <b>ADC_BATTMAP</b></li> <li>■ <b>ADC_NOROUTE</b> If <i>internalChannelMask</i> is not desired, pass <b>ADC_NOROUTE</b> in lieu of this parameter.</li> </ul>
----------------------------	---

**Returns**

false if the initialization fails due to an in progress conversion

2.6.2.24 `bool ADC14_isBusy ( void )`

Returns a boolean value that tells if a conversion/sample is in progress

**Returns**

true if conversion is active, false otherwise

2.6.2.25 `void ADC14_registerInterrupt ( void(*)(void) intHandler )`

Registers an interrupt handler for the ADC interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the ADC interrupt occurs.
-------------------	--

This function registers the handler to be called when an ADC interrupt occurs. This function enables the global interrupt in the interrupt controller; specific ADC14 interrupts must be enabled via [ADC14\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [ADC14\\_clearInterruptFlag\(\)](#).

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 2.6.2.26 bool ADC14\_setComparatorWindowValue ( uint32\_t *window*, int16\_t *low*, int16\_t *high* )

Sets the lower and upper limits of the specified window comparator. Note that this function will truncate values based on the resolution/data format configured. If the ADC is operating in 10-bit mode, and a 12-bit value is passed into this function the most significant 2 bits will be truncated.

The parameters provided to this function for the upper and lower threshold depend on the current resolution for the ADC. For example, if configured in 12-bit mode, a 12-bit resolution is the maximum that can be provided for the window. If in 2's complement mode, Bit 15 is used as the MSB.

#### Parameters

<i>window</i>	Memory location to store sample/conversion value. Possible values include: <b>ADC_COMP_WINDOW0</b> [DEFAULT] <b>ADC_COMP_WINDOW1</b>
<i>low</i>	is the lower limit of the window comparator
<i>high</i>	is the upper limit of the window comparator

#### Returns

false if setting fails due to an in progress conversion

### 2.6.2.27 bool ADC14\_setPowerMode ( uint32\_t *powerMode* )

Sets the power mode of the ADC module. A more aggressive power mode will restrict the number of samples per second for sampling while optimizing power consumption. Ideally, if power consumption is a concern, this value should be set to the most restrictive setting that satisfies your sampling requirement.

#### Parameters

<i>adcPowerMode</i>	is the power mode to set. Valid values are: <ul style="list-style-type: none"> <li>■ <b>ADC_UNRESTRICTED_POWER_MODE</b> (no restriction)</li> <li>■ <b>ADC_LOW_POWER_MODE</b> (500ksps restriction)</li> <li>■ <b>ADC_ULTRA_LOW_POWER_MODE</b> (200ksps restriction)</li> <li>■ <b>ADC_EXTREME_LOW_POWER_MODE</b> (50ksps restriction)</li> </ul>
---------------------	---

#### Returns

false if setting fails due to an in progress conversion

### 2.6.2.28 void ADC14\_setResolution ( uint32\_t *resolution* )

Sets the resolution of the ADC module. The default resolution is 12-bit, however for power consumption concerns this can be limited to a lower resolution

**Parameters**

<i>resolution</i>	Resolution of the ADC module <ul style="list-style-type: none"> <li>■ <b>ADC_8BIT</b> (10 clock cycle conversion time)</li> <li>■ <b>ADC_10BIT</b> (12 clock cycle conversion time)</li> <li>■ <b>ADC_12BIT</b> (14 clock cycle conversion time)</li> <li>■ <b>ADC_14BIT</b> (16 clock cycle conversion time)[DEFAULT]</li> </ul>
-------------------	---

**Returns**

none

2.6.2.29 `bool ADC14_setResultFormat ( uint32_t resultFormat )`

Switches between a binary unsigned data format and a signed 2's complement data format.

**Parameters**

<i>resultFormat</i>	Format for result to conversion results. Possible values include: <b>ADC_UNSIGNED_BINARY</b> [DEFAULT] <b>ADC_SIGNED_BINARY</b>
---------------------	--

**Returns**

false if setting fails due to an in progress conversion

2.6.2.30 `bool ADC14_setSampleHoldTime ( uint32_t firstPulseWidth, uint32_t secondPulseWidth )`

Sets the sample/hold time for the specified memory register range. The duration of time required for a sample differs depending on the user's hardware configuration.

There are two values in the ADCC module. The first value controls ADC memory locations `ADC_MEMORY_0` through `ADC_MEMORY_7` and `ADC_MEMORY_24` through `ADC_MEMORY_31`, while the second value controls memory locations `ADC_MEMORY_8` through `ADC_MEMORY_23`.

**Parameters**

<i>firstPulseWidth</i>	Pulse width of the first pulse in ADCCLK cycles Possible values must be one of the following: <ul style="list-style-type: none"> <li>■ <b>ADC_PULSE_WIDTH_4</b> [DEFAULT]</li> <li>■ <b>ADC_PULSE_WIDTH_8</b></li> <li>■ <b>ADC_PULSE_WIDTH_16</b></li> <li>■ <b>ADC_PULSE_WIDTH_32</b></li> <li>■ <b>ADC_PULSE_WIDTH_64</b></li> <li>■ <b>ADC_PULSE_WIDTH_96</b></li> <li>■ <b>ADC_PULSE_WIDTH_128</b></li> <li>■ <b>ADC_PULSE_WIDTH_192</b></li> </ul>
<i>second-PulseWidth</i>	Pulse width of the second pulse in ADCCLK cycles. Possible values must be one of the following: <ul style="list-style-type: none"> <li>■ <b>ADC_PULSE_WIDTH_4</b> [DEFAULT]</li> <li>■ <b>ADC_PULSE_WIDTH_8</b></li> <li>■ <b>ADC_PULSE_WIDTH_16</b></li> <li>■ <b>ADC_PULSE_WIDTH_32</b></li> <li>■ <b>ADC_PULSE_WIDTH_64</b></li> <li>■ <b>ADC_PULSE_WIDTH_96</b></li> <li>■ <b>ADC_PULSE_WIDTH_128</b></li> <li>■ <b>ADC_PULSE_WIDTH_192</b></li> </ul>

**Returns**

false if setting fails due to an in progress conversion

### 2.6.2.31 bool ADC14\_setSampleHoldTrigger ( uint32\_t *source*, bool *invertSignal* )

Sets the source for the trigger of the ADC module. By default, this value is configured to a software source (the ADCSC bit), however depending on the specific device the trigger can be set to different sources (for example, a timer output). These sources vary from part to part and the user should refer to the device specific datasheet.

## Parameters

<i>source</i>	Trigger source for sampling. Possible values include: <ul style="list-style-type: none"> <li>■ <b>ADC_TRIGGER_ADCSC</b> [DEFAULT]</li> <li>■ <b>ADC_TRIGGER_SOURCE1</b></li> <li>■ <b>ADC_TRIGGER_SOURCE2</b></li> <li>■ <b>ADC_TRIGGER_SOURCE3</b></li> <li>■ <b>ADC_TRIGGER_SOURCE4</b></li> <li>■ <b>ADC_TRIGGER_SOURCE5</b></li> <li>■ <b>ADC_TRIGGER_SOURCE6</b></li> <li>■ <b>ADC_TRIGGER_SOURCE7</b></li> </ul>
<i>invertSignal</i>	When set to true, will invert the trigger signal to a falling edge. When false, will use a rising edge.

**Returns**

false if setting fails due to an in progress conversion

2.6.2.32 `bool ADC14_toggleConversionTrigger ( void )`

Toggles the trigger for conversion of the ADC module by toggling the trigger software bit. Note that this will cause the ADC to start conversion regardless if the software bit was set as the trigger using `ADC14_setSampleHoldTrigger`.

**Returns**

false if setting fails due to an in progress conversion

2.6.2.33 `void ADC14_unregisterInterrupt ( void )`

Unregisters the interrupt handler for the ADCC module.

This function unregisters the handler to be called when an ADCC interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 3 Advanced Encryption Standard 256 Module (AES256)

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### 3.1 Module Operation

The AES256 accelerator module performs encryption and decryption of 128-bit data with 128-bit keys according to the advanced encryption standard (AES256) (FIPS PUB 197) in hardware.

### 3.2 Key Features

The key features of the AES256 module include:

- Encryption and decryption according to AES256 FIPS PUB 197 with 128-bit key
- On-the-fly key expansion for encryption and decryption
- Off-line key generation for decryption
- Byte and word access to key, input, and output data
- AES256 ready interrupt flag

The AES256256 accelerator module performs encryption and decryption of 128-bit data with 128-/192-/256-bit keys according to the advanced encryption standard (AES256) (FIPS PUB 197) in hardware.



## 3.3 Encryption/Decryption Cycle Times

The the AES256 accelerator decryption/encryption cycle counts are as follows:

### AES256 encryption

- 128 bit - 168 cycles
- 192 bit - 204 cycles
- 256 bit - 234 cycles

### AES256 decryption:

- 128 bit - 168 cycles
- 192 bit - 206 cycles
- 256 bit - 234 cycles

## 3.4 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the AES256 module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. Below is a simple code example of how to encrypt/decrypt data using a cipher key with the AES256 module

```
/* Load a cipher key to module */
MAP_AES256_setCipherKey(AES256_BASE, CipherKey, AES256_KEYLENGTH_256BIT);

/* Encrypt data with preloaded cipher key */
MAP_AES256_encryptData(AES256_BASE, Data, DataAESencrypted);

/* Load a decipher key to module */
MAP_AES256_setDecipherKey(AES256_BASE, CipherKey, AES256_KEYLENGTH_256BIT);

/* Decrypt data with keys that were generated during encryption - takes
 214 MCLK cyles. This function will generate all round keys needed for
 decryption first and then the encryption process starts */
MAP_AES256_decryptData(AES256_BASE, DataAESencrypted, DataAESdecrypted);
```

## 3.5 Definitions

### Functions

- void [AES256\\_clearErrorFlag](#) (uint32\_t moduleInstance)
- void [AES256\\_clearInterruptFlag](#) (uint32\_t moduleInstance)
- void [AES256\\_decryptData](#) (uint32\_t moduleInstance, const uint8\_t \*data, uint8\_t \*decryptedData)
- void [AES256\\_disableInterrupt](#) (uint32\_t moduleInstance)
- void [AES256\\_enableInterrupt](#) (uint32\_t moduleInstance)
- void [AES256\\_encryptData](#) (uint32\_t moduleInstance, const uint8\_t \*data, uint8\_t \*encryptedData)
- bool [AES256\\_getDataOut](#) (uint32\_t moduleInstance, uint8\_t \*outputData)
- uint32\_t [AES256\\_getErrorFlagStatus](#) (uint32\_t moduleInstance)
- uint32\_t [AES256\\_getInterruptFlagStatus](#) (uint32\_t moduleInstance)
- uint32\_t [AES256\\_getInterruptStatus](#) (uint32\_t moduleInstance)
- bool [AES256\\_isBusy](#) (uint32\_t moduleInstance)
- void [AES256\\_registerInterrupt](#) (uint32\_t moduleInstance, void(\*intHandler)(void))
- void [AES256\\_reset](#) (uint32\_t moduleInstance)
- bool [AES256\\_setCipherKey](#) (uint32\_t moduleInstance, const uint8\_t \*cipherKey, uint\_fast16\_t keyLength)
- bool [AES256\\_setDecipherKey](#) (uint32\_t moduleInstance, const uint8\_t \*cipherKey, uint\_fast16\_t keyLength)
- void [AES256\\_startDecryptData](#) (uint32\_t moduleInstance, const uint8\_t \*data)
- void [AES256\\_startEncryptData](#) (uint32\_t moduleInstance, const uint8\_t \*data)
- bool [AES256\\_startSetDecipherKey](#) (uint32\_t moduleInstance, const uint8\_t \*cipherKey, uint\_fast16\_t keyLength)
- void [AES256\\_unregisterInterrupt](#) (uint32\_t moduleInstance)

### 3.5.1 Detailed Description

The code for this module is contained in `driverlib/aes256.c` and `driverlib/legacy/MSP432xx/legacy_aes256.c`, with `driverlib/aes256.h` and `driverlib/legacy/MSP432xx/legacy_aes256.h` containing the API declarations for use by applications.

## 3.5.2 Function Documentation

### 3.5.2.1 void AES256\_clearErrorFlag ( uint32\_t *moduleInstance* )

Clears the AES256 error flag.

#### Parameters

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

Modified bits are **AESERRFG** of **AESACTL0** register.

#### Returns

None

### 3.5.2.2 void AES256\_clearInterruptFlag ( uint32\_t *moduleInstance* )

Clears the AES256 ready interrupt flag.

#### Parameters

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

Modified bits are **AESRDYIFG** of **AESACTL0** register.

#### Returns

None

### 3.5.2.3 void AES256\_decryptData ( uint32\_t *moduleInstance*, const uint8\_t \* *data*, uint8\_t \* *decryptedData* )

Decrypts a block of data using the AES256 module.

This function requires a pregenerated decryption key. A key can be loaded and pregenerated by using function [AES256\\_setDecipherKey\(\)](#) or [AES256\\_startSetDecipherKey\(\)](#). The decryption takes 167 MCLK.

#### Parameters

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>data</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains encrypted data to be decrypted.
<i>decryptedData</i>	is a pointer to an uint8_t array with a length of 16 bytes in that the decrypted data will be written.

#### Returns

None

### 3.5.2.4 void AES256\_disableInterrupt ( uint32\_t *moduleInstance* )

Disables AES256 ready interrupt.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

Modified bits are **AESRDYIE** of **AESACTL0** register.

**Returns**

None

### 3.5.2.5 void AES256\_enableInterrupt ( uint32\_t *moduleInstance* )

Enables AES256 ready interrupt.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

Modified bits are **AESRDYIE** of **AESACTL0** register.

**Returns**

None

### 3.5.2.6 void AES256\_encryptData ( uint32\_t *moduleInstance*, const uint8\_t \* *data*, uint8\_t \* *encryptedData* )

Encrypts a block of data using the AES256 module.

The cipher key that is used for encryption should be loaded in advance by using function [AES256\\_setCipherKey\(\)](#)

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>data</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains data to be encrypted.
<i>encryptedData</i>	is a pointer to an uint8_t array with a length of 16 bytes in that the encrypted data will be written.

**Returns**

None

### 3.5.2.7 bool AES256\_getDataOut ( uint32\_t *moduleInstance*, uint8\_t \* *outputData* )

Reads back the output data from AES256 module.

This function is meant to use after an encryption or decryption process that was started and finished by initiating an interrupt by use of [AES256\\_startEncryptData](#) or [AES256\\_startDecryptData](#) functions.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>outputData</i>	is a pointer to an uint8_t array with a length of 16 bytes in that the data will be written.

**Returns**

true if data is valid, otherwise false

3.5.2.8 uint32\_t AES256\_getErrorFlagStatus ( uint32\_t *moduleInstance* )

Gets the AES256 error flag status.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

**Returns**

One of the following:

- **AES256\_ERROR\_OCCURRED**
  - **AES256\_NO\_ERROR**
- indicating the error flag status

3.5.2.9 uint32\_t AES256\_getInterruptFlagStatus ( uint32\_t *moduleInstance* )

Gets the AES256 ready interrupt flag status.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

**Returns**

One of the following:

- **AES256\_READY\_INTERRUPT**
  - **AES256\_NOTREADY\_INTERRUPT**
- indicating the status of the AES256 ready status

Referenced by [AES256\\_getInterruptStatus\(\)](#).

3.5.2.10 uint32\_t AES256\_getInterruptStatus ( uint32\_t *moduleInstance* )

Returns the current interrupt flag for the peripheral.

**Parameters**

<i>moduleInstance</i>	Instance of the AES256 module
-----------------------	-------------------------------

**Returns**

The currently triggered interrupt flag for the module.

References [AES256\\_getInterruptFlagStatus\(\)](#).

3.5.2.11 `bool AES256_isBusy ( uint32_t moduleInstance )`

Gets the AES256 module busy status.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

**Returns**

true if busy, false otherwise

3.5.2.12 void AES256\_registerInterrupt ( uint32\_t *moduleInstance*, void(\*)(void) *intHandler* )

Registers an interrupt handler for the AES interrupt.

**Parameters**

<i>moduleInstance</i>	Instance of the AES256 module
<i>intHandler</i>	is a pointer to the function to be called when the AES interrupt occurs.

This function registers the handler to be called when a AES interrupt occurs. This function enables the global interrupt in the interrupt controller; specific AES interrupts must be enabled via [AES256\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [AES256\\_clearInterrupt\(\)](#).

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

3.5.2.13 void AES256\_reset ( uint32\_t *moduleInstance* )

Resets AES256 Module immediately.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
-----------------------	---

Modified bits are **AESSWRST** of **AESACTL0** register.

**Returns**

None

3.5.2.14 bool AES256\_setCipherKey ( uint32\_t *moduleInstance*, const uint8\_t \* *cipherKey*, uint\_fast16\_t *keyLength* )

Loads a 128, 192 or 256 bit cipher key to AES256 module.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>cipherKey</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains a 128 bit cipher key.
<i>keyLength</i>	is the length of the key. Valid values are: <ul style="list-style-type: none"> <li>■ AES256_KEYLENGTH_128BIT</li> <li>■ AES256_KEYLENGTH_192BIT</li> <li>■ AES256_KEYLENGTH_256BIT</li> </ul>

**Returns**

true if set correctly, false otherwise

3.5.2.15 `bool AES256_setDecipherKey ( uint32_t moduleInstance, const uint8_t * cipherKey, uint_fast16_t keyLength )`

Sets the decipher key.

The API `AES256_startSetDecipherKey` or `AES256_setDecipherKey` must be invoked before invoking `AES256_startDecryptData`.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>cipherKey</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains a 128 bit cipher key.
<i>keyLength</i>	is the length of the key. Valid values are: <ul style="list-style-type: none"> <li>■ AES256_KEYLENGTH_128BIT</li> <li>■ AES256_KEYLENGTH_192BIT</li> <li>■ AES256_KEYLENGTH_256BIT</li> </ul>

**Returns**

true if set, false otherwise

3.5.2.16 `void AES256_startDecryptData ( uint32_t moduleInstance, const uint8_t * data )`

Decrypts a block of data using the AES256 module.

This is the non-blocking equivalent of `AES256_decryptData()`. This function requires a pregenerated decryption key. A key can be loaded and pregenerated by using function `AES256_setDecipherKey()` or `AES256_startSetDecipherKey()`. The decryption takes 167 MCLK. It is recommended to use interrupt to check for procedure completion then use the `AES256_getDataOut()` API to retrieve the decrypted data.

**Parameters**



<i>moduleInstance</i>	is the base address of the AES256 module.
<i>data</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains encrypted data to be decrypted.

**Returns**

None

3.5.2.17 void AES256\_startEncryptData ( uint32\_t *moduleInstance*, const uint8\_t \* *data* )

Starts an encryption process on the AES256 module.

The cipher key that is used for decryption should be loaded in advance by using function [AES256\\_setCipherKey\(\)](#). This is a non-blocking equivalent of [AES256\\_encryptData\(\)](#). It is recommended to use the interrupt functionality to check for procedure completion then use the [AES256\\_getDataOut\(\)](#) API to retrieve the encrypted data.

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>data</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains data to be encrypted.

**Returns**

None

3.5.2.18 bool AES256\_startSetDecipherKey ( uint32\_t *moduleInstance*, const uint8\_t \* *cipherKey*, uint\_fast16\_t *keyLength* )

Sets the decipher key.

The API [AES256\\_startSetDecipherKey\(\)](#) or [AES256\\_setDecipherKey\(\)](#) must be invoked before invoking [AES256\\_startDecryptData\(\)](#).

**Parameters**

<i>moduleInstance</i>	is the base address of the AES256 module.
<i>cipherKey</i>	is a pointer to an uint8_t array with a length of 16 bytes that contains a 128 bit cipher key.
<i>keyLength</i>	is the length of the key. Valid values are: <ul style="list-style-type: none"> <li>■ AES256_KEYLENGTH_128BIT</li> <li>■ AES256_KEYLENGTH_192BIT</li> <li>■ AES256_KEYLENGTH_256BIT</li> </ul>

**Returns**

true if set correctly, false otherwise

3.5.2.19 void AES256\_unregisterInterrupt ( uint32\_t *moduleInstance* )

Unregisters the interrupt handler for the AES interrupt

**Parameters**

<i>moduleInstance</i>	Instance of the AES256 module
-----------------------	-------------------------------

This function unregisters the handler to be called when AES interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 4 Analog Comparator (COMP\_E)

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### 4.1 Module Operation

The Comparator (Comp) API provides a set of functions for using the MSPWare COMP\_E modules. Functions are provided to initialize the COMP\_E modules, setup reference voltages for input, and manage interrupts for the COMP\_E modules.

The COMP\_E module provides the ability to compare two analog signals and use the output in software and on an output pin. The output represents whether the signal on the positive terminal is higher than the signal on the negative terminal. The COMP\_E module may be used to generate a hysteresis. There are 16 different inputs that can be used, as well as the ability to short 2 input together. The COMP\_E module also has control over the REF\_A module to generate a reference voltage as an input.

The COMP\_E module can generate multiple interrupts. An interrupt may be asserted for the output, with separate interrupts on whether the output rises, or falls.

## 4.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the COMP\_E module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a simple example of how to setup the COMP\_E module to setup a comparator window with a Vcompare of 1.2v using the internal reference.

First, below is an example of setting up the COMP\_E module configuration structure:

```
/* Comparator configuration structure */
const COMP_E_Config compConfig =
{
    COMP_E_VREF,                // Positive Input Terminal
    COMP_E_INPUT7,              // Negative Input Terminal
    COMP_E_FILTEROUTPUT_DLYLVL4, // Delay Level 4 Filter
    COMP_E_NORMALOUTPUTPOLARITY // Normal Output Polarity
};
```

Below are the actual DriverLib calls to configure/setup the Comp module:

## 4.3 Definitions

### Data Structures

- struct `_COMP_E_Config`

### Functions

- void `COMP_E_clearInterruptFlag` (uint32\_t comparator, uint\_fast16\_t mask)
- void `COMP_E_disableInputBuffer` (uint32\_t comparator, uint\_fast16\_t inputPort)
- void `COMP_E_disableInterrupt` (uint32\_t comparator, uint\_fast16\_t mask)
- void `COMP_E_disableModule` (uint32\_t comparator)
- void `COMP_E_enableInputBuffer` (uint32\_t comparator, uint\_fast16\_t inputPort)
- void `COMP_E_enableInterrupt` (uint32\_t comparator, uint\_fast16\_t mask)
- void `COMP_E_enableModule` (uint32\_t comparator)
- uint\_fast16\_t `COMP_E_getEnabledInterruptStatus` (uint32\_t comparator)
- uint\_fast16\_t `COMP_E_getInterruptStatus` (uint32\_t comparator)
- bool `COMP_E_initModule` (uint32\_t comparator, const `COMP_E_Config` \*config)
- uint8\_t `COMP_E_outputValue` (uint32\_t comparator)
- void `COMP_E_registerInterrupt` (uint32\_t comparator, void(\*intHandler)(void))
- void `COMP_E_setInterruptEdgeDirection` (uint32\_t comparator, uint\_fast8\_t edgeDirection)
- void `COMP_E_setPowerMode` (uint32\_t comparator, uint\_fast16\_t powerMode)
- void `COMP_E_setReferenceAccuracy` (uint32\_t comparator, uint\_fast16\_t referenceAccuracy)
- void `COMP_E_setReferenceVoltage` (uint32\_t comparator, uint\_fast16\_t supplyVoltageReferenceBase, uint\_fast16\_t lowerLimitSupplyVoltageFractionOf32, uint\_fast16\_t upperLimitSupplyVoltageFractionOf32)
- void `COMP_E_shortInputs` (uint32\_t comparator)
- void `COMP_E_swapIO` (uint32\_t comparator)
- void `COMP_E_toggleInterruptEdgeDirection` (uint32\_t comparator)
- void `COMP_E_unregisterInterrupt` (uint32\_t comparator)
- void `COMP_E_unshortInputs` (uint32\_t comparator)

### 4.3.1 Detailed Description

The code for this module is contained in `driverlib/comp_e.c`, with `driverlib/comp_e.h` containing the API declarations for use by applications.

## 4.3.2 Function Documentation

### 4.3.2.1 void COMP\_E\_clearInterruptFlag ( uint32\_t *comparator*, uint\_fast16\_t *mask* )

Clears Comparator interrupt flags.

#### Parameters

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>mask</i>	is a bit mask of the interrupt sources to be cleared. Mask value is the logical OR of any of the following <ul style="list-style-type: none"> <li>■ <b>COMP_E_INTERRUPT_FLAG</b> - Output interrupt flag</li> <li>■ <b>COMP_E_INTERRUPT_FLAG_INVERTED_POLARITY</b> - Output interrupt flag inverted polarity</li> <li>■ <b>COMP_E_INTERRUPT_FLAG_READY</b> - Ready interrupt flag</li> </ul>

The Comparator interrupt source is cleared, so that it no longer asserts. The highest interrupt flag is automatically cleared when an interrupt vector generator is used.

#### Returns

NONE

### 4.3.2.2 void COMP\_E\_disableInputBuffer ( uint32\_t *comparator*, uint\_fast16\_t *inputPort* )

Disables the input buffer of the selected input port to effectively allow for analog signals.

## Parameters

<i>comparator</i>	<p>is the instance of the Comparator module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>inputPort</i>	<p>is the port in which the input buffer will be disabled. Valid values are a logical OR of the following:</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E_INPUT0</b> [Default]</li> <li>■ <b>COMP_E_INPUT1</b></li> <li>■ <b>COMP_E_INPUT2</b></li> <li>■ <b>COMP_E_INPUT3</b></li> <li>■ <b>COMP_E_INPUT4</b></li> <li>■ <b>COMP_E_INPUT5</b></li> <li>■ <b>COMP_E_INPUT6</b></li> <li>■ <b>COMP_E_INPUT7</b></li> <li>■ <b>COMP_E_INPUT8</b></li> <li>■ <b>COMP_E_INPUT9</b></li> <li>■ <b>COMP_E_INPUT10</b></li> <li>■ <b>COMP_E_INPUT11</b></li> <li>■ <b>COMP_E_INPUT12</b></li> <li>■ <b>COMP_E_INPUT13</b></li> <li>■ <b>COMP_E_INPUT14</b></li> <li>■ <b>COMP_E_INPUT15</b></li> </ul> <p>Modified bits are <b>CEPDx</b> of <b>CECTL3</b> register.</p>

This function sets the bit to disable the buffer for the specified input port to allow for analog signals from any of the comparator input pins. This bit is automatically set when the input is initialized to be used with the comparator module. This function should be used whenever an analog input is connected to one of these pins to prevent parasitic voltage from causing unexpected results.

**Returns**  
NONE

4.3.2.3 void COMP\_E\_disableInterrupt ( uint32\_t *comparator*, uint\_fast16\_t *mask* )

Disables selected Comparator interrupt sources.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>mask</i>	is the bit mask of the interrupt sources to be disabled. Mask value is the logical OR of any of the following <ul style="list-style-type: none"> <li>■ <b>COMP_E_OUTPUT_INTERRUPT</b> - Output interrupt</li> <li>■ <b>COMP_E_INVERTED_POLARITY_INTERRUPT</b> - Output interrupt inverted polarity</li> <li>■ <b>COMP_E_READY_INTERRUPT</b> - Ready interrupt</li> </ul>

Disables the indicated Comparator interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Returns**  
NONE

4.3.2.4 void COMP\_E\_disableModule ( uint32\_t *comparator* )

Turns off the Comparator module.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function clears the CEON bit disabling the operation of the Comparator module, saving from excess power consumption.

Modified bits are **CEON** of **CECTL1** register.



**Returns**  
NONE

4.3.2.5 void COMP\_E\_enableInputBuffer ( uint32\_t *comparator*, uint\_fast16\_t *inputPort* )

Enables the input buffer of the selected input port to allow for digital signals.

## Parameters

<i>comparator</i>	<p>is the instance of the Comparator module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>inputPort</i>	<p>is the port in which the input buffer will be enabled. Valid values are a logical OR of the following:</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E_INPUT0</b> [Default]</li> <li>■ <b>COMP_E_INPUT1</b></li> <li>■ <b>COMP_E_INPUT2</b></li> <li>■ <b>COMP_E_INPUT3</b></li> <li>■ <b>COMP_E_INPUT4</b></li> <li>■ <b>COMP_E_INPUT5</b></li> <li>■ <b>COMP_E_INPUT6</b></li> <li>■ <b>COMP_E_INPUT7</b></li> <li>■ <b>COMP_E_INPUT8</b></li> <li>■ <b>COMP_E_INPUT9</b></li> <li>■ <b>COMP_E_INPUT10</b></li> <li>■ <b>COMP_E_INPUT11</b></li> <li>■ <b>COMP_E_INPUT12</b></li> <li>■ <b>COMP_E_INPUT13</b></li> <li>■ <b>COMP_E_INPUT14</b></li> <li>■ <b>COMP_E_INPUT15</b></li> </ul> <p>Modified bits are <b>CEPDx</b> of <b>CECTL3</b> register.</p>

This function clears the bit to enable the buffer for the specified input port to allow for digital signals from any of the comparator input pins. This should not be reset if there is an analog signal connected to the specified input pin to prevent from unexpected results.

**Returns**  
NONE

4.3.2.6 void COMP\_E\_enableInterrupt ( uint32\_t *comparator*, uint\_fast16\_t *mask* )

Enables selected Comparator interrupt sources.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>mask</i>	is the bit mask of the interrupt sources to be enabled. Mask value is the logical OR of any of the following <ul style="list-style-type: none"> <li>■ <b>COMP_E_OUTPUT_INTERRUPT</b> - Output interrupt</li> <li>■ <b>COMP_E_INVERTED_POLARITY_INTERRUPT</b> - Output interrupt inverted polarity</li> <li>■ <b>COMP_E_READY_INTERRUPT</b> - Ready interrupt</li> </ul>

Enables the indicated Comparator interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. The default trigger for the non-inverted interrupt is a rising edge of the output, this can be changed with the interruptSetEdgeDirection() function.

**Returns**  
NONE

4.3.2.7 void COMP\_E\_enableModule ( uint32\_t *comparator* )

Turns on the Comparator module.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function sets the bit that enables the operation of the Comparator module.

**Returns**  
NONE

#### 4.3.2.8 uint\_fast16\_t COMP\_E\_getEnabledInterruptStatus ( uint32\_t *comparator* )

Enables selected Comparator interrupt sources masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

Enables the indicated Comparator interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. The default trigger for the non-inverted interrupt is a rising edge of the output, this can be changed with the [COMP\\_E\\_setInterruptEdgeDirection\(\)](#) function.

**Returns**  
NONE

References [COMP\\_E\\_getInterruptStatus\(\)](#).

#### 4.3.2.9 uint\_fast16\_t COMP\_E\_getInterruptStatus ( uint32\_t *comparator* )

Gets the current Comparator interrupt status.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This returns the interrupt status for the Comparator module based on which flag is passed.

**Returns**  
The current interrupt flag status for the corresponding mask.

Referenced by [COMP\\_E\\_getEnabledInterruptStatus\(\)](#).

#### 4.3.2.10 bool COMP\_E\_initModule ( uint32\_t *comparator*, const **COMP\_E\_Config** \* *config* )

Initializes the Comparator Module.

## Parameters

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>config</i>	Configuration structure for the Comparator module

## Configuration options for COMP\_E\_Config structure.

## Parameters

<i>positiveTerminalInput</i>	selects the input to the positive terminal. Valid values are <ul style="list-style-type: none"> <li>■ <b>COMP_E_INPUT0</b> [Default]</li> <li>■ <b>COMP_E_INPUT1</b></li> <li>■ <b>COMP_E_INPUT2</b></li> <li>■ <b>COMP_E_INPUT3</b></li> <li>■ <b>COMP_E_INPUT4</b></li> <li>■ <b>COMP_E_INPUT5</b></li> <li>■ <b>COMP_E_INPUT6</b></li> <li>■ <b>COMP_E_INPUT7</b></li> <li>■ <b>COMP_E_INPUT8</b></li> <li>■ <b>COMP_E_INPUT9</b></li> <li>■ <b>COMP_E_INPUT10</b></li> <li>■ <b>COMP_E_INPUT11</b></li> <li>■ <b>COMP_E_INPUT12</b></li> <li>■ <b>COMP_E_INPUT13</b></li> <li>■ <b>COMP_E_INPUT14</b></li> <li>■ <b>COMP_E_INPUT15</b></li> <li>■ <b>COMP_E_VREF</b></li> </ul> <p>Modified bits are <b>CEIPSEL</b> and <b>CEIPEN</b> of <b>CECTL0</b> register, <b>CERSEL</b> of <b>CECTL2</b> register, and <b>CEPDx</b> of <b>CECTL3</b> register.</p>
------------------------------	---

<i>negativeTerminalInput</i>	<p>selects the input to the negative terminal. Valid values are:</p> <ul style="list-style-type: none"><li>■ <b>COMP_E_INPUT0</b> [Default]</li><li>■ <b>COMP_E_INPUT1</b></li><li>■ <b>COMP_E_INPUT2</b></li><li>■ <b>COMP_E_INPUT3</b></li><li>■ <b>COMP_E_INPUT4</b></li><li>■ <b>COMP_E_INPUT5</b></li><li>■ <b>COMP_E_INPUT6</b></li><li>■ <b>COMP_E_INPUT7</b></li><li>■ <b>COMP_E_INPUT8</b></li><li>■ <b>COMP_E_INPUT9</b></li><li>■ <b>COMP_E_INPUT10</b></li><li>■ <b>COMP_E_INPUT11</b></li><li>■ <b>COMP_E_INPUT12</b></li><li>■ <b>COMP_E_INPUT13</b></li><li>■ <b>COMP_E_INPUT14</b></li><li>■ <b>COMP_E_INPUT15</b></li><li>■ <b>COMP_E_VREF</b></li></ul> <p>Modified bits are <b>CEIMSEL</b> and <b>CEIMEN</b> of <b>CECTL0</b> register, <b>CERSEL</b> of <b>CECTL2</b> register, and <b>CEPDx</b> of <b>CECTL3</b> register.</p>
------------------------------	---

<p><i>outputFilterEnableAndDelayLevel</i></p>	<p>controls the output filter delay state, which is either off or enabled with a specified delay level. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E_FILTEROUTPUT_OFF</b> [Default]</li> <li>■ <b>COMP_E_FILTEROUTPUT_DLYLVL1</b></li> <li>■ <b>COMP_E_FILTEROUTPUT_DLYLVL2</b></li> <li>■ <b>COMP_E_FILTEROUTPUT_DLYLVL3</b></li> <li>■ <b>COMP_E_FILTEROUTPUT_DLYLVL4</b></li> </ul> <p>This parameter is device specific and delay levels should be found in the device's datasheet. Modified bits are <b>CEF</b> and <b>CEFDLY</b> of <b>CECTL1</b> register.</p>
<p><i>invertedOutputPolarity</i></p>	<p>controls if the output will be inverted or not. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E_NORMALOUTPUTPOLARITY</b> - indicates the output should be normal. [Default]</li> <li>■ <b>COMP_E_INVERTEDOUTPUTPOLARITY</b> - the output should be inverted.</li> </ul> <p>Modified bits are <b>CEOUTPOL</b> of <b>CECTL1</b> register.</p>
<p><i>powerMode</i></p>	<p>controls the power mode of the module</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E_HIGH_SPEED_MODE</b> [default]</li> <li>■ <b>COMP_E_NORMAL_MODE</b></li> <li>■ <b>COMP_E_ULTRA_LOW_POWER_MODE</b> Upon successful initialization of the Comparator module, this function will have reset all necessary register bits and set the given options in the registers. To actually use the comparator module, the <a href="#">COMP_E_enableModule()</a> function must be explicitly called before use. If a Reference Voltage is set to a terminal, the Voltage should be set using the <a href="#">COMP_E_setReferenceVoltage()</a> function.</li> </ul>

**Returns**

true or false of the initialization process.

4.3.2.11 `uint8_t COMP_E_outputValue ( uint32_t comparator )`

Returns the output value of the Comparator module.

**Parameters**

<p><i>comparator</i></p>	<p>is the instance of the Comparator module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
--------------------------	---

Returns the output value of the Comparator module.

**Returns**

COMP\_E\_HIGH or COMP\_E\_LOW as the output value of the Comparator module.

#### 4.3.2.12 void COMP\_E\_registerInterrupt ( uint32\_t *comparator*, void(\*)(void) *intHandler* )

Registers an interrupt handler for the Comparator E interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the Comparator interrupt occurs.
<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>

This function registers the handler to be called when a Comparator interrupt occurs. This function enables the global interrupt in the interrupt controller; specific Comparator interrupts must be enabled via [COMP\\_E\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [COMP\\_E\\_clearInterruptFlag\(\)](#).

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

#### 4.3.2.13 void COMP\_E\_setInterruptEdgeDirection ( uint32\_t *comparator*, uint\_fast8\_t *edgeDirection* )

Explicitly sets the edge direction that would trigger an interrupt.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>edgeDirection</i>	determines which direction the edge would have to go to generate an interrupt based on the non-inverted interrupt flag. Valid values are <ul style="list-style-type: none"> <li>■ <b>COMP_E_FALLINGEDGE</b> - sets the bit to generate an interrupt when the output of the comparator falls from HIGH to LOW if the normal interrupt bit is set(and LOW to HIGH if the inverted interrupt enable bit is set). [Default]</li> <li>■ <b>COMP_E_RISINGEDGE</b> - sets the bit to generate an interrupt when the output of the comparator rises from LOW to HIGH if the normal interrupt bit is set(and HIGH to LOW if the inverted interrupt enable bit is set).</li> </ul> Modified bits are <b>CEIES</b> of <b>CECTL1</b> register.

This function will set which direction the output will have to go, whether rising or falling, to generate an interrupt based on a non-inverted interrupt.



**Returns**  
NONE

4.3.2.14 void COMP\_E\_setPowerMode ( uint32\_t *comparator*, uint\_fast16\_t *powerMode* )

Sets the power mode

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>powerMode</i>	decides the power mode Valid values are <ul style="list-style-type: none"> <li>■ <b>COMP_E_HIGH_SPEED_MODE</b></li> <li>■ <b>COMP_E_NORMAL_MODE</b></li> <li>■ <b>COMP_E_ULTRA_LOW_POWER_MODE</b></li> </ul> Modified bits are <b>CEPWRMD</b> of <b>CECTL1</b> register.

**Returns**  
NONE

4.3.2.15 void COMP\_E\_setReferenceAccuracy ( uint32\_t *comparator*, uint\_fast16\_t *referenceAccuracy* )

Sets the reference accuracy

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>referenceAccuracy</i>	is the reference accuracy setting of the comparator. Clocked is for low power/low accuracy. Valid values are <ul style="list-style-type: none"> <li>■ <b>COMP_E_ACCURACY_STATIC</b></li> <li>■ <b>COMP_E_ACCURACY_CLOCKED</b></li> </ul> Modified bits are <b>CEREFACC</b> of <b>CECTL2</b> register.

The reference accuracy is set to the desired setting. Clocked is better for low power operations but has a lower accuracy.

**Returns**

NONE

4.3.2.16 void COMP\_E\_setReferenceVoltage ( uint32\_t *comparator*, uint\_fast16\_t *supplyVoltageReferenceBase*, uint\_fast16\_t *lowerLimitSupplyVoltageFractionOf32*, uint\_fast16\_t *upperLimitSupplyVoltageFractionOf32* )

Generates a Reference Voltage to the terminal selected during initialization.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
<i>supplyVoltageReferenceBase</i>	decides the source and max amount of Voltage that can be used as a reference. Valid values are <ul style="list-style-type: none"> <li>■ <b>COMP_E_REFERENCE_AMPLIFIER_DISABLED</b></li> <li>■ <b>COMP_E_VREFBASE1_2V</b></li> <li>■ <b>COMP_E_VREFBASE2_0V</b></li> <li>■ <b>COMP_E_VREFBASE2_5V</b></li> </ul>
<i>upperLimitSupplyVoltageFractionOf32</i>	is the numerator of the equation to generate the reference voltage for the upper limit reference voltage. Valid values are between 0 and 32.
<i>lowerLimitSupplyVoltageFractionOf32</i>	is the numerator of the equation to generate the reference voltage for the lower limit reference voltage. Valid values are between 0 and 32. Modified bits are <b>CEREF0</b> of <b>CECTL2</b> register.

Use this function to generate a voltage to serve as a reference to the terminal selected at initialization. The voltage is determined by the equation:  $V_{base} * (\text{Numerator} / 32)$ . If the upper and lower limit voltage numerators are equal, then a static reference is defined, whereas they are different then a hysteresis effect is generated.

**Returns**

NONE

4.3.2.17 void COMP\_E\_shortInputs ( uint32\_t *comparator* )

Shorts the two input pins chosen during initialization.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function sets the bit that shorts the devices attached to the input pins chosen from the initialization of the comparator.

Modified bits are **CESHORT** of **CECTL1** register.

**Returns**

NONE

#### 4.3.2.18 void COMP\_E\_swapIO ( uint32\_t *comparator* )

Toggles the bit that swaps which terminals the inputs go to, while also inverting the output of the comparator.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ \ bCOMP_E0</li> <li>■ \ bCOMP_E1</li> </ul>
-------------------	--

This function toggles the bit that controls which input goes to which terminal. After initialization, this bit is set to 0, after toggling it once the inputs are routed to the opposite terminal and the output is inverted.

Modified bits are **CEEX** of **CECTL1** register.

**Returns**

NONE

#### 4.3.2.19 void COMP\_E\_toggleInterruptEdgeDirection ( uint32\_t *comparator* )

Toggles the edge direction that would trigger an interrupt.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function will toggle which direction the output will have to go, whether rising or falling, to generate an interrupt based on a non-inverted interrupt. If the direction was rising, it is now falling, if it was falling, it is now rising.

Modified bits are **CEIES** of **CECTL1** register.

**Returns**  
NONE

#### 4.3.2.20 void COMP\_E\_unregisterInterrupt ( uint32\_t *comparator* )

Unregisters the interrupt handler for the Comparator E interrupt

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function unregisters the handler to be called when Comparator E interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**  
None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

#### 4.3.2.21 void COMP\_E\_unshortInputs ( uint32\_t *comparator* )

Disables the short of the two input pins chosen during initialization.

**Parameters**

<i>comparator</i>	is the instance of the Comparator module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>COMP_E0_BASE</b></li> <li>■ <b>COMP_E1_BASE</b></li> </ul>
-------------------	--

This function clears the bit that shorts the devices attached to the input pins chosen from the initialization of the comparator.

Modified bits are **CESHORT** of **CECTL1** register.

**Returns**  
NONE

## 5 Cyclic Redundancy Check 32 (CRC32)

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### 5.1 Module Operation

The Cyclic Redundancy Check 32 (CRC32) API provides a set of functions for using the MSPWare CRC32 module. Functions are provided to initialize the CRC and create a CRC signature to check the validity of data. This is mostly useful in the communication of data, or as a startup procedure to as a more complex and accurate check of data.

The CRC32 module offers no interrupts and is used only to generate CRC signatures to verify against pre-made CRC signatures (Checksums).

The CRC32 module provides the capability for both 32-bit and 16-bit calculations. As such, the DriverLib API provides functionality for the user to provide variable bit-length data for either 16-bit or 32-bit calculations.

### 5.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the CRC32 module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

In the following very simple code example, an array of data is fed into the CRC32 module and the 32-bit calculation is retrieved:

## 5.3 Definitions

### Functions

- `uint32_t CRC32_getResult` (`uint_fast8_t crcType`)
- `uint32_t CRC32_getResultReversed` (`uint_fast8_t crcType`)
- `void CRC32_set16BitData` (`uint16_t dataIn, uint_fast8_t crcType`)
- `void CRC32_set16BitDataReversed` (`uint16_t dataIn, uint_fast8_t crcType`)
- `void CRC32_set32BitData` (`uint32_t dataIn`)
- `void CRC32_set32BitDataReversed` (`uint32_t dataIn`)
- `void CRC32_set8BitData` (`uint8_t dataIn, uint_fast8_t crcType`)
- `void CRC32_set8BitDataReversed` (`uint8_t dataIn, uint_fast8_t crcType`)
- `void CRC32_setSeed` (`uint32_t seed, uint_fast8_t crcType`)

### 5.3.1 Detailed Description

The code for this module is contained in `driverlib/crc32.c` and `driverlib/legacy/MSP432xx/legacy_crc32.c`, with `driverlib/crc32.h` and `driverlib/legacy/MSP432xx/legacy_crc32.h` containing the API declarations for use by applications.

## 5.3.2 Function Documentation

### 5.3.2.1 uint32\_t CRC32\_getResult ( uint\_fast8\_t *crcType* )

Returns the value of CRC Signature Result.

#### Parameters

<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>
----------------	--

This function returns the value of the signature result generated by the CRC. Bit 0 is treated as LSB.

#### Returns

uint32\_t Result

### 5.3.2.2 uint32\_t CRC32\_getResultReversed ( uint\_fast8\_t *crcType* )

Returns the bit-wise reversed format of the 32 bit Signature Result.

#### Parameters

<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>
----------------	--

This function returns the bit-wise reversed format of the Signature Result. Bit 0 is treated as MSB.

#### Returns

uint32\_t Result

### 5.3.2.3 void CRC32\_set16BitData ( uint16\_t *dataIn*, uint\_fast8\_t *crcType* )

Sets the 16 Bit data to add into the CRC module to generate a new signature.

#### Parameters

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC16DIW0</b> of <b>CRC16DIW0</b> register. <b>CRC32DIW0</b> of <b>CRC32DIW0</b> register.
<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>

This function sets the given data into the CRC module to generate the new signature from the current signature and new data. Bit 0 is treated as LSB

#### Returns

NONE

### 5.3.2.4 void CRC32\_set16BitDataReversed ( uint16\_t *dataIn*, uint\_fast8\_t *crcType* )

Translates the data by reversing the bits in each 16 bit data and then sets this data to add into the CRC module to generate a new signature.

**Parameters**

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC16DIRBW0</b> of <b>CRC16DIRBW0</b> register. <b>CRC32DIRBW0</b> of <b>CRC32DIRBW0</b> register.
<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>

This function first reverses the bits in each byte of the data and then generates the new signature from the current signature and new translated data. Bit 0 is treated as MSB.

**Returns**

NONE

5.3.2.5 void CRC32\_set32BitData ( uint32\_t *dataIn* )

Sets the 32 Bit data to add into the CRC module to generate a new signature. Available only for CRC32\_MODE and not for CRC16\_MODE

**Parameters**

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC32DIL0</b> of <b>CRC32DIL0</b> register.
---------------	---

This function sets the given data into the CRC module to generate the new signature from the current signature and new data. Bit 0 is treated as LSB

**Returns**

NONE

5.3.2.6 void CRC32\_set32BitDataReversed ( uint32\_t *dataIn* )

Translates the data by reversing the bits in each 32 Bit Data and then sets this data to add into the CRC module to generate a new signature. Available only for CRC32 mode and not for CRC16 mode

**Parameters**

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC32DIRBLO</b> of <b>CRC32DIRBLO</b> register.
---------------	---

This function first reverses the bits in each byte of the data and then generates the new signature from the current signature and new translated data. Bit 0 is treated as MSB.

**Returns**

NONE

5.3.2.7 void CRC32\_set8BitData ( uint8\_t *dataIn*, uint\_fast8\_t *crcType* )

Sets the 8 Bit data to add into the CRC module to generate a new signature.



**Parameters**

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC16DIB0</b> of <b>CRC16DIB0</b> register. <b>CRC32DIB0</b> of <b>CRC32DIB0</b> register.
<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>

This function sets the given data into the CRC module to generate the new signature from the current signature and new data. Bit 0 is treated as LSB.

**Returns**

NONE

5.3.2.8 void CRC32\_set8BitDataReversed ( uint8\_t *dataIn*, uint\_fast8\_t *crcType* )

Translates the data by reversing the bits in each 8 bit data and then sets this data to add into the CRC module to generate a new signature.

**Parameters**

<i>dataIn</i>	is the data to be added, through the CRC module, to the signature. Modified bits are <b>CRC16DIRBB0</b> of <b>CRC16DIRBB0</b> register. <b>CRC32DIRBB0</b> of <b>CRC32DIRBB0</b> register.
<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>

This function first reverses the bits in each byte of the data and then generates the new signature from the current signature and new translated data. Bit 0 is treated as MSB.

**Returns**

NONE

5.3.2.9 void CRC32\_setSeed ( uint32\_t *seed*, uint\_fast8\_t *crcType* )

Sets the seed for the CRC.

**Parameters**

<i>seed</i>	is the seed for the CRC to start generating a signature from. Modified bits are <b>CRC16INIRESL0</b> of <b>CRC16INIRESL0</b> register. <b>CRC32INIRESL0</b> of <b>CRC32INIRESL0</b> register
<i>crcType</i>	selects between CRC32 and CRC16 Valid values are <b>CRC16_MODE</b> and <b>CRC32_MODE</b>

This function sets the seed for the CRC to begin generating a signature with the given seed and all passed data. Using this function resets the CRC32 signature.

**Returns**

NONE

## 6 Clock System (CS)

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### 6.1 Module Operation

The clock system module for DriverLib gives users the ability to fully configure and control all aspects of the MSP432 clock system. This includes initializing and maintaining the MCLK, ACLK, HSMCLK, SMCLK, and BCLK clock systems. Additionally, APIs exist for configuring connected crystal oscillators as well as configuring/manipulating the DCO and reference oscillator.

### 6.2 Timeout Parameters

For crystal configuration APIs (starting the LFXT and HFXT), a "timeout" API exists that will return control of execution back to the user application if a specified duration passes. The variable that is passed into these functions is a unit of time specified by how many "loop iterations" elapse before unsuccessful stabilization of the respected crystal. The API will attempt to check to see if there was a crystal fault, clear the crystal fault flag, and repeat the check until no fault exists. If the user calls the API with a specified timeout, the loop will only check the given number of loop iterations for a successfully stabilized crystal.

### 6.3 Custom DCO Frequency

For tuning the DCO frequency to a specific frequency, a convenient `CS_setDCOFrequency` function is provided to users. This function accepts any `uint32_t` frequency and automatically calculates the appropriate tuning parameters to get the DCO frequency as close as possible to the provided frequency. Note that with this function, floating point math is involved so if efficiency is a concern the user should enable the FPU using the `FPU_enableModule` function.

### 6.4 Specifying External Crystal Frequencies

MSP432 DriverLib has a variety of convenience functions for obtaining the specific frequency of a clock source ( such as `CS_getMCLK` ). If a clock source is sourced from an external crystal, the crystal frequency must be specified explicitly using the `CS_setExternalClockSourceFrequency` function. This function must be used prior to the getters for the clock source if an external crystal is used.

## 6.5 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the CS module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to start the external high frequency crystal and source MCLK from this crystal. An LED is configured as an output in this example as well. For a set of more detailed code examples, please refer to the code examples in the examples/ directory of the MSPWare release:

```
/* Configuring pins for peripheral/crystal usage and LED for output */
MAP_GPIO_setAsPeripheralModuleFunctionOutputPin(GPIO_PORT_PJ,
        GPIO_PIN3 | GPIO_PIN2,  GPIO_PRIMARY_MODULE_FUNCTION);
MAP_GPIO_setAsOutputPin(GPIO_PORT_P1,  GPIO_PIN0);

/* Just in case the user wants to use the getACLK,  getMCLK,  etc. functions,
 * let's set the clock frequency in the code.
 */
CS_setExternalClockSourceFrequency(32000, 48000000);

/* Starting HFXT in non-bypass mode without a timeout. Before we start
 * we have to change VCORE to 1 to support the 48MHz frequency */
MAP_PCM_setCoreVoltageLevel(PCM_VCORE1);
MAP_FlashCtl_setWaitState(FLASH_BANK0,  2);
MAP_FlashCtl_setWaitState(FLASH_BANK1,  2);
CS_startHFXT(false);

/* Initializing MCLK to HFXT (effectively 48MHz) */
MAP_CS_initClockSignal(CS_MCLK,  CS_HFXTCLK_SELECT,  CS_CLOCK_DIVIDER_1);
```

## 6.6 Definitions

### Functions

- void `CS_clearInterruptFlag` (uint32\_t flags)
- void `CS_disableClockRequest` (uint32\_t selectClock)
- void `CS_disableDCOExternalResistor` (void)
- void `CS_disableFaultCounter` (uint\_fast8\_t counterSelect)
- void `CS_disableInterrupt` (uint32\_t flags)
- void `CS_enableClockRequest` (uint32\_t selectClock)
- void `CS_enableDCOExternalResistor` (void)
- void `CS_enableFaultCounter` (uint\_fast8\_t counterSelect)
- void `CS_enableInterrupt` (uint32\_t flags)
- uint32\_t `CS_getACLK` (void)
- uint32\_t `CS_getBCLK` (void)
- uint32\_t `CS_getDCOFrequency` (void)
- uint32\_t `CS_getEnabledInterruptStatus` (void)
- uint32\_t `CS_getHSMCLK` (void)
- uint32\_t `CS_getInterruptStatus` (void)
- uint32\_t `CS_getMCLK` (void)
- uint32\_t `CS_getSMCLK` (void)
- void `CS_initClockSignal` (uint32\_t selectedClockSignal, uint32\_t clockSource, uint32\_t clockSourceDivider)
- void `CS_registerInterrupt` (void(\*intHandler)(void))
- void `CS_resetFaultCounter` (uint\_fast8\_t counterSelect)
- void `CS_setDCOCenteredFrequency` (uint32\_t dcoFreq)
- void `CS_setDCOExternalResistorCalibration` (uint\_fast8\_t uiCalData, uint\_fast8\_t freqRange)
- void `CS_setDCOFrequency` (uint32\_t dcoFrequency)
- void `CS_setExternalClockSourceFrequency` (uint32\_t lfxt\_XT\_CLK\_frequency, uint32\_t hfxt\_XT\_CLK\_frequency)
- void `CS_setReferenceOscillatorFrequency` (uint8\_t referenceFrequency)
- void `CS_startFaultCounter` (uint\_fast8\_t counterSelect, uint\_fast8\_t countValue)
- bool `CS_startHFXT` (bool bypassMode)
- bool `CS_startHFXTWithTimeout` (bool bypassMode, uint32\_t timeout)
- bool `CS_startLFXT` (uint32\_t xtDrive)
- bool `CS_startLFXTWithTimeout` (uint32\_t xtDrive, uint32\_t timeout)
- void `CS_tuneDCOFrequency` (int16\_t tuneParameter)
- void `CS_unregisterInterrupt` (void)

### 6.6.1 Detailed Description

The code for this module is contained in `driverlib/cs.c`, with `driverlib/cs.h` containing the API declarations for use by applications.

## 6.6.2 Function Documentation

### 6.6.2.1 void CS\_clearInterruptFlag ( uint32\_t flags )

Clears clock system interrupt sources.

#### Parameters

<i>flags</i>	is a bit mask of the interrupt sources to be cleared. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ CS_LFXT_FAULT,</li> <li>■ CS_HFXT_FAULT,</li> <li>■ CS_DCO_OPEN_FAULT,</li> <li>■ CS_STARTCOUNT_LFXT_FAULT,</li> <li>■ CS_STARTCOUNT_HFXT_FAULT,</li> </ul>
--------------	---

The specified clock system interrupt sources are cleared, so that they no longer assert. This function must be called in the interrupt handler to keep it from being called again immediately upon exit.

#### Note

Because there is a write buffer in the Cortex-M processor, it may take several clock cycles before the interrupt source is actually cleared. Therefore, it is recommended that the interrupt source be cleared early in the interrupt handler (as opposed to the very last action) to avoid returning from the interrupt handler before the interrupt source is actually cleared. Failure to do so may result in the interrupt handler being immediately reentered (because the interrupt controller still sees the interrupt source asserted).

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

#### Returns

None.

### 6.6.2.2 void CS\_disableClockRequest ( uint32\_t selectClock )

Disables conditional module requests

#### Parameters

<i>selectClock</i>	selects specific request disables. Valid values are are a logical OR of the following values: <ul style="list-style-type: none"> <li>■ CS_ACLK,</li> <li>■ CS_HSMCLK,</li> <li>■ CS_SMCLK,</li> <li>■ CS_MCLK</li> </ul>
--------------------	--

#### Returns

NONE

## 6.6.2.3 void CS\_disableDCOExternalResistor ( void )

Disables the external resistor for DCO operation

**Returns**

NONE

## 6.6.2.4 void CS\_disableFaultCounter ( uint\_fast8\_t counterSelect )

Disables the fault counter for the CS module. This function can disable either the HFXT fault counter or the LFXT fault counter.

**Parameters**

<i>counterSelect</i>	selects the fault counter to disable <ul style="list-style-type: none"> <li>■ CS_HFXT_FAULT_COUNTER</li> <li>■ CS_LFXT_FAULT_COUNTER</li> </ul>
----------------------	---

**Returns**

NONE

## 6.6.2.5 void CS\_disableInterrupt ( uint32\_t flags )

Disables individual clock system interrupt sources.

**Parameters**

<i>flags</i>	is a bit mask of the interrupt sources to be disabled. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ CS_LFXT_FAULT,</li> <li>■ CS_HFXT_FAULT,</li> <li>■ CS_DCOMIN_FAULT,</li> <li>■ CS_DCOMAX_FAULT,</li> <li>■ CS_DCO_OPEN_FAULT,</li> <li>■ CS_STARTCOUNT_LFXT_FAULT,</li> <li>■ CS_STARTCOUNT_HFXT_FAULT,</li> </ul>
--------------	--

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**

None.

6.6.2.6 void CS\_enableClockRequest ( uint32\_t *selectClock* )

Enables conditional module requests

**Parameters**

<i>selectClock</i>	selects specific request enables. Valid values are a logical OR of the following values: <ul style="list-style-type: none"> <li>■ <b>CS_ACLK,</b></li> <li>■ <b>CS_HSMCLK,</b></li> <li>■ <b>CS_SMCLK,</b></li> <li>■ <b>CS_MCLK</b></li> </ul>
--------------------	---

**Returns**

NONE

6.6.2.7 void CS\_enableDCOExternalResistor ( void )

Enables the external resistor for DCO operation

**Returns**

NONE

6.6.2.8 void CS\_enableFaultCounter ( uint\_fast8\_t *counterSelect* )

Enables the fault counter for the CS module. This function can enable either the HFXT fault counter or the LFXT fault counter.

**Parameters**

<i>counterSelect</i>	selects the fault counter to enable <ul style="list-style-type: none"> <li>■ <b>CS_HFXT_FAULT_COUNTER</b></li> <li>■ <b>CS_LFXT_FAULT_COUNTER</b></li> </ul>
----------------------	--



**Returns**  
NONE

### 6.6.2.9 void CS\_enableInterrupt ( uint32\_t flags )

Enables individual clock control interrupt sources.

**Parameters**

<i>flags</i>	<p>is a bit mask of the interrupt sources to be enabled. Must be a logical OR of:</p> <ul style="list-style-type: none"> <li>■ CS_LFXT_FAULT,</li> <li>■ CS_HFXT_FAULT,</li> <li>■ CS_DCOMIN_FAULT,</li> <li>■ CS_DCOMAX_FAULT,</li> <li>■ CS_DCO_OPEN_FAULT,</li> <li>■ CS_STARTCOUNT_LFXT_FAULT,</li> <li>■ CS_STARTCOUNT_HFXT_FAULT,</li> </ul>
--------------	--

This function enables the indicated clock system interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**  
None.

### 6.6.2.10 uint32\_t CS\_getACLK ( void )

Get the current ACLK frequency.

If a oscillator fault is set, the frequency returned will be based on the fail safe mechanism of CS module. The user of this API must ensure that [CS\\_setExternalClockSourceFrequency\(\)](#) API was invoked before in case LFXT is being used.

**Returns**  
Current ACLK frequency in Hz

### 6.6.2.11 uint32\_t CS\_getBCLK ( void )

Get the current BCLK frequency.

If a oscillator fault is set, the frequency returned will be based on the fail safe mechanism of CS module. The user of this API must ensure that [CS\\_setExternalClockSourceFrequency](#) API was invoked before in case LFXT or HFXT is being used.

**Returns**

Current BCLK frequency in Hz

6.6.2.12 `uint32_t CS_getDCOFrequency ( void )`

Gets the current tuned DCO frequency. If no tuning has been done, this returns the nominal DCO frequency of the current DCO range. Note that this function will grab any constant/calibration data from the DDS table without any user interaction needed.

**Note**

This function uses floating point math to calculate the DCO tuning parameter. If efficiency is a concern, the user should use the [FPU\\_enableModule](#) function (if available) to enable the floating point co-processor.

**Returns**

Current DCO frequency in Hz

References [SysCtl\\_getTLVInfo\(\)](#).

6.6.2.13 `uint32_t CS_getEnabledInterruptStatus ( void )`

Gets the current interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Returns**

The current interrupt status, enumerated as a bit field of

- `CS_LFXT_FAULT`,
- `CS_HFXT_FAULT`,
- `CS_DCO_OPEN_FAULT`,
- `CS_DCO_SHORT_FAULT`,
- `CS_STARTCOUNT_LFXT_FAULT`,
- `CS_STARTCOUNT_HFXT_FAULT`,

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

References [CS\\_getInterruptStatus\(\)](#).

6.6.2.14 `uint32_t CS_getHSMCLK ( void )`

Get the current HSMCLK frequency.

If an oscillator fault is set, the frequency returned will be based on the fail safe mechanism of CS module. The user of this API must ensure that [CS\\_setExternalClockSourceFrequency](#) API was invoked before in case LFXT or HFXT is being used.

**Returns**

Current HSMCLK frequency in Hz

### 6.6.2.15 uint32\_t CS\_getInterruptStatus ( void )

Gets the current interrupt status.

#### Returns

The current interrupt status, enumerated as a bit field of:

- CS\_LFXT\_FAULT,
- CS\_HFXT\_FAULT,
- CS\_DCO\_OPEN\_FAULT,
- CS\_DCO\_SHORT\_FAULT,
- CS\_STARTCOUNT\_LFXT\_FAULT,
- CS\_STARTCOUNT\_HFXT\_FAULT,

#### Note

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

Referenced by [CS\\_getEnabledInterruptStatus\(\)](#).

### 6.6.2.16 uint32\_t CS\_getMCLK ( void )

Get the current MCLK frequency.

If a oscillator fault is set, the frequency returned will be based on the fail safe mechanism of CS module. The user of this API must ensure that CS\_setExternalClockSourceFrequency API was invoked before in case LFXT or HFXT is being used.

#### Returns

Current MCLK frequency in Hz

### 6.6.2.17 uint32\_t CS\_getSMCLK ( void )

Get the current SMCLK frequency.

If a oscillator fault is set, the frequency returned will be based on the fail safe mechanism of CS module. The user of this API must ensure that CS\_setExternalClockSourceFrequency API was invoked before in case LFXT or HFXT is being used.

#### Returns

Current SMCLK frequency in Hz

### 6.6.2.18 void CS\_initClockSignal ( uint32\_t *selectedClockSignal*, uint32\_t *clockSource*, uint32\_t *clockSourceDivider* )

This function initializes each of the clock signals. The user must ensure that this function is called for each clock signal. If not, the default state is assumed for the particular clock signal. Refer to DriverLib documentation for CS module or Device Family User's Guide for details of default clock signal states.

Note that this function is blocking and will wait on the appropriate bit to be set in the CSSTAT READY register to be set before setting the clock source.

Also note that when HSMCLK and SMCLK share the same clock signal. If you change the clock signal for HSMCLK, the clock signal for SMCLK will change also (and vice-versa).

HFXTCLK is not available for BCLK or ACLK.

#### Parameters

<i>selected-ClockSignal</i>	<p>Clock signal to initialize.</p> <ul style="list-style-type: none"> <li>■ CS_ACLK,</li> <li>■ CS_MCLK,</li> <li>■ CS_HSMCLK</li> <li>■ CS_SMCLK</li> <li>■ CS_BCLK [clockSourceDivider is ignored for this parameter]</li> </ul>
<i>clockSource</i>	<p>Clock source for the selectedClockSignal signal.</p> <ul style="list-style-type: none"> <li>■ CS_LFXTCLK_SELECT,</li> <li>■ CS_HFXTCLK_SELECT,</li> <li>■ CS_VLOCLK_SELECT, [Not available for BCLK]</li> <li>■ CS_DCOCLK_SELECT, [Not available for ACLK, BCLK]</li> <li>■ CS_REFOCLK_SELECT,</li> <li>■ CS_MODOSC_SELECT [Not available for ACLK, BCLK]</li> </ul>
<i>clockSourceDi-vider</i>	<p>- selected the clock divider to calculate clock signal from clock source. This parameter is ignored when setting BLCK. Valid values are:</p> <ul style="list-style-type: none"> <li>■ CS_CLOCK_DIVIDER_1,</li> <li>■ CS_CLOCK_DIVIDER_2,</li> <li>■ CS_CLOCK_DIVIDER_4,</li> <li>■ CS_CLOCK_DIVIDER_8,</li> <li>■ CS_CLOCK_DIVIDER_16,</li> <li>■ CS_CLOCK_DIVIDER_32,</li> <li>■ CS_CLOCK_DIVIDER_64,</li> <li>■ CS_CLOCK_DIVIDER_128</li> </ul>

#### Returns

NONE

6.6.2.19 void CS\_registerInterrupt ( void(\*) (void) *intHandler* )

Registers an interrupt handler for the clock system interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the clock system interrupt occurs.
-------------------	---

This function registers the handler to be called when a clock system interrupt occurs. This function enables the global interrupt in the interrupt controller; specific clock system interrupts must be enabled via [CS\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [CS\\_clearInterruptFlag\(\)](#).

Clock System can generate interrupts when

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

#### 6.6.2.20 void CS\_resetFaultCounter ( uint\_fast8\_t *counterSelect* )

Resets the fault counter for the CS module. This function can reset either the HFXT fault counter or the LFXT fault counter.

**Parameters**

<i>counterSelect</i>	selects the fault counter to reset <ul style="list-style-type: none"> <li>■ <b>CS_HFXT_FAULT_COUNTER</b></li> <li>■ <b>CS_LFXT_FAULT_COUNTER</b></li> </ul>
----------------------	---

**Returns**

NONE

#### 6.6.2.21 void CS\_setDCOCenteredFrequency ( uint32\_t *dcoFreq* )

Sets the centered frequency of DCO operation. Each frequency represents the centred frequency of a particular frequency range. Further tuning can be achieved by using the [CS\\_tuneDCOFrequency](#) function. Note that setting the nominal frequency will reset the tuning parameters.

**Parameters**

<i>dcoFreq</i>	selects between the valid frequencies: <ul style="list-style-type: none"> <li>■ <b>CS_DCO_FREQUENCY_1_5</b>, [1MHz to 2MHz]</li> <li>■ <b>CS_DCO_FREQUENCY_3</b>, [2MHz to 4MHz]</li> <li>■ <b>CS_DCO_FREQUENCY_6</b>, [4MHz to 8MHz]</li> <li>■ <b>CS_DCO_FREQUENCY_12</b>, [8MHz to 16MHz]</li> <li>■ <b>CS_DCO_FREQUENCY_24</b>, [16MHz to 32MHz]</li> <li>■ <b>CS_DCO_FREQUENCY_48</b> [32MHz to 64MHz]</li> </ul>
----------------	--

**Returns**  
NONE

Referenced by [CS\\_setDCOFrequency\(\)](#).

6.6.2.22 void CS\_setDCOExternalResistorCalibration ( uint\_fast8\_t *uiCalData*,  
uint\_fast8\_t *freqRange* )

Sets the calibration value for the DCO when using the external resistor mode. This value is used for tuning the DCO to custom frequencies. By default, the value in the CS module is populated by the calibration data of the suggested external resistor (see device datasheet).

**Parameters**

<i>calData</i>	is the calibration data constant for the external resistor.
<i>freqRange</i>	is the range of the DCO to set the external calibration for. Frequencies above 32MHZ have a different calibration value than frequencies below 32MHZ.

**Returns**  
None

6.6.2.23 void CS\_setDCOFrequency ( uint32\_t *dcoFrequency* )

Automatically sets/tunes the DCO to the given frequency. Any valid value up to max frequency in the spec can be given to this function and the API will do its best to determine the correct tuning parameter.

**Note**

The frequency ranges that can be custom tuned on early release MSP432 devices is limited. For further details on supported tunable frequencies, please refer to the device errata sheet or data sheet.

**Parameters**

<i>dcoFrequency</i>	Frequency in Hz that the user wants to set the DCO to.
---------------------	--

**Note**

This function uses floating point math to calculate the DCO tuning parameter. If efficiency is a concern, the user should use the [FPU\\_enableModule](#) function (if available) to enable the floating point co-processor.

**Returns**  
None

Automatically sets/tunes the DCO to the given frequency. Any valid value up to (and including) 64Mhz can be given to this function and the API will do its best to determine the correct tuning parameter.

**Note**

This function is not currently available on pre-release MSP432 devices. On early release versions of MSP432, the DCO calibration information has not been populated making the DCO only able to operate at the pre-calibrated centered frequencies accessible by the [CS\\_setDCOCenteredFrequency](#) function. While this function will be added on the final devices being released, for early silicon please default to the pre-calibrated DCO center frequencies.

**Parameters**

<i>dcoFrequency</i>	Frequency in Hz (1500000 - 64000000) that the user wants to set the DCO to.
---------------------	---

**Note**

This function uses floating point math to calculate the DCO tuning parameter. If efficiency is a concern, the user should use the [FPU\\_enableModule](#) function (if available) to enable the floating point co-processor.

**Returns**

None

References [CS\\_setDCOCenteredFrequency\(\)](#), [CS\\_tuneDCOFrequency\(\)](#), and [SysCtl\\_getTLVInfo\(\)](#).

6.6.2.24 void CS\_setExternalClockSourceFrequency ( uint32\_t *lfxt\_XT\_CLK\_frequency*, uint32\_t *hfxt\_XT\_CLK\_frequency* )

This function sets the external clock sources LFXT and HFXT crystal oscillator frequency values. This function must be called if an external crystal LFXT or HFXT is used and the user intends to call CS\_getSMCLK, CS\_getMCLK, CS\_getBCLK, CS\_getHSMCLK, CS\_getACLK and any of the HFXT oscillator control functions

**Parameters**

<i>lfxt_XT_CLK_frequency</i>	is the LFXT crystal frequencies in Hz
<i>hfxt_XT_CLK_frequency</i>	is the HFXT crystal frequencies in Hz

**Returns**

None

6.6.2.25 void CS\_setReferenceOscillatorFrequency ( uint8\_t *referenceFrequency* )

Selects between the frequency of the internal REFO clock source

**Parameters**

<i>referenceFrequency</i>	selects between the valid frequencies: <ul style="list-style-type: none"> <li>■ <b>CS_REFO_32KHZ,</b></li> <li>■ <b>CS_REFO_128KHZ,</b></li> </ul>
---------------------------	--

**Returns**  
NONE

6.6.2.26 void CS\_startFaultCounter ( uint\_fast8\_t *counterSelect*, uint\_fast8\_t *countValue* )

Sets the count for the start value of the fault counter. This function can be used to set either the HFXT count or the LFXT count.

**Parameters**

<i>counterSelect</i>	selects the fault counter to reset <ul style="list-style-type: none"> <li>■ <b>CS_HFXT_FAULT_COUNTER</b></li> <li>■ <b>CS_LFXT_FAULT_COUNTER</b></li> </ul>
<i>countValue</i>	selects the cycles to set the fault counter to <ul style="list-style-type: none"> <li>■ <b>CS_FAULT_COUNTER_4096_CYCLES</b></li> <li>■ <b>CS_FAULT_COUNTER_8192_CYCLES</b></li> <li>■ <b>CS_FAULT_COUNTER_16384_CYCLES</b></li> <li>■ <b>CS_FAULT_COUNTER_32768_CYCLES</b></li> </ul>

**Returns**  
NONE

6.6.2.27 bool CS\_startHFXT ( bool *bypassMode* )

Initializes the HFXT crystal oscillator, which supports crystal frequencies between 0 MHz and 48 MHz, depending on the selected drive strength. Loops until all oscillator fault flags are cleared, with no timeout. See the device-specific data sheet for appropriate drive settings. NOTE: User must call CS\_setExternalClockSourceFrequency to set frequency of external clocks before calling this function.

**Parameters**

<i>bypassMode</i>	When this variable is set, the oscillator will start in bypass mode and the signal can be generated by a digital square wave.
-------------------	---

**Returns**  
true if started correctly, false otherwise

References [CS\\_startHFXTWithTimeout\(\)](#).



### 6.6.2.28 bool CS\_startHFXTWithTimeout ( bool *bypassMode*, uint32\_t *timeout* )

Initializes the HFXT crystal oscillator, which supports crystal frequencies between 0 MHz and 48 MHz, depending on the selected drive strength. Loops until all oscillator fault flags are cleared, with no timeout. See the device-specific data sheet for appropriate drive settings. NOTE: User must call CS\_setExternalClockSourceFrequency to set frequency of external clocks before calling this function. This function has a timeout associated with stabilizing the oscillator.

#### Parameters

<i>bypassMode</i>	When this variable is set, the oscillator will start in bypass mode and the signal can be generated by a digital square wave.
<i>timeout</i>	is the count value that gets decremented every time the loop that clears oscillator fault flags gets executed.

#### Returns

true if started correctly, false otherwise

References [SysCtl\\_disableNMISource\(\)](#), [SysCtl\\_enableNMISource\(\)](#), and [SysCtl\\_getNMISourceStatus\(\)](#).

Referenced by [CS\\_startHFXT\(\)](#).

### 6.6.2.29 bool CS\_startLFXT ( uint32\_t *xtDrive* )

Initializes the LFXT crystal oscillator, which supports crystal frequencies up to 50kHz, depending on the selected drive strength. Loops until all oscillator fault flags are cleared, with no timeout. See the device-specific data sheet for appropriate drive settings. NOTE: User must call CS\_setExternalClockSourceFrequency to set frequency of external clocks before calling this function.

#### Parameters

<i>xtDrive</i>	is the target drive strength for the LFXT crystal oscillator. Valid values are: <ul style="list-style-type: none"> <li>■ CS_LFXT_DRIVE0,</li> <li>■ CS_LFXT_DRIVE1,</li> <li>■ CS_LFXT_DRIVE2,</li> <li>■ CS_LFXT_DRIVE3, [Default Value]</li> <li>■ CS_LFXT_BYPASS</li> </ul>
----------------	--

#### Note

When CS\_LFXT\_BYPASS is passed as a parameter the oscillator will start in bypass mode and the signal can be generated by a digital square wave.

#### Returns

true if started correctly, false otherwise

References [CS\\_startLFXTWithTimeout\(\)](#).

### 6.6.2.30 bool CS\_startLFXTWithTimeout ( uint32\_t *xtDrive*, uint32\_t *timeout* )

Initializes the LFXT crystal oscillator, which supports crystal frequencies up to 50kHz, depending on the selected drive strength. Loops until all oscillator fault flags are cleared. See the device-specific data sheet for appropriate drive settings. NOTE: User must call CS\_setExternalClockSourceFrequency to set frequency of external clocks before calling this function. This function has a timeout associated with stabilizing the oscillator.

#### Parameters

<i>xtDrive</i>	is the target drive strength for the LFXT crystal oscillator. Valid values are: <ul style="list-style-type: none"> <li>■ CS_LFXT_DRIVE0,</li> <li>■ CS_LFXT_DRIVE1,</li> <li>■ CS_LFXT_DRIVE2,</li> <li>■ CS_LFXT_DRIVE3, [Default Value]</li> <li>■ CS_LFXT_BYPASS</li> </ul>
----------------	--

#### Note

When CS\_LFXT\_BYPASS is passed as a parameter the oscillator will start in bypass mode and the signal can be generated by a digital square wave.

#### Parameters

<i>timeout</i>	is the count value that gets decremented every time the loop that clears oscillator fault flags gets executed.
----------------	--

#### Returns

true if started correctly, false otherwise

References [SysCtl\\_disableNMISource\(\)](#), [SysCtl\\_enableNMISource\(\)](#), and [SysCtl\\_getNMISourceStatus\(\)](#).

Referenced by [CS\\_startLFXT\(\)](#).

### 6.6.2.31 void CS\_tuneDCOFrequency ( int16\_t *tuneParameter* )

Tunes the DCO to a specific frequency. Tuning of the DCO is based off of the following equation in the user's guide:

See the user's guide for more detailed information about DCO tuning.

#### Note

This function is not currently available on pre-release MSP432 devices. On early release versions of MSP432, the DCO calibration information has not been populated making the DCO only able to operate at the pre-calibrated centered frequencies accessible by the [CS\\_setDCOCenteredFrequency](#) function. While this function will be added on the final devices being released, for early silicon please default to the pre-calibrated DCO center frequencies.

**Parameters**

<i>tuneParameter</i>	Tuning parameter in 2's Compliment representation. Can be negative or positive.
----------------------	---

**Returns**

NONE

Referenced by [CS\\_setDCOFrequency\(\)](#).**6.6.2.32 void CS\_unregisterInterrupt ( void )**

Unregisters the interrupt handler for the clock system.

This function unregisters the handler to be called when a clock system interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 7 Direct Memory Access Controller (DMA)

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## 7.1 Module Operation

The Micro Direct Memory Access (DMA) API provides functions to configure the MSP432 uDMA controller. The DMA controller is designed to work with the ARM Cortex-M processor and provides an efficient and low-overhead means of transferring blocks of data in the system.

The DMA controller has the following features:

- dedicated channels for supported peripherals
- one channel each for receive and transmit for devices with receive and transmit paths
- dedicated channel for software initiated data transfers
- channels can be independently configured and operated
- an arbitration scheme that is configurable per channel
- two levels of priority
- subordinate to Cortex-M processor bus usage
- data sizes of 8, 16, or 32 bits
- address increment of byte, half-word, word, or none
- maskable device requests
- optional software initiated transfers on any channel
- interrupt on transfer completion

The uDMA controller supports several different transfer modes, allowing for complex transfer schemes. The following transfer modes are provided:

- **Basic** mode performs a simple transfer when a request is asserted by a device. This mode is appropriate to use with peripherals where the peripheral asserts the request signal whenever data should be transferred. The transfer pauses if the request is de-asserted, even if the transfer is not complete.
- **Auto-request** mode performs a simple transfer that is started by a request, but always completes the entire transfer, even if the request is de-asserted. This mode is appropriate to use with software-initiated transfers.
- **Ping-Pong** mode is used to transfer data to or from two buffers, switching from one buffer to the other as each buffer fills. This mode is appropriate to use with peripherals as a way to ensure a continuous flow of data to or from the peripheral. However, it is more complex to set up and requires code to manage the ping-pong buffers in the interrupt handler.
- **Memory scatter-gather** mode is a complex mode that provides a way to set up a list of transfer “tasks” for the uDMA controller. Blocks of data can be transferred to and from arbitrary locations in memory.
- **Peripheral scatter-gather** mode is similar to memory scatter-gather mode except that it is controlled by a peripheral request.

Detailed explanation of the various transfer modes is beyond the scope of this document. Please refer to the device data sheet for more information on the operation of the uDMA controller.

## 7.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the DMA module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief example of how to configure the DMA controller to transfer from a data array (data\_array) to the EUSCI I2C module to be sent over the I2C line. This is useful in the sense that the EUSCI module does not constantly have to wake up the CPU in order to load the next byte into the buffer.

```

/* Configuring DMA module */
MAP_DMA_enableModule();
MAP_DMA_setControlBase(controlTable);

/* Assigning Channel 2 to EUSCI1TX0, and Channel 5 to EUSCI2RX0 and
 * enabling channels 2 and 5*/
MAP_DMA_assignChannel(DMA_CH2_EUSCI1TX0);
MAP_DMA_assignChannel(DMA_CH5_EUSCI2RX0);

/* Disabling channel attributes */
MAP_DMA_disableChannelAttribute(DMA_CH2_EUSCI1TX0,
                                UDMA_ATTR_ALTSELECT | UDMA_ATTR_USEBURST |
                                UDMA_ATTR_HIGH_PRIORITY |
                                UDMA_ATTR_REQMASK);
MAP_DMA_disableChannelAttribute(DMA_CH5_EUSCI2RX0,
                                UDMA_ATTR_ALTSELECT | UDMA_ATTR_USEBURST |
                                UDMA_ATTR_HIGH_PRIORITY |
                                UDMA_ATTR_REQMASK);

/* Setting Control Indexes */
MAP_DMA_setChannelControl(UDMA_PRI_SELECT | DMA_CH2_EUSCI1TX0,
                          UDMA_SIZE_8 | UDMA_SRC_INC_8 | UDMA_DST_INC_NONE | UDMA_ARB_1);
MAP_DMA_setChannelControl(UDMA_PRI_SELECT | DMA_CH5_EUSCI2RX0,
                          UDMA_SIZE_8 | UDMA_SRC_INC_NONE | UDMA_DST_INC_8 | UDMA_ARB_1);
MAP_DMA_setChannelTransfer(UDMA_PRI_SELECT | DMA_CH2_EUSCI1TX0,
                          UDMA_MODE_BASIC, data_array,
                          (void*) MAP_I2C_getTransmitBufferAddressForDMA(EUSCI_B1_BASE), 1024);
MAP_DMA_setChannelTransfer(UDMA_PRI_SELECT | DMA_CH5_EUSCI2RX0,
                          UDMA_MODE_BASIC,
                          (void*)MAP_I2C_getReceiveBufferAddressForDMA(EUSCI_B2_BASE), recBuffer,
                          1024);

/* Assigning/Enabling Interrupts */
MAP_DMA_assignInterrupt(DMA_INT1, 2);
MAP_interrupt_enableInterrupt(INT_DMA_INT1);

/* Now that the DMA is primed and setup, enabling the channels. The EUSCI
 * hardware should take over and transfer/receive all bytes */
MAP_DMA_enableChannel(2);
MAP_DMA_enableChannel(5);

/* Sending the start condition */
MAP_I2C_masterSendStart(EUSCI_B1_BASE);
while(!MAP_I2C_masterIsStartSent(EUSCI_B1_BASE));

```

## 7.3 Definitions

### Macros

- #define `DMA_TaskStructEntry`(transferCount, itemSize, srcIncrement, srcAddr, dstIncrement, dstAddr, arbSize, mode)

### Functions

- void `DMA_assignChannel` (uint32\_t mapping)
- void `DMA_assignInterrupt` (uint32\_t interruptNumber, uint32\_t channel)
- void `DMA_clearErrorStatus` (void)
- void `DMA_clearInterruptFlag` (uint32\_t intChannel)
- void `DMA_disableChannel` (uint32\_t channelNum)
- void `DMA_disableChannelAttribute` (uint32\_t channelNum, uint32\_t attr)
- void `DMA_disableInterrupt` (uint32\_t interruptNumber)
- void `DMA_disableModule` (void)
- void `DMA_enableChannel` (uint32\_t channelNum)
- void `DMA_enableChannelAttribute` (uint32\_t channelNum, uint32\_t attr)
- void `DMA_enableInterrupt` (uint32\_t interruptNumber)
- void `DMA_enableModule` (void)
- uint32\_t `DMA_getChannelAttribute` (uint32\_t channelNum)
- uint32\_t `DMA_getChannelMode` (uint32\_t channelStructIndex)
- uint32\_t `DMA_getChannelSize` (uint32\_t channelStructIndex)
- void \* `DMA_getControlAlternateBase` (void)
- void \* `DMA_getControlBase` (void)
- uint32\_t `DMA_getErrorStatus` (void)
- uint32\_t `DMA_getInterruptStatus` (void)
- bool `DMA_isChannelEnabled` (uint32\_t channelNum)
- void `DMA_registerInterrupt` (uint32\_t intChannel, void(\*intHandler)(void))
- void `DMA_requestChannel` (uint32\_t channelNum)
- void `DMA_requestSoftwareTransfer` (uint32\_t channel)
- void `DMA_setChannelControl` (uint32\_t channelStructIndex, uint32\_t control)
- void `DMA_setChannelScatterGather` (uint32\_t channelNum, uint32\_t taskCount, void \*taskList, uint32\_t isPeriphSG)
- void `DMA_setChannelTransfer` (uint32\_t channelStructIndex, uint32\_t mode, void \*srcAddr, void \*dstAddr, uint32\_t transferSize)
- void `DMA_setControlBase` (void \*controlTable)
- void `DMA_unregisterInterrupt` (uint32\_t intChannel)

### 7.3.1 Detailed Description

The code for this module is contained in `driverlib/dma.c`, with `driverlib/dma.h` containing the API declarations for use by applications.

## 7.3.2 Macro Definition Documentation

### 7.3.2.1 `#define DMA_TaskStructEntry( transferCount, itemSize, srcIncrement, srcAddr, dstIncrement, dstAddr, arbSize, mode )`

A helper macro for building scatter-gather task table entries.

This macro is intended to be used to help populate a table of DMA tasks for a scatter-gather transfer. This macro will calculate the values for the fields of a task structure entry based on the input parameters.

There are specific requirements for the values of each parameter. No checking is done so it is up to the caller to ensure that correct values are used for the parameters.

The **transferCount** parameter is the number of items that will be transferred by this task. It must be in the range 1-1024.

The **itemSize** parameter is the bit size of the transfer data. It must be one of **UDMA\_SIZE\_8**, **UDMA\_SIZE\_16**, or **UDMA\_SIZE\_32**.

The **srcIncrement** parameter is the increment size for the source data. It must be one of **UDMA\_SRC\_INC\_8**, **UDMA\_SRC\_INC\_16**, **UDMA\_SRC\_INC\_32**, or **UDMA\_SRC\_INC\_NONE**.

The **srcAddr** parameter is a void pointer to the beginning of the source data.

The **dstIncrement** parameter is the increment size for the destination data. It must be one of **UDMA\_DST\_INC\_8**, **UDMA\_DST\_INC\_16**, **UDMA\_DST\_INC\_32**, or **UDMA\_DST\_INC\_NONE**.

The **dstAddr** parameter is a void pointer to the beginning of the location where the data will be transferred.

The **arbSize** parameter is the arbitration size for the transfer, and must be one of **UDMA\_ARB\_1**, **UDMA\_ARB\_2**, **UDMA\_ARB\_4**, and so on up to **UDMA\_ARB\_1024**. This is used to select the arbitration size in powers of 2, from 1 to 1024.

The **mode** parameter is the mode to use for this transfer task. It must be one of **UDMA\_MODE\_BASIC**, **UDMA\_MODE\_AUTO**, **UDMA\_MODE\_MEM\_SCATTER\_GATHER**, or **UDMA\_MODE\_PER\_SCATTER\_GATHER**. Note that normally all tasks will be one of the scatter-gather modes while the last task in a task list will be AUTO or BASIC.

This macro is intended to be used to initialize individual entries of a structure of **DMA\_ControlTable** type, like this:

```
* DMA_ControlTable MyTaskList[] =
* {
*     DMA_TaskStructEntry(Task1Count, UDMA_SIZE_8,
*                          UDMA_SRC_INC_8, MySourceBuf,
*                          UDMA_DST_INC_8, MyDestBuf,
*                          UDMA_ARB_8, UDMA_MODE_MEM_SCATTER_GATHER),
*     DMA_TaskStructEntry(Task2Count, ... ),
* }
*
```

#### Parameters

<i>transferCount</i>	is the count of items to transfer for this task.
----------------------	--



<i>itemSize</i>	is the bit size of the items to transfer for this task.
<i>srcIncrement</i>	is the bit size increment for source data.
<i>srcAddr</i>	is the starting address of the data to transfer.
<i>dstIncrement</i>	is the bit size increment for destination data.
<i>dstAddr</i>	is the starting address of the destination data.
<i>arbSize</i>	is the arbitration size to use for the transfer task.
<i>mode</i>	is the transfer mode for this task.

**Returns**

Nothing; this is not a function.

### 7.3.3 Function Documentation

#### 7.3.3.1 void DMA\_assignChannel ( uint32\_t mapping )

Assigns a peripheral mapping for a DMA channel.

**Parameters**

<i>mapping</i>	is a macro specifying the peripheral assignment for a channel.
----------------	--

This function assigns a peripheral mapping to a DMA channel. It is used to select which peripheral is used for a DMA channel. The parameter *mapping* should be one of the macros named **UDMA\_CHn\_tttt** from the header file *dma.h*. For example, to assign DMA channel 0 to the eUSCI AO RX channel, the parameter should be the macro **UDMA\_CH1\_EUSCIA0RX**.

Please consult the data sheet for a table showing all the possible peripheral assignments for the DMA channels for a particular device.

**Returns**

None.

#### 7.3.3.2 void DMA\_assignInterrupt ( uint32\_t interruptNumber, uint32\_t channel )

Assigns a specific DMA channel to the corresponding interrupt handler. For MSP432 devices, there are three configurable interrupts, and one master interrupt. This function will assign a specific DMA channel to the provided configurable DMA interrupt.

Note that once a channel is assigned to a configurable interrupt, it will be masked in hardware from the master DMA interrupt (interruptNumber zero). This function can also be used in conjunction with the DMAIntTrigger function to provide the feature to software trigger specific channel interrupts.

**Parameters**

<i>interruptNumber</i>	is the configurable interrupt to assign the given channel. Valid values are: <ul style="list-style-type: none"> <li>■ <b>DMA_INT1</b> the first configurable DMA interrupt handler</li> <li>■ <b>DMA_INT2</b> the second configurable DMA interrupt handler</li> <li>■ <b>DMA_INT3</b> the third configurable DMA interrupt handler</li> </ul>
<i>channel</i>	is the channel to assign the interrupt

**Returns**

None.

References [DMA\\_enableInterrupt\(\)](#).

## 7.3.3.3 void DMA\_clearErrorStatus ( void )

Clears the DMA error interrupt.

This function clears a pending DMA error interrupt. This function should be called from within the DMA error interrupt handler to clear the interrupt.

**Returns**

None.

7.3.3.4 void DMA\_clearInterruptFlag ( uint32\_t *intChannel* )

Clears the DMA controller channel interrupt mask for interrupt zero.

**Parameters**

<i>channel</i>	is the channel interrupt to clear.
----------------	------------------------------------

This function is used to clear the interrupt status of the DMA controller. Note that only interrupts that weren't assigned to DMA interrupts one through three using the [DMA\\_assignInterrupt](#) function will be affected by this functions. For other DMA interrupts, only one channel can be associated and therefore clearing is unnecessary.

**Returns**

None

7.3.3.5 void DMA\_disableChannel ( uint32\_t *channelNum* )

Disables a DMA channel for operation.

**Parameters**

<i>channelNum</i>	is the channel number to disable.
-------------------	-----------------------------------

This function disables a specific DMA channel. Once disabled, a channel cannot respond to DMA transfer requests until re-enabled via [DMA\\_enableChannel\(\)](#).

**Returns**

None.

7.3.3.6 void DMA\_disableChannelAttribute ( uint32\_t *channelNum*, uint32\_t *attr* )

Disables attributes of a DMA channel.

**Parameters**

<i>channelNum</i>	is the channel to configure.
<i>attr</i>	is a combination of attributes for the channel.

This function is used to disable attributes of a DMA channel.

The *attr* parameter is the logical OR of any of the following:

- **UDMA\_ATTR\_USEBURST** is used to restrict transfers to use only burst mode.
- **UDMA\_ATTR\_ALTSELECT** is used to select the alternate control structure for this channel.
- **UDMA\_ATTR\_HIGH\_PRIORITY** is used to set this channel to high priority.
- **UDMA\_ATTR\_REQMASK** is used to mask the hardware request signal from the peripheral for this channel.

**Returns**

None.

### 7.3.3.7 void DMA\_disableInterrupt ( uint32\_t *interruptNumber* )

Disables the specified interrupt for the DMA controller.

**Parameters**

<i>interruptNumber</i>	identifies which DMA interrupt is to be disabled. This interrupt should be one of the following:
------------------------	--

- **DMA\_INT0** the master DMA interrupt handler
  - **DMA\_INT1** the first configurable DMA interrupt handler
  - **DMA\_INT2** the second configurable DMA interrupt handler
  - **DMA\_INT3** the third configurable DMA interrupt handler
  - **DMA\_INTERR** the third configurable DMA interrupt handler
- Note for interrupts that are associated with a specific DMA channel (DMA\_INT1 - DMA\_INT3), this function will also enable that specific channel for interrupts.

**Returns**

None.

### 7.3.3.8 void DMA\_disableModule ( void )

Disables the DMA controller for use.

This function disables the DMA controller. Once disabled, the DMA controller cannot operate until re-enabled with [DMA\\_enableModule\(\)](#).

**Returns**

None.

7.3.3.9 void DMA\_enableChannel ( uint32\_t *channelNum* )

Enables a DMA channel for operation.

**Parameters**

<i>channelNum</i>	is the channel number to enable.
-------------------	----------------------------------

When a DMA transfer is completed, the channel is automatically disabled by the DMA controller. Therefore, this function should be called prior to starting up any new transfer.

**Returns**

None.

### 7.3.3.10 void DMA\_enableChannelAttribute ( uint32\_t *channelNum*, uint32\_t *attr* )

Enables attributes of a DMA channel.

**Parameters**

<i>channelNum</i>	is the channel to configure.
<i>attr</i>	is a combination of attributes for the channel.

This function is used to enable attributes of a DMA channel.

The *attr* parameter is the logical OR of any of the following:

- **UDMA\_ATTR\_USEBURST** is used to restrict transfers to use only burst mode.
- **UDMA\_ATTR\_ALTSELECT** is used to select the alternate control structure for this channel (it is very unlikely that this flag should be used).
- **UDMA\_ATTR\_HIGH\_PRIORITY** is used to set this channel to high priority.
- **UDMA\_ATTR\_REQMASK** is used to mask the hardware request signal from the peripheral for this channel.

**Returns**

None.

### 7.3.3.11 void DMA\_enableInterrupt ( uint32\_t *interruptNumber* )

Enables the specified interrupt for the DMA controller. Note for interrupts one through three, specific channels have to be mapped to the interrupt using the `DMA_assignInterrupt` function.

**Parameters**

<i>interruptNumber</i>	identifies which DMA interrupt is to be enabled. This interrupt should be one of the following:
------------------------	---

- **DMA\_INT0** the master DMA interrupt handler
- **DMA\_INT1** the first configurable DMA interrupt handler
- **DMA\_INT2** the second configurable DMA interrupt handler
- **DMA\_INT3** the third configurable DMA interrupt handler
- **DMA\_INTERR** the third configurable DMA interrupt handler

**Returns**

None.

Referenced by [DMA\\_assignInterrupt\(\)](#).

## 7.3.3.12 void DMA\_enableModule ( void )

Enables the DMA controller for use.

This function enables the DMA controller. The DMA controller must be enabled before it can be configured and used.

**Returns**

None.

7.3.3.13 uint32\_t DMA\_getChannelAttribute ( uint32\_t *channelNum* )

Gets the enabled attributes of a DMA channel.

**Parameters**

<i>channelNum</i>	is the channel to configure.
-------------------	------------------------------

This function returns a combination of flags representing the attributes of the DMA channel.

**Returns**

Returns the logical OR of the attributes of the DMA channel, which can be any of the following:

- **UDMA\_ATTR\_USEBURST** is used to restrict transfers to use only burst mode.
- **UDMA\_ATTR\_ALTSELECT** is used to select the alternate control structure for this channel.
- **UDMA\_ATTR\_HIGH\_PRIORITY** is used to set this channel to high priority.
- **UDMA\_ATTR\_REQMASK** is used to mask the hardware request signal from the peripheral for this channel.

7.3.3.14 uint32\_t DMA\_getChannelMode ( uint32\_t *channelStructIndex* )

Gets the transfer mode for a DMA channel control structure.

**Parameters**

<i>channelStructIndex</i>	is the logical OR of the DMA channel number with either <b>UDMA_PRI_SELECT</b> or <b>UDMA_ALT_SELECT</b> .
---------------------------	--

This function is used to get the transfer mode for the DMA channel and to query the status of a transfer on a channel. When the transfer is complete the mode is **UDMA\_MODE\_STOP**.

**Returns**

Returns the transfer mode of the specified channel and control structure, which is one of the following values: **UDMA\_MODE\_STOP**, **UDMA\_MODE\_BASIC**, **UDMA\_MODE\_AUTO**, **UDMA\_MODE\_PINGPONG**, **UDMA\_MODE\_MEM\_SCATTER\_GATHER**, or **UDMA\_MODE\_PER\_SCATTER\_GATHER**.

7.3.3.15 uint32\_t DMA\_getChannelSize ( uint32\_t *channelStructIndex* )

Gets the current transfer size for a DMA channel control structure.

**Parameters**

<i>channelStructIndex</i>	is the logical OR of the DMA channel number with either <b>UDMA_PRI_SELECT</b> or <b>UDMA_ALT_SELECT</b> .
---------------------------	--

This function is used to get the DMA transfer size for a channel. The transfer size is the number of items to transfer, where the size of an item might be 8, 16, or 32 bits. If a partial transfer has already occurred, then the number of remaining items is returned. If the transfer is complete, then 0 is returned.

**Returns**

Returns the number of items remaining to transfer.

## 7.3.3.16 void\* DMA\_getControlAlternateBase ( void )

Gets the base address for the channel control table alternate structures.

This function gets the base address of the second half of the channel control table that holds the alternate control structures for each channel.

**Returns**

Returns a pointer to the base address of the second half of the channel control table.

## 7.3.3.17 void\* DMA\_getControlBase ( void )

Gets the base address for the channel control table.

This function gets the base address of the channel control table. This table resides in system memory and holds control information for each DMA channel.

**Returns**

Returns a pointer to the base address of the channel control table.

## 7.3.3.18 uint32\_t DMA\_getErrorStatus ( void )

Gets the DMA error status.

This function returns the DMA error status. It should be called from within the DMA error interrupt handler to determine if a DMA error occurred.

**Returns**

Returns non-zero if a DMA error is pending.

## 7.3.3.19 uint32\_t DMA\_getInterruptStatus ( void )

Gets the DMA controller channel interrupt status for interrupt zero.

This function is used to get the interrupt status of the DMA controller. The returned value is a 32-bit bit mask that indicates which channels are requesting an interrupt. This function can be used from within an interrupt handler to determine or confirm which DMA channel has requested an interrupt.

Note that this will only apply to interrupt zero for the DMA controller as only one interrupt can be associated with interrupts one through three. If an interrupt is assigned to an interrupt other than interrupt zero, it will be masked by this function.

**Returns**

Returns a 32-bit mask which indicates requesting DMA channels. There is a bit for each channel and a 1 indicates that the channel is requesting an interrupt. Multiple bits can be set.

7.3.3.20 `bool DMA_isChannelEnabled ( uint32_t channelNum )`

Checks if a DMA channel is enabled for operation.

**Parameters**

<i>channelNum</i>	is the channel number to check.
-------------------	---------------------------------

This function checks to see if a specific DMA channel is enabled. This function can be used to check the status of a transfer, as the channel is automatically disabled at the end of a transfer.

**Returns**

Returns **true** if the channel is enabled, **false** if disabled.

7.3.3.21 `void DMA_registerInterrupt ( uint32_t intChannel, void(*)(void) intHandler )`

Registers an interrupt handler for the DMA controller.

**Parameters**

<i>interruptNumber</i>	identifies which DMA interrupt is to be registered.
<i>intHandler</i>	is a pointer to the function to be called when the interrupt is called.

This function registers and enables the handler to be called when the DMA controller generates an interrupt. The *interrupt* parameter should be one of the following:

- **DMA\_INT0** the master DMA interrupt handler
- **DMA\_INT1** the first configurable DMA interrupt handler
- **DMA\_INT2** the second configurable DMA interrupt handler
- **DMA\_INT3** the third configurable DMA interrupt handler
- **DMA\_INTERR** the third configurable DMA interrupt handler

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

7.3.3.22 `void DMA_requestChannel ( uint32_t channelNum )`

Requests a DMA channel to start a transfer.



**Parameters**

<i>channelNum</i>	is the channel number on which to request a DMA transfer.
-------------------	---

This function allows software to request a DMA channel to begin a transfer. This function could be used for performing a memory-to-memory transfer, or if for some reason a transfer needs to be initiated by software instead of the peripheral associated with that channel.

**Returns**

None.

7.3.3.23 void DMA\_requestSoftwareTransfer ( uint32\_t *channel* )

Initializes a software transfer of the corresponding DMA channel. This is done if the user wants to force a DMA on the specified channel without the hardware precondition. Specific channels can be configured using the DMA\_assignChannel function.

**Parameters**

<i>channel</i>	is the channel to trigger the interrupt
----------------	---

**Returns**

None

7.3.3.24 void DMA\_setChannelControl ( uint32\_t *channelStructIndex*, uint32\_t *control* )

Sets the control parameters for a DMA channel control structure.

**Parameters**

<i>channelStructIndex</i>	is the logical OR of the DMA channel number with <b>UDMA_PRI_SELECT</b> or <b>UDMA_ALT_SELECT</b> .
<i>control</i>	is logical OR of several control values to set the control parameters for the channel.

This function is used to set control parameters for a DMA transfer. These parameters are typically not changed often.

The *channelStructIndex* parameter should be the logical OR of the channel number with one of **UDMA\_PRI\_SELECT** or **UDMA\_ALT\_SELECT** to choose whether the primary or alternate data structure is used.

The *control* parameter is the logical OR of five values: the data size, the source address increment, the destination address increment, the arbitration size, and the use burst flag. The choices available for each of these values is described below.

Choose the data size from one of **UDMA\_SIZE\_8**, **UDMA\_SIZE\_16**, or **UDMA\_SIZE\_32** to select a data size of 8, 16, or 32 bits.

Choose the source address increment from one of **UDMA\_SRC\_INC\_8**, **UDMA\_SRC\_INC\_16**, **UDMA\_SRC\_INC\_32**, or **UDMA\_SRC\_INC\_NONE** to select an address increment of 8-bit bytes, 16-bit half-words, 32-bit words, or to select non-incrementing.

Choose the destination address increment from one of **UDMA\_DST\_INC\_8**, **UDMA\_DST\_INC\_16**, **UDMA\_DST\_INC\_32**, or **UDMA\_SRC\_INC\_8** to select an address increment of 8-bit bytes, 16-bit half-words, 32-bit words, or to select non-incrementing.

The arbitration size determines how many items are transferred before the DMA controller re-arbitrates for the bus. Choose the arbitration size from one of **UDMA\_ARB\_1**, **UDMA\_ARB\_2**, **UDMA\_ARB\_4**, **UDMA\_ARB\_8**, through **UDMA\_ARB\_1024** to select the arbitration size from 1 to 1024 items, in powers of 2.

The value **UDMA\_NEXT\_USEBURST** is used to force the channel to only respond to burst requests at the tail end of a scatter-gather transfer.

**Note**

The address increment cannot be smaller than the data size.

**Returns**

None.

7.3.3.25 void DMA\_setChannelScatterGather ( uint32\_t *channelNum*, uint32\_t *taskCount*, void \* *taskList*, uint32\_t *isPeriphSG* )

Configures a DMA channel for scatter-gather mode.

**Parameters**

<i>channelNum</i>	is the DMA channel number.
<i>taskCount</i>	is the number of scatter-gather tasks to execute.
<i>taskList</i>	is a pointer to the beginning of the scatter-gather task list.
<i>isPeriphSG</i>	is a flag to indicate it is a peripheral scatter-gather transfer (else it is memory scatter-gather transfer)

This function is used to configure a channel for scatter-gather mode. The caller must have already set up a task list and must pass a pointer to the start of the task list as the *taskList* parameter. The *taskCount* parameter is the count of tasks in the task list, not the size of the task list. The flag *isPeriphSG* should be used to indicate if scatter-gather should be configured for peripheral or memory operation.

**See Also**

[DMA\\_TaskStructEntry](#)

**Returns**

None.

7.3.3.26 void DMA\_setChannelTransfer ( uint32\_t *channelStructIndex*, uint32\_t *mode*, void \* *srcAddr*, void \* *dstAddr*, uint32\_t *transferSize* )

Sets the transfer parameters for a DMA channel control structure.

**Parameters**

<i>channelStructIndex</i>	is the logical OR of the DMA channel number with either <b>UDMA_PRI_SELECT</b> or <b>UDMA_ALT_SELECT</b> .
---------------------------	--

<i>mode</i>	is the type of DMA transfer.
<i>srcAddr</i>	is the source address for the transfer.
<i>dstAddr</i>	is the destination address for the transfer.
<i>transferSize</i>	is the number of data items to transfer.

This function is used to configure the parameters for a DMA transfer. These parameters are typically changed often. The function [DMA\\_setChannelControl\(\)](#) MUST be called at least once for this channel prior to calling this function.

The *channelStructIndex* parameter should be the logical OR of the channel number with one of **UDMA\_PRI\_SELECT** or **UDMA\_ALT\_SELECT** to choose whether the primary or alternate data structure is used.

The *mode* parameter should be one of the following values:

- **UDMA\_MODE\_STOP** stops the DMA transfer. The controller sets the mode to this value at the end of a transfer.
- **UDMA\_MODE\_BASIC** to perform a basic transfer based on request.
- **UDMA\_MODE\_AUTO** to perform a transfer that always completes once started even if the request is removed.
- **UDMA\_MODE\_PINGPONG** to set up a transfer that switches between the primary and alternate control structures for the channel. This mode allows use of ping-pong buffering for DMA transfers.
- **UDMA\_MODE\_MEM\_SCATTER\_GATHER** to set up a memory scatter-gather transfer.
- **UDMA\_MODE\_PER\_SCATTER\_GATHER** to set up a peripheral scatter-gather transfer.

The *srcAddr* and *dstAddr* parameters are pointers to the first location of the data to be transferred. These addresses should be aligned according to the item size. The compiler takes care of this alignment if the pointers are pointing to storage of the appropriate data type.

The *transferSize* parameter is the number of data items, not the number of bytes.

The two scatter-gather modes, memory and peripheral, are actually different depending on whether the primary or alternate control structure is selected. This function looks for the **UDMA\_PRI\_SELECT** and **UDMA\_ALT\_SELECT** flag along with the channel number and sets the scatter-gather mode as appropriate for the primary or alternate control structure.

The channel must also be enabled using [DMA\\_enableChannel\(\)](#) after calling this function. The transfer does not begin until the channel has been configured and enabled. Note that the channel is automatically disabled after the transfer is completed, meaning that [DMA\\_enableChannel\(\)](#) must be called again after setting up the next transfer.

#### Note

Great care must be taken to not modify a channel control structure that is in use or else the results are unpredictable, including the possibility of undesired data transfers to or from memory or peripherals. For BASIC and AUTO modes, it is safe to make changes when the channel is disabled, or the [DMA\\_getChannelMode\(\)](#) returns **UDMA\_MODE\_STOP**. For PINGPONG or one of the SCATTER\_GATHER modes, it is safe to modify the primary or alternate control structure only when the other is being used. The [DMA\\_getChannelMode\(\)](#) function returns **UDMA\_MODE\_STOP** when a channel control structure is inactive and safe to modify.

#### Returns

None.

7.3.3.27 void DMA\_setControlBase ( void \* *controlTable* )

Sets the base address for the channel control table.

**Parameters**

<i>controlTable</i>	is a pointer to the 1024-byte-aligned base address of the DMA channel control table.
---------------------	--

This function configures the base address of the channel control table. This table resides in system memory and holds control information for each DMA channel. The table must be aligned on a 1024-byte boundary. The base address must be configured before any of the channel functions can be used.

The size of the channel control table depends on the number of DMA channels and the transfer modes that are used. Refer to the introductory text and the microcontroller datasheet for more information about the channel control table.

**Returns**

None.

### 7.3.3.28 void DMA\_unregisterInterrupt ( uint32\_t *intChannel* )

Unregisters an interrupt handler for the DMA controller.

**Parameters**

<i>interruptNumber</i>	identifies which DMA interrupt to unregister.
------------------------	---

This function disables and unregisters the handler to be called for the specified DMA interrupt. The *interrupt* parameter should be one of **the** parameters as documented for the function [DMA\\_registerInterrupt\(\)](#).

Note for interrupts that are associated with a specific DMA channel (DMA\_INT1 - DMA\_INT3), this function will also disable that specific channel for interrupts.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 8 Flash Memory Controller (FlashCtl)

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### 8.1 Module Operation

The MSP432 DriverLib Flash Controller peripheral is designed to simplify the process of writing, erasing, and configuring the flash memory on the MSP432 part. Many of the stringent verification requirements/preconditions are handled entirely inside the FlashCtl APIs.

### 8.2 Flash Controller Limitations

When utilizing the flash controller for MSP432, the user program has to take special consideration on a few critical limitations. The biggest obstacle that the user has to be mindful of is the stringent verification requirements imposed by the flash controller. Many operations (such as program and verify) will take multiple cycles to complete successfully and the usage is somewhat complicated for a normal user program. For this reason, it is strongly recommended that the user uses the DriverLib APIs for programming and erasing flash. Using the flash controller directly is strongly discouraged as the level of overhead and attention to verification requirements make for a very intricate user experience.

Furthermore, when using the FlashCtl APIs, the user must take special consideration of where the API is being executed. For the critical APIs (such as erase and program), the DriverLib APIs are required to be executed from either SRAM or ROM (using the ROM\_ prefix). Due to the verification requirements of the flash controller, running these APIs out of Flash is not currently supported.

### 8.3 Wait State Considerations

When changing read modes on the MSP432 microcontroller, some read modes (such as erase verify) require an additional number of wait states. The wait states of the flash controller can be configured using the FlashCtl\_setWaitState command. When using the DriverLib APIs, the wait states are automatically changed within the API.

## 8.4 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the FlashCtl module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to unprotect a sector and issue a mass erase with the FlashCtl module:

```
/* Unprotecting User Bank 1, Sectors 30 and 31 */
MAP_FlashCtl_unprotectSector(FLASH_MAIN_MEMORY_SPACE_BANK1,
                             FLASH_SECTOR30 | FLASH_SECTOR31);

/* Trying a mass erase. Since we unprotected User Bank 1,
 * sectors 31 and 32, this should erase these sectors. If it fails, we
 * trap inside an infinite loop.
 */
if(!MAP_FlashCtl_performMassErase())
    while(1);
```

## 8.5 Definitions

### Functions

- void `FlashCtl_clearInterruptFlag` (uint32\_t flags)
- void `FlashCtl_clearProgramVerification` (uint32\_t verificationSetting)
- void `FlashCtl_disableInterrupt` (uint32\_t flags)
- void `FlashCtl_disableReadBuffering` (uint\_fast8\_t memoryBank, uint\_fast8\_t accessMethod)
- void `FlashCtl_disableWordProgramming` (void)
- void `FlashCtl_enableInterrupt` (uint32\_t flags)
- void `FlashCtl_enableReadBuffering` (uint\_fast8\_t memoryBank, uint\_fast8\_t accessMethod)
- void `FlashCtl_enableWordProgramming` (uint32\_t mode)
- bool `FlashCtl_eraseSector` (uint32\_t addr)
- uint32\_t `FlashCtl_getEnabledInterruptStatus` (void)
- uint32\_t `FlashCtl_getInterruptStatus` (void)
- void `FlashCtl_getMemoryInfo` (uint32\_t addr, uint32\_t \*sectorNum, uint32\_t \*bankNum)
- uint32\_t `FlashCtl_getReadMode` (uint32\_t flashBank)
- uint32\_t `FlashCtl_getWaitState` (uint32\_t bank)
- void `FlashCtl_initiateMassErase` (void)
- void `FlashCtl_initiateSectorErase` (uint32\_t addr)
- bool `FlashCtl_isSectorProtected` (uint\_fast8\_t memorySpace, uint32\_t sector)
- uint32\_t `FlashCtl_isWordProgrammingEnabled` (void)
- bool `FlashCtl_performMassErase` (void)
- bool `FlashCtl_programMemory` (void \*src, void \*dest, uint32\_t length)
- bool `FlashCtl_protectSector` (uint\_fast8\_t memorySpace, uint32\_t sectorMask)
- void `FlashCtl_registerInterrupt` (void(\*intHandler)(void))
- void `FlashCtl_setProgramVerification` (uint32\_t verificationSetting)
- bool `FlashCtl_setReadMode` (uint32\_t flashBank, uint32\_t readMode)
- void `FlashCtl_setWaitState` (uint32\_t bank, uint32\_t waitState)
- bool `FlashCtl_unprotectSector` (uint\_fast8\_t memorySpace, uint32\_t sectorMask)
- void `FlashCtl_unregisterInterrupt` (void)
- bool `FlashCtl_verifyMemory` (void \*verifyAddr, uint32\_t length, uint\_fast8\_t pattern)

### 8.5.1 Detailed Description

The code for this module is contained in `driverlib/flash.c`, with `driverlib/flash.h` containing the API declarations for use by applications.



## 8.5.2 Function Documentation

### 8.5.2.1 void FlashCtl\_clearInterruptFlag ( uint32\_t *flags* )

Clears flash system interrupt sources.

#### Parameters

<i>flags</i>	<p>is a bit mask of the interrupt sources to be cleared. Must be a logical OR of:</p> <ul style="list-style-type: none"> <li>■ FLASH_PROGRAM_ERROR,</li> <li>■ FLASH_BENCHMARK_INT,</li> <li>■ FLASH_ERASE_COMPLETE,</li> <li>■ FLASH_BRSTPRGM_COMPLETE,</li> <li>■ FLASH_WRDPRGM_COMPLETE,</li> <li>■ FLASH_POSTVERIFY_FAILED,</li> <li>■ FLASH_PREVERIFY_FAILED,</li> <li>■ FLASH_BRSTRDCMP_COMPLETE</li> </ul>
--------------	---

The specified flash system interrupt sources are cleared, so that they no longer assert. This function must be called in the interrupt handler to keep it from being called again immediately upon exit.

#### Note

Because there is a write buffer in the Cortex-M processor, it may take several clock cycles before the interrupt source is actually cleared. Therefore, it is recommended that the interrupt source be cleared early in the interrupt handler (as opposed to the very last action) to avoid returning from the interrupt handler before the interrupt source is actually cleared. Failure to do so may result in the interrupt handler being immediately reentered (because the interrupt controller still sees the interrupt source asserted).

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**

None.

8.5.2.2 void FlashCtl\_clearProgramVerification ( uint32\_t *verificationSetting* )

Clears pre/post verification of burst and regular flash programming instructions. Note that this API is for advanced users that are programming their own flash drivers. The program/erase APIs are not affected by this setting and take care of the verification requirements.

**Parameters**

<i>verificationSetting</i>	Verification setting to clear. This value can be a bitwise OR of the following values: <ul style="list-style-type: none"> <li>■ <b>FLASH_BURSTPOST</b>,</li> <li>■ <b>FLASH_BURSTPRE</b>,</li> <li>■ <b>FLASH_REGPRE</b>,</li> <li>■ <b>FLASH_REGPOST</b></li> <li>■ <b>FLASH_NOVER</b> No verification enabled</li> <li>■ <b>FLASH_FULLVER</b> Full verification enabled</li> </ul>
----------------------------	--

**Returns**

none

8.5.2.3 void FlashCtl\_disableInterrupt ( uint32\_t *flags* )

Disables individual flash system interrupt sources.

**Parameters**

<i>flags</i>	is a bit mask of the interrupt sources to be disabled. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ <b>FLASH_PROGRAM_ERROR</b>,</li> <li>■ <b>FLASH_BENCHMARK_INT</b>,</li> <li>■ <b>FLASH_ERASE_COMPLETE</b>,</li> <li>■ <b>FLASH_BRSTPRGM_COMPLETE</b>,</li> <li>■ <b>FLASH_WRDPRGM_COMPLETE</b>,</li> <li>■ <b>FLASH_POSTVERIFY_FAILED</b>,</li> <li>■ <b>FLASH_PREVERIFY_FAILED</b>,</li> <li>■ <b>FLASH_BRSTRDCMP_COMPLETE</b></li> </ul>
--------------	---

This function disables the indicated flash system interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Returns**

None.

8.5.2.4 void FlashCtl\_disableReadBuffering ( uint\_fast8\_t *memoryBank*, uint\_fast8\_t *accessMethod* )

Disables read buffering on accesses to a specified bank of flash memory

**Parameters**

<i>memoryBank</i>	is the value of the memory bank to disable read buffering. Must be only one of the following values: <ul style="list-style-type: none"> <li>■ <b>FLASH_BANK0</b>,</li> <li>■ <b>FLASH_BANK1</b></li> </ul>
<i>accessMethod</i>	is the value of the access type to disable read buffering. Must be only one of the following values: <ul style="list-style-type: none"> <li>■ <b>FLASH_DATA_READ</b>,</li> <li>■ <b>FLASH_INSTRUCTION_FETCH</b></li> </ul>

**Returns**

None.

## 8.5.2.5 void FlashCtl\_disableWordProgramming ( void )

Disables word programming of flash memory.

Refer to FlashCtl\_enableWordProgramming and the user's guide for description on the difference between full word and immediate programming

**Returns**

None.

Referenced by [FlashCtl\\_programMemory\(\)](#).

## 8.5.2.6 void FlashCtl\_enableInterrupt ( uint32\_t flags )

Enables individual flash control interrupt sources.

**Parameters**

<i>flags</i>	is a bit mask of the interrupt sources to be enabled. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ <b>FLASH_PROGRAM_ERROR</b>,</li> <li>■ <b>FLASH_BENCHMARK_INT</b>,</li> <li>■ <b>FLASH_ERASE_COMPLETE</b>,</li> <li>■ <b>FLASH_BRSTPRGM_COMPLETE</b>,</li> <li>■ <b>FLASH_WRDPRGM_COMPLETE</b>,</li> <li>■ <b>FLASH_POSTVERIFY_FAILED</b>,</li> <li>■ <b>FLASH_PREVERIFY_FAILED</b>,</li> <li>■ <b>FLASH_BRSTRDCMP_COMPLETE</b></li> </ul>
--------------	--

This function enables the indicated flash system interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**

None.

### 8.5.2.7 void FlashCtl\_enableReadBuffering ( uint\_fast8\_t *memoryBank*, uint\_fast8\_t *accessMethod* )

Enables read buffering on accesses to a specified bank of flash memory

**Parameters**

<i>memoryBank</i>	is the value of the memory bank to enable read buffering. Must be only one of the following values: <ul style="list-style-type: none"> <li>■ FLASH_BANK0,</li> <li>■ FLASH_BANK1</li> </ul>
<i>accessMethod</i>	is the value of the access type to enable read buffering. Must be only one of the following values: <ul style="list-style-type: none"> <li>■ FLASH_DATA_READ,</li> <li>■ FLASH_INSTRUCTION_FETCH</li> </ul>

**Returns**

None.

### 8.5.2.8 void FlashCtl\_enableWordProgramming ( uint32\_t *mode* )

Enables word programming of flash memory.

This function will enable word programming of the flash memory and set the mode of behavior when the flash write occurs.

**Parameters**

<i>mode</i>	The mode specifies the behavior of the flash controller when programming words to flash. In <b>FLASH_IMMEDIATE_WRITE_MODE</b> , the program operation happens immediately on the write to flash while in <b>FLASH_COLLATED_WRITE_MODE</b> the write will be delayed until a full 128-bits have been collated. Possible values include: <ul style="list-style-type: none"> <li>■ FLASH_IMMEDIATE_WRITE_MODE</li> <li>■ FLASH_COLLATED_WRITE_MODE</li> </ul>
-------------	--

Refer to the user's guide for further documentation.

**Returns**

none

Referenced by [FlashCtl\\_programMemory\(\)](#).

8.5.2.9 `bool FlashCtl_eraseSector ( uint32_t addr )`

Erases a sector of MAIN or INFO flash memory.

**Parameters**

<i>addr</i>	The start of the sector to erase. Note that with flash, the minimum allowed size that can be erased is a flash sector (which is 4KB on the MSP432 family). If an address is provided to this function which is not on a 4KB boundary, the entire sector will still be erased.
-------------	---

**Note**

This function is blocking and will not exit until operation has either completed or failed due to an error. Furthermore, given the complex verification requirements of the flash controller, master interrupts are disabled throughout execution of this function. The original interrupt context is saved at the start of execution and restored prior to exit of the API.

Due to the hardware limitations of the flash controller, this function cannot erase a memory address in the same flash bank that it is executing from. If using the ROM version of this API (by using the (ROM\_ or MAP\_ prefixes) this is a don't care, however if this API resides in flash then special care needs to be taken to ensure no code execution or reads happen in the flash bank being programmed while this API is being executed.

**Returns**

true if sector erase is successful, false otherwise.

References [FlashCtl\\_verifyMemory\(\)](#), [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [SysCtl\\_getTLVInfo\(\)](#).

Referenced by [FlashCtl\\_performMassErase\(\)](#).

#### 8.5.2.10 uint32\_t FlashCtl\_getEnabledInterruptStatus ( void )

Gets the current interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Returns**

The current interrupt status, enumerated as a bit field of

- FLASH\_PROGRAM\_ERROR,
- FLASH\_BENCHMARK\_INT,
- FLASH\_ERASE\_COMPLETE,
- FLASH\_BRSTPRGM\_COMPLETE,
- FLASH\_WRDPRGM\_COMPLETE,
- FLASH\_POSTVERIFY\_FAILED,
- FLASH\_PREVERIFY\_FAILED,
- FLASH\_BRSTRDCMP\_COMPLETE

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

References [FlashCtl\\_getInterruptStatus\(\)](#).

#### 8.5.2.11 uint32\_t FlashCtl\_getInterruptStatus ( void )

Gets the current interrupt status.

**Returns**

The current interrupt status, enumerated as a bit field of:

- FLASH\_PROGRAM\_ERROR,
- FLASH\_BENCHMARK\_INT,
- FLASH\_ERASE\_COMPLETE,
- FLASH\_BRSTPRGM\_COMPLETE,
- FLASH\_WRDPRGM\_COMPLETE,
- FLASH\_POSTVERIFY\_FAILED,
- FLASH\_PREVERIFY\_FAILED,
- FLASH\_BRSTRDCMP\_COMPLETE

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

Referenced by [FlashCtl\\_getEnabledInterruptStatus\(\)](#).

#### 8.5.2.12 void FlashCtl\_getMemoryInfo ( uint32\_t *addr*, uint32\_t \* *sectorNum*, uint32\_t \* *bankNum* )

Calculates the flash bank and sector number given an address. Stores the results into the two pointers given as parameters. The user must provide a valid memory address (an address in SRAM for example will give an invalid result).

**Parameters**

<i>addr</i>	Address to calculate the bank/sector information for
<i>sectorNum</i>	The sector number will be stored in here after the function completes.
<i>sectorNum</i>	The bank number will be stored in here after the function completes.

**Note**

For simplicity, this API only works with address in MAIN flash memory. For calculating the sector/bank number of an address in info memory, please refer to your device datasheet/

**Returns**

None.

References [SysCtl\\_getFlashSize\(\)](#).

#### 8.5.2.13 uint32\_t FlashCtl\_getReadMode ( uint32\_t *flashBank* )

Gets the flash read mode to be used by default flash read operations.

**Parameters**

<i>flashBank</i>	Flash bank to set read mode for. Valid values are: <ul style="list-style-type: none"> <li>■ FLASH_BANK0</li> <li>■ FLASH_BANK1</li> </ul>
------------------	---



**Returns**

Returns the read mode to set. Valid values are:

- FLASH\_NORMAL\_READ\_MODE,
- FLASH\_MARGIN0\_READ\_MODE,
- FLASH\_MARGIN1\_READ\_MODE,
- FLASH\_PROGRAM\_VERIFY\_READ\_MODE,
- FLASH\_ERASE\_VERIFY\_READ\_MODE,
- FLASH\_LEAKAGE\_VERIFY\_READ\_MODE,
- FLASH\_MARGIN0B\_READ\_MODE,
- FLASH\_MARGIN1B\_READ\_MODE

Referenced by [FlashCtl\\_verifyMemory\(\)](#).

8.5.2.14 `uint32_t FlashCtl_getWaitState ( uint32_t bank )`

Returns the set number of flash wait states for the given flash bank.

**Parameters**

<i>flashBank</i>	Flash bank to set wait state for. Valid values are: <ul style="list-style-type: none"> <li>■ FLASH_BANK0</li> <li>■ FLASH_BANK1</li> </ul>
------------------	--

**Returns**

The wait state setting for the specified flash bank

Referenced by [FlashCtl\\_verifyMemory\(\)](#).

8.5.2.15 `void FlashCtl_initiateMassErase ( void )`

Initiates a mass erase and returns control back to the program. This is a non-blocking function, however it is the user's responsibility to perform the necessary verification requirements after the interrupt is set to signify completion.

**Returns**

None

8.5.2.16 `void FlashCtl_initiateSectorErase ( uint32_t addr )`

Initiates a sector erase of MAIN or INFO flash memory. Note that this function simply initiates the sector erase, but does no verification which is required by the flash controller. The user must manually set and enable interrupts on the flash controller to fire on erase completion and then use the `FlashCtl_verifyMemory` function to verify that the sector was actually erased

**Parameters**

<i>addr</i>	The start of the sector to erase. Note that with flash, the minimum allowed size that can be erased is a flash sector (which is 4KB on the MSP432 family). If an address is provided to this function which is not on a 4KB boundary, the entire sector will still be erased.
-------------	---

**Returns**

None

8.5.2.17 `bool FlashCtl_isSectorProtected ( uint_fast8_t memorySpace, uint32_t sector )`

Returns the sector protection for given sector mask and memory space

## Parameters

<i>memorySpace</i>	<p>is the value of the memory bank to check for program protection. Must be only one of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>FLASH_MAIN_MEMORY_SPACE_BANK0,</b></li> <li>■ <b>FLASH_MAIN_MEMORY_SPACE_BANK1,</b></li> <li>■ <b>FLASH_INFO_MEMORY_SPACE_BANK0,</b></li> <li>■ <b>FLASH_INFO_MEMORY_SPACE_BANK1</b></li> </ul>
<i>sector</i>	<p>is the sector to check for program protection. Must be one of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>FLASH_SECTOR0,</b></li> <li>■ <b>FLASH_SECTOR1,</b></li> <li>■ <b>FLASH_SECTOR2,</b></li> <li>■ <b>FLASH_SECTOR3,</b></li> <li>■ <b>FLASH_SECTOR4,</b></li> <li>■ <b>FLASH_SECTOR5,</b></li> <li>■ <b>FLASH_SECTOR6,</b></li> <li>■ <b>FLASH_SECTOR7,</b></li> <li>■ <b>FLASH_SECTOR8,</b></li> <li>■ <b>FLASH_SECTOR9,</b></li> <li>■ <b>FLASH_SECTOR10,</b></li> <li>■ <b>FLASH_SECTOR11,</b></li> <li>■ <b>FLASH_SECTOR12,</b></li> <li>■ <b>FLASH_SECTOR13,</b></li> <li>■ <b>FLASH_SECTOR14,</b></li> <li>■ <b>FLASH_SECTOR15,</b></li> <li>■ <b>FLASH_SECTOR16,</b></li> <li>■ <b>FLASH_SECTOR17,</b></li> <li>■ <b>FLASH_SECTOR18,</b></li> <li>■ <b>FLASH_SECTOR19,</b></li> <li>■ <b>FLASH_SECTOR20,</b></li> <li>■ <b>FLASH_SECTOR21,</b></li> <li>■ <b>FLASH_SECTOR22,</b></li> <li>■ <b>FLASH_SECTOR23,</b></li> <li>■ <b>FLASH_SECTOR24,</b></li> <li>■ <b>FLASH_SECTOR25,</b></li> <li>■ <b>FLASH_SECTOR26,</b></li> <li>■ <b>FLASH_SECTOR27,</b></li> <li>■ <b>FLASH_SECTOR28,</b></li> <li>■ <b>FLASH_SECTOR29,</b></li> <li>■ <b>FLASH_SECTOR30,</b></li> <li>■ <b>FLASH_SECTOR31</b></li> </ul>

Note that flash sector sizes are 4KB and the number of sectors may vary depending on the specific device. Also, for INFO memory space, only sectors FLASH\_SECTOR0 and FLASH\_SECTOR1 will exist.

**Note**

Not all devices will contain a dedicated INFO memory. Please check the device datasheet to see if your device has INFO memory available for use. For devices without INFO memory, any operation related to the INFO memory will be ignored by the hardware.

**Returns**

true if sector protection enabled false otherwise.

Referenced by [FlashCtl\\_protectSector\(\)](#), and [FlashCtl\\_unprotectSector\(\)](#).

### 8.5.2.18 uint32\_t FlashCtl\_isWordProgrammingEnabled ( void )

Returns if word programming mode is enabled (and if it is, the specific mode)

Refer to [FlashCtl\\_enableWordProgramming](#) and the user's guide for description on the difference between full word and immediate programming

**Returns**

a zero value if word programming is disabled,

- **FLASH\_IMMEDIATE\_WRITE\_MODE**
- **FLASH\_COLLATED\_WRITE\_MODE**

### 8.5.2.19 bool FlashCtl\_performMassErase ( void )

Performs a mass erase on all unprotected flash sectors. Protected sectors are ignored.

**Note**

This function is blocking and will not exit until operation has either completed or failed due to an error. Furthermore, given the complex verification requirements of the flash controller, master interrupts are disabled throughout execution of this function. The original interrupt context is saved at the start of execution and restored prior to exit of the API.

Due to the hardware limitations of the flash controller, this function cannot erase a memory address in the same flash bank that it is executing from. If using the ROM version of this API (by using the (ROM\_ or MAP\_ prefixes) this is a don't care, however if this API resides in flash then special care needs to be taken to ensure no code execution or reads happen in the flash bank being programmed while this API is being executed.

**Returns**

true if mass erase completes successfully, false otherwise

References [FlashCtl\\_eraseSector\(\)](#), [FlashCtl\\_verifyMemory\(\)](#), [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [SysCtl\\_getFlashSize\(\)](#).

### 8.5.2.20 bool FlashCtl\_programMemory ( void \* src, void \* dest, uint32\_t length )

Program a portion of flash memory with the provided data

**Parameters**

<i>src</i>	Pointer to the data source to program into flash
<i>dest</i>	Pointer to the destination in flash to program
<i>length</i>	Length in bytes to program

**Note**

There are no sector/boundary restrictions for this function, however it is encouraged to provide a start address aligned on 32-bit boundaries. Providing an unaligned address will result in unaligned data accesses and detriment efficiency.

This function is blocking and will not exit until operation has either completed or failed due to an error. Furthermore, given the complex verification requirements of the flash controller, master interrupts are disabled throughout execution of this function. The original interrupt context is saved at the start of execution and restored prior to exit of the API.

Due to the hardware limitations of the flash controller, this function cannot program a memory address in the same flash bank that it is executing from. If using the ROM version of this API (by using the (ROM\_ or MAP\_ prefixes) this is a don't care, however if this API resides in flash then special care needs to be taken to ensure no code execution or reads happen in the flash bank being programmed while this API is being executed.

**Returns**

Whether or not the program succeeded

References [FlashCtl\\_disableWordProgramming\(\)](#), [FlashCtl\\_enableWordProgramming\(\)](#), [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [SysCtl\\_getTLVInfo\(\)](#).

### 8.5.2.21 bool FlashCtl\_protectSector ( uint\_fast8\_t *memorySpace*, uint32\_t *sectorMask* )

Enables program protection on the given sector mask. This setting can be applied on a sector-wise bases on a given memory space (INFO or MAIN).

**Parameters**

<i>memorySpace</i>	is the value of the memory bank to enable program protection. Must be only one of the following values: <ul style="list-style-type: none"> <li>■ FLASH_MAIN_MEMORY_SPACE_BANK0,</li> <li>■ FLASH_MAIN_MEMORY_SPACE_BANK1,</li> <li>■ FLASH_INFO_MEMORY_SPACE_BANK0,</li> <li>■ FLASH_INFO_MEMORY_SPACE_BANK1</li> </ul>
--------------------	---

<i>sectorMask</i>	<p>is a bit mask of the sectors to enable program protection. Must be a bitfield of the following values:</p> <ul style="list-style-type: none"><li>■ FLASH_SECTOR0,</li><li>■ FLASH_SECTOR1,</li><li>■ FLASH_SECTOR2,</li><li>■ FLASH_SECTOR3,</li><li>■ FLASH_SECTOR4,</li><li>■ FLASH_SECTOR5,</li><li>■ FLASH_SECTOR6,</li><li>■ FLASH_SECTOR7,</li><li>■ FLASH_SECTOR8,</li><li>■ FLASH_SECTOR9,</li><li>■ FLASH_SECTOR10,</li><li>■ FLASH_SECTOR11,</li><li>■ FLASH_SECTOR12,</li><li>■ FLASH_SECTOR13,</li><li>■ FLASH_SECTOR14,</li><li>■ FLASH_SECTOR15,</li><li>■ FLASH_SECTOR16,</li><li>■ FLASH_SECTOR17,</li><li>■ FLASH_SECTOR18,</li><li>■ FLASH_SECTOR19,</li><li>■ FLASH_SECTOR20,</li><li>■ FLASH_SECTOR21,</li><li>■ FLASH_SECTOR22,</li><li>■ FLASH_SECTOR23,</li><li>■ FLASH_SECTOR24,</li><li>■ FLASH_SECTOR25,</li><li>■ FLASH_SECTOR26,</li><li>■ FLASH_SECTOR27,</li><li>■ FLASH_SECTOR28,</li><li>■ FLASH_SECTOR29,</li><li>■ FLASH_SECTOR30,</li><li>■ FLASH_SECTOR31</li></ul>
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**Note**

Flash sector sizes are 4KB and the number of sectors may vary depending on the specific device. Also, for INFO memory space, only sectors **FLASH\_SECTOR0** and **FLASH\_SECTOR1** will exist.

Not all devices will contain a dedicated INFO memory. Please check the device datasheet to see if your device has INFO memory available for use. For devices without INFO memory, any operation related to the INFO memory will be ignored by the hardware.

**Returns**

true if sector protection enabled false otherwise.

References [FlashCtl\\_isSectorProtected\(\)](#).

### 8.5.2.22 void FlashCtl\_registerInterrupt ( void(\*)(void) *intHandler* )

Registers an interrupt handler for flash clock system interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the clock system interrupt occurs.
-------------------	---

This function registers the handler to be called when a clock system interrupt occurs. This function enables the global interrupt in the interrupt controller; specific flash controller interrupts must be enabled via [FlashCtl\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [FlashCtl\\_clearInterruptFlag\(\)](#).

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 8.5.2.23 void FlashCtl\_setProgramVerification ( uint32\_t *verificationSetting* )

Setups pre/post verification of burst and regular flash programming instructions. Note that this API is for advanced users that are programming their own flash drivers. The program/erase APIs are not affected by this setting and take care of the verification requirements.

**Parameters**

<i>verificationSetting</i>	<p>Verification setting to set. This value can be a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>FLASH_BURSTPOST</b>,</li> <li>■ <b>FLASH_BURSTPRE</b>,</li> <li>■ <b>FLASH_REGPRE</b>,</li> <li>■ <b>FLASH_REGPOST</b></li> <li>■ <b>FLASH_NOVER</b> No verification enabled</li> <li>■ <b>FLASH_FULLVER</b> Full verification enabled</li> </ul>
----------------------------	---

**Returns**

none

8.5.2.24 bool FlashCtl\_setReadMode ( uint32\_t *flashBank*, uint32\_t *readMode* )

Sets the flash read mode to be used by default flash read operations. Note that the proper wait states must be set prior to entering this function.

**Parameters**

<i>flashBank</i>	Flash bank to set read mode for. Valid values are: <ul style="list-style-type: none"> <li>■ FLASH_BANK0</li> <li>■ FLASH_BANK1</li> </ul>
<i>readMode</i>	The read mode to set. Valid values are: <ul style="list-style-type: none"> <li>■ FLASH_NORMAL_READ_MODE,</li> <li>■ FLASH_MARGIN0_READ_MODE,</li> <li>■ FLASH_MARGIN1_READ_MODE,</li> <li>■ FLASH_PROGRAM_VERIFY_READ_MODE,</li> <li>■ FLASH_ERASE_VERIFY_READ_MODE,</li> <li>■ FLASH_LEAKAGE_VERIFY_READ_MODE,</li> <li>■ FLASH_MARGIN0B_READ_MODE,</li> <li>■ FLASH_MARGIN1B_READ_MODE</li> </ul>

**Returns**

None.

Referenced by [FlashCtl\\_verifyMemory\(\)](#).

8.5.2.25 void FlashCtl\_setWaitState ( uint32\_t *bank*, uint32\_t *waitState* )

Changes the number of wait states that are used by the flash controller for read operations. When changing frequency ranges of the clock, this functions must be used in order to allow for readable flash memory.

**Parameters**

<i>waitState</i>	The number of wait states to set. Note that only bits 0-3 are used.
<i>flashBank</i>	Flash bank to set wait state for. Valid values are: <ul style="list-style-type: none"> <li>■ FLASH_BANK0</li> <li>■ FLASH_BANK1</li> </ul>

Referenced by [FlashCtl\\_verifyMemory\(\)](#).



8.5.2.26 `bool FlashCtl_unprotectSector ( uint_fast8_t memorySpace, uint32_t sectorMask )`

Disables program protection on the given sector mask. This setting can be applied on a sector-wise bases on a given memory space (INFO or MAIN).

## Parameters

<i>memorySpace</i>	<p>is the value of the memory bank to disable program protection. Must be only one of the following values:</p> <ul style="list-style-type: none"> <li>■ FLASH_MAIN_MEMORY_SPACE_BANK0,</li> <li>■ FLASH_MAIN_MEMORY_SPACE_BANK1,</li> <li>■ FLASH_INFO_MEMORY_SPACE_BANK0,</li> <li>■ FLASH_INFO_MEMORY_SPACE_BANK1</li> </ul>
<i>sectorMask</i>	<p>is a bit mask of the sectors to disable program protection. Must be a bitfield of the following values:</p> <ul style="list-style-type: none"> <li>■ FLASH_SECTOR0,</li> <li>■ FLASH_SECTOR1,</li> <li>■ FLASH_SECTOR2,</li> <li>■ FLASH_SECTOR3,</li> <li>■ FLASH_SECTOR4,</li> <li>■ FLASH_SECTOR5,</li> <li>■ FLASH_SECTOR6,</li> <li>■ FLASH_SECTOR7,</li> <li>■ FLASH_SECTOR8,</li> <li>■ FLASH_SECTOR9,</li> <li>■ FLASH_SECTOR10,</li> <li>■ FLASH_SECTOR11,</li> <li>■ FLASH_SECTOR12,</li> <li>■ FLASH_SECTOR13,</li> <li>■ FLASH_SECTOR14,</li> <li>■ FLASH_SECTOR15,</li> <li>■ FLASH_SECTOR16,</li> <li>■ FLASH_SECTOR17,</li> <li>■ FLASH_SECTOR18,</li> <li>■ FLASH_SECTOR19,</li> <li>■ FLASH_SECTOR20,</li> <li>■ FLASH_SECTOR21,</li> <li>■ FLASH_SECTOR22,</li> <li>■ FLASH_SECTOR23,</li> <li>■ FLASH_SECTOR24,</li> <li>■ FLASH_SECTOR25,</li> <li>■ FLASH_SECTOR26,</li> <li>■ FLASH_SECTOR27,</li> <li>■ FLASH_SECTOR28,</li> <li>■ FLASH_SECTOR29,</li> <li>■ FLASH_SECTOR30,</li> <li>■ FLASH_SECTOR31</li> </ul>

**Note**

Flash sector sizes are 4KB and the number of sectors may vary depending on the specific device. Also, for INFO memory space, only sectors **FLASH\_SECTOR0** and **FLASH\_SECTOR1** will exist.

Not all devices will contain a dedicated INFO memory. Please check the device datasheet to see if your device has INFO memory available for use. For devices without INFO memory, any operation related to the INFO memory will be ignored by the hardware.

**Returns**

true if sector protection disabled false otherwise.

References [FlashCtl\\_isSectorProtected\(\)](#).

## 8.5.2.27 void FlashCtl\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the flash system.

This function unregisters the handler to be called when a clock system interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

8.5.2.28 bool FlashCtl\_verifyMemory ( void \* *verifyAddr*, uint32\_t *length*, uint\_fast8\_t *pattern* )

Verifies a given segment of memory based off either a high (1) or low (0) state.

**Parameters**

<i>verifyAddr</i>	Start address where verification will begin
<i>length</i>	Length in bytes to verify based off the pattern
<i>pattern</i>	The pattern which verification will check versus. This can either be a low pattern (each register will be checked versus a pattern of 32 zeros, or a high pattern (each register will be checked versus a pattern of 32 ones). Valid values are: FLASH_0_PATTERN, FLASH_1_PATTERN

**Note**

There are no sector/boundary restrictions for this function, however it is encouraged to provide a start address aligned on 32-bit boundaries. Providing an unaligned address will result in unaligned data accesses and detriment efficiency.

This function is blocking and will not exit until operation has either completed or failed due to an error. Furthermore, given the complex verification requirements of the flash controller, master interrupts are disabled throughout execution of this function. The original interrupt context is saved at the start of execution and restored prior to exit of the API.

Due to the hardware limitations of the flash controller, this function cannot verify a memory address in the same flash bank that it is executing from. If using the ROM version of this API (by using the (ROM\_ or MAP\_ prefixes) this is a don't care, however if this API resides in flash then special care needs to be taken to ensure no code execution or reads happen in the flash bank being programmed while this API is being executed.

**Returns**

true if memory verification is successful, false otherwise.

References [FlashCtl\\_getReadMode\(\)](#), [FlashCtl\\_getWaitState\(\)](#), [FlashCtl\\_setReadMode\(\)](#), [FlashCtl\\_setWaitState\(\)](#), [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [SysCtl\\_getFlashSize\(\)](#).

Referenced by [FlashCtl\\_eraseSector\(\)](#), and [FlashCtl\\_performMassErase\(\)](#).

## 9 Floating Point Unit (FPU)

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### 9.1 Module Operation

The floating-point unit (FPU) driver provides methods for manipulating the behavior of the floating-point unit in the Cortex-M processor. By default, the floating-point is disabled and must be enabled prior to the execution of any floating-point instructions. If a floating-point instruction is executed when the floating-point unit is disabled, a NOCP usage fault is generated. This feature can be used by an RTOS, for example, to keep track of which tasks actually use the floating-point unit, and therefore only perform floating-point context save/restore on task switches that involve those tasks.

There are three methods of handling the floating-point context when the processor executes an interrupt handler: it can do nothing with the floating-point context, it can always save the floating-point context, or it can perform a lazy save/restore of the floating-point context. If nothing is done with the floating-point context, the interrupt stack frame is identical to a Cortex-M processor that does not have a floating-point unit, containing only the volatile registers of the integer unit. This method is useful for applications where the floating-point unit is used by the main thread of execution, but not in any of the interrupt handlers. By not saving the floating-point context, stack usage is reduced and interrupt latency is kept to a minimum.

Alternatively, the floating-point context can always be saved onto the stack. This method allows floating-point operations to be performed inside interrupt handlers without any special precautions, at the expense of increased stack usage (for the floating-point context) and increased interrupt latency (due to the additional writes to the stack). The advantage to this method is that the stack frame always contains the floating-point context when inside an interrupt handler.

The default handling of the floating-point context is to perform a lazy save/restore. When an interrupt is taken, space is reserved on the stack for the floating-point context but the context is not written. This method keeps the interrupt latency to a minimum because only the integer state is written to the stack. Then, if a floating-point instruction is executed from within the interrupt handler, the floating-point context is written to the stack prior to the execution of the floating-point instruction. Finally, upon return from the interrupt, the floating-point context is restored from the stack only if it was written. Using lazy save/restore provides a blend between fast interrupt response and the ability to use floating-point instructions in the interrupt handler.

The floating-point unit can generate an interrupt when one of several exceptions occur. The exceptions are underflow, overflow, divide by zero, invalid operation, input denormal, and inexact exception. The application can optionally choose to enable one or more of these interrupts and use the interrupt handler to decide upon a course of action to be taken in each case.

The behavior of the floating-point unit can also be adjusted, specifying the format of half-precision floating-point values, the handle of NaN values, the flush-to-zero mode (which sacrifices full IEEE compliance for execution speed), and the rounding mode for results.

## 9.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the FPU module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief example of floating point operation. While the compiler will usually enable the floating point unit by default, when executing floating point operations it is important to make sure that the coprocessor is enabled (otherwise a system fault will occur).

```
/* Enabling FPU for DCO Frequency calculation */  
MAP_FPU_enableModule();  
  
/* Setting the DCO Frequency to a non-standard 8.33MHz */  
MAP_CS_setDCOFrequency(8330000);
```

## 9.3 Definitions

### Functions

- void `FPU_disableModule` (void)
- void `FPU_disableStacking` (void)
- void `FPU_enableLazyStacking` (void)
- void `FPU_enableModule` (void)
- void `FPU_enableStacking` (void)
- void `FPU_setFlushToZeroMode` (uint32\_t mode)
- void `FPU_setHalfPrecisionMode` (uint32\_t mode)
- void `FPU_setNaNMode` (uint32\_t mode)
- void `FPU_setRoundingMode` (uint32\_t mode)

### 9.3.1 Detailed Description

The code for this module is contained in `driverlib/fpu.c`, with `driverlib/fpu.h` containing the API declarations for use by applications.

## 9.3.2 Function Documentation

### 9.3.2.1 void FPU\_disableModule ( void )

Disables the floating-point unit.

This function disables the floating-point unit, preventing floating-point instructions from executing (generating a NOCP usage fault instead).

**Returns**

None.

### 9.3.2.2 void FPU\_disableStacking ( void )

Disables the stacking of floating-point registers.

This function disables the stacking of floating-point registers s0-s15 when an interrupt is handled. When floating-point context stacking is disabled, floating-point operations performed in an interrupt handler destroy the floating-point context of the main thread of execution.

**Returns**

None.

### 9.3.2.3 void FPU\_enableLazyStacking ( void )

Enables the lazy stacking of floating-point registers.

This function enables the lazy stacking of floating-point registers s0-s15 when an interrupt is handled. When lazy stacking is enabled, space is reserved on the stack for the floating-point context, but the floating-point state is not saved. If a floating-point instruction is executed from within the interrupt context, the floating-point context is first saved into the space reserved on the stack. On completion of the interrupt handler, the floating-point context is only restored if it was saved (as the result of executing a floating-point instruction).

This method provides a compromise between fast interrupt response (because the floating-point state is not saved on interrupt entry) and the ability to use floating-point in interrupt handlers (because the floating-point state is saved if floating-point instructions are used).

**Returns**

None.

### 9.3.2.4 void FPU\_enableModule ( void )

Enables the floating-point unit.

This function enables the floating-point unit, allowing the floating-point instructions to be executed. This function must be called prior to performing any hardware floating-point operations; failure to do so results in a NOCP usage fault.



**Returns**

None.

## 9.3.2.5 void FPU\_enableStacking ( void )

Enables the stacking of floating-point registers.

This function enables the stacking of floating-point registers s0-s15 when an interrupt is handled. When enabled, space is reserved on the stack for the floating-point context and the floating-point state is saved into this stack space. Upon return from the interrupt, the floating-point context is restored.

If the floating-point registers are not stacked, floating-point instructions cannot be safely executed in an interrupt handler because the values of s0-s15 are not likely to be preserved for the interrupted code. On the other hand, stacking the floating-point registers increases the stacking operation from 8 words to 26 words, also increasing the interrupt response latency.

**Returns**

None.

## 9.3.2.6 void FPU\_setFlushToZeroMode ( uint32\_t mode )

Selects the flush-to-zero mode.

**Parameters**

<i>mode</i>	is the flush-to-zero mode; which is either <b>FPU_FLUSH_TO_ZERO_DIS</b> or <b>FPU_FLUSH_TO_ZERO_EN</b> .
-------------	--

This function enables or disables the flush-to-zero mode of the floating-point unit. When disabled (the default), the floating-point unit is fully IEEE compliant. When enabled, values close to zero are treated as zero, greatly improving the execution speed at the expense of some accuracy (as well as IEEE compliance).

**Note**

Unless this function is called prior to executing any floating-point instructions, the default mode is used.

**Returns**

None.

## 9.3.2.7 void FPU\_setHalfPrecisionMode ( uint32\_t mode )

Selects the format of half-precision floating-point values.

**Parameters**

<i>mode</i>	is the format for half-precision floating-point value, which is either <b>FPU_HALF_IEEE</b> or <b>FPU_HALF_ALTERNATE</b> .
-------------	--

This function selects between the IEEE half-precision floating-point representation and the Cortex-M processor alternative representation. The alternative representation has a larger range but does not have a way to encode infinity (positive or negative) or NaN (quiet or signalling). The default setting is the IEEE format.

**Note**

Unless this function is called prior to executing any floating-point instructions, the default mode is used.

**Returns**

None.

### 9.3.2.8 void FPU\_setNaNMode ( uint32\_t *mode* )

Selects the NaN mode.

**Parameters**

<i>mode</i>	is the mode for NaN results; which is either <b>FPU_NAN_PROPAGATE</b> or <b>FPU_NAN_DEFAULT</b> .
-------------	---

This function selects the handling of NaN results during floating-point computations. NaNs can either propagate (the default), or they can return the default NaN.

**Note**

Unless this function is called prior to executing any floating-point instructions, the default mode is used.

**Returns**

None.

### 9.3.2.9 void FPU\_setRoundingMode ( uint32\_t *mode* )

Selects the rounding mode for floating-point results.

**Parameters**

<i>mode</i>	is the rounding mode.
-------------	-----------------------

This function selects the rounding mode for floating-point results. After a floating-point operation, the result is rounded toward the specified value. The default mode is **FPU\_ROUND\_NEAREST**.

The following rounding modes are available (as specified by *mode*):

- **FPU\_ROUND\_NEAREST** - round toward the nearest value
- **FPU\_ROUND\_POS\_INF** - round toward positive infinity
- **FPU\_ROUND\_NEG\_INF** - round toward negative infinity
- **FPU\_ROUND\_ZERO** - round toward zero

**Note**

Unless this function is called prior to executing any floating-point instructions, the default mode is used.

**Returns**

None.

# 10 General Purpose Input/Output (GPIO)

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## 10.1 Module Operation

The Digital I/O (GPIO) API provides a set of functions for using the MSPWare L GPIO modules. Functions are provided to setup and enable use of input/output pins, setting them up with or without interrupts and those that access the pin value.

## 10.2 Key Features

The digital I/O features include:

- Independently programmable individual I/Os
- Any combination of input or output
- Individually configurable P1 and P2 interrupts. Some devices may include additional port interrupts.
- Independent input and output data registers
- Individually configurable pullup or pulldown resistors

Devices within the family may have up to twelve digital I/O ports implemented (P1 to P11 and PJ). Most ports contain eight I/O lines; however, some ports may contain less (see the device-specific data sheet for ports available). Each I/O line is individually configurable for input or output direction, and each can be individually read or written. Each I/O line is individually configurable for pullup or pulldown resistors. PJ contains only four I/O lines.

Individual ports can be accessed as byte-wide ports or can be combined into word-wide ports and accessed via word formats. Port pairs P1/P2, P3/P4, P5/P6, P7/P8, etc., are associated with the names PA, PB, PC, PD, etc., respectively. All port registers are handled in this manner with this naming convention.

When writing to port PA with word operations, all 16 bits are written to the port. When writing to the lower byte of the PA port using byte operations, the upper byte remains unchanged. Similarly, writing to the upper byte of the PA port using byte instructions leaves the lower byte unchanged. When writing to a port that contains less than the maximum number of bits possible, the unused bits are a "don't care". Ports PB, PC, PD, PE, and PF behave similarly.

Reading of the PA port using word operations causes all 16 bits to be transferred to the destination. Reading the lower or upper byte of the PA port (P1 or P2) and storing to memory using byte operations causes only the lower or upper byte to be transferred to the destination, respectively. Reading of the PA port and storing to a general-purpose register using byte operations causes the byte transferred to be written to the least significant byte of the register. The upper significant byte of the destination register is cleared automatically. Ports PB, PC, PD, PE,

and PF behave similarly. When reading from ports that contain less than the maximum bits possible, unused bits are read as zeros (similarly for port PJ).

The GPIO pin may be configured as an I/O pin with `GPIO_setAsOutputPin`, `GPIO_setAsInputPin`, `GPIO_setAsInputPinWithPullDownResistor` or `GPIO_setAsInputPinWithPullUpResistor`. The GPIO pin may instead be configured to operate in the Peripheral Module assigned function by configuring the GPIO using `GPIO_setAsPeripheralModuleFunctionOutputPin` or `GPIO_setAsPeripheralModuleFunctionInputPin`.

## 10.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the GPIO module. These code examples are accessible under the `examples/` folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a simple example of how to set up a GPIO in output mode and toggle an LED using a simple delay:

```
int main(void)
{
    volatile uint32_t ii;

    /* Halting the Watchdog */
    MAP_WDT_A_holdTimer();

    /* Configuring P1.0 as output */
    MAP_GPIO_setAsOutputPin(GPIO_PORT_P1, GPIO_PIN0);

    while (1)
    {
        /* Delay Loop */
        for(ii=0;ii<5000;ii++)
        {
        }

        MAP_GPIO_toggleOutputOnPin(GPIO_PORT_P1, GPIO_PIN0);
    }
}
```

## 10.4 Definitions

### Functions

- void `GPIO_clearInterruptFlag` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_disableInterrupt` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_enableInterrupt` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- uint\_fast16\_t `GPIO_getEnabledInterruptStatus` (uint\_fast8\_t selectedPort)
- uint8\_t `GPIO_getInputPinValue` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- uint\_fast16\_t `GPIO_getInterruptStatus` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_interruptEdgeSelect` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins, uint\_fast8\_t edgeSelect)
- void `GPIO_registerInterrupt` (uint\_fast8\_t selectedPort, void(\*intHandler)(void))
- void `GPIO_setAsInputPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_setAsInputPinWithPullDownResistor` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_setAsInputPinWithPullUpResistor` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_setAsOutputPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_setAsPeripheralModuleFunctionInputPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins, uint\_fast8\_t mode)
- void `GPIO_setAsPeripheralModuleFunctionOutputPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins, uint\_fast8\_t mode)
- void `GPIO_setDriveStrengthHigh` (uint\_fast8\_t selectedPort, uint\_fast8\_t selectedPins)
- void `GPIO_setDriveStrengthLow` (uint\_fast8\_t selectedPort, uint\_fast8\_t selectedPins)
- void `GPIO_setOutputHighOnPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_setOutputLowOnPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_toggleOutputOnPin` (uint\_fast8\_t selectedPort, uint\_fast16\_t selectedPins)
- void `GPIO_unregisterInterrupt` (uint\_fast8\_t selectedPort)

### 10.4.1 Detailed Description

The code for this module is contained in `driverlib/gpio.c` and `driverlib/legacy/MSP432xx/legacy_gpio.c`, with `driverlib/gpio.h` and `driverlib/legacy/MSP432xx/legacy_gpio.h` containing the API declarations for use by applications.

## 10.4.2 Function Documentation

### 10.4.2.1 void GPIO\_clearInterruptFlag ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function clears the interrupt flag on the selected pin.

This function clears the interrupt flag on the selected pin. Note that only Port 1, 2, A have this capability.

#### Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_PA</li> </ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>

Modified bits of **PxIFG** register.

#### Returns

None

### 10.4.2.2 void GPIO\_disableInterrupt ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function disables the port interrupt on the selected pin.

This function disables the port interrupt on the selected pin. Note that only Port 1, 2, A have this capability.



## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_PA</li> </ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>

Modified bits of **PxIE** register.

**Returns**

None

10.4.2.3 void GPIO\_enableInterrupt ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function enables the port interrupt on the selected pin.

This function enables the port interrupt on the selected pin. Note that only Port 1, 2, A have this capability.

## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_PA</li> </ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>

Modified bits of **PxIE** register.

**Returns**

None

#### 10.4.2.4 uint\_fast16\_t GPIO\_getEnabledInterruptStatus ( uint\_fast8\_t *selectedPort* )

This function gets the interrupt status of the provided PIN and masks it with the interrupts that are actually enabled. This is useful for inside ISRs where the status of only the enabled interrupts needs to be checked.

## Parameters

<i>selectedPort</i>	<p>is the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_P3</li> <li>■ GPIO_PORT_P4</li> <li>■ GPIO_PORT_P5</li> <li>■ GPIO_PORT_P6</li> <li>■ GPIO_PORT_P7</li> <li>■ GPIO_PORT_P8</li> <li>■ GPIO_PORT_P9</li> <li>■ GPIO_PORT_P10</li> <li>■ GPIO_PORT_P11</li> <li>■ GPIO_PORT_PJ</li> </ul>
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## Returns

Logical OR of any of the following:

- GPIO\_PIN0
- GPIO\_PIN1
- GPIO\_PIN2
- GPIO\_PIN3
- GPIO\_PIN4
- GPIO\_PIN5
- GPIO\_PIN6
- GPIO\_PIN7
- GPIO\_PIN8
- GPIO\_PIN9
- GPIO\_PIN10
- GPIO\_PIN11
- GPIO\_PIN12
- GPIO\_PIN13
- GPIO\_PIN14
- GPIO\_PIN15,
- PIN\_ALL8,
- PIN\_ALL16

indicating the interrupt status of the selected pins [Default: 0]

References [GPIO\\_getInterruptStatus\(\)](#).

10.4.2.5 `uint8_t GPIO_getInputPinValue ( uint_fast8_t selectedPort, uint_fast16_t selectedPins )`

This function gets the input value on the selected pin.

This function gets the input value on the selected pin.

## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
<i>selectedPins</i>	is the specified pin in the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PIN0</li><li>■ GPIO_PIN1</li><li>■ GPIO_PIN2</li><li>■ GPIO_PIN3</li><li>■ GPIO_PIN4</li><li>■ GPIO_PIN5</li><li>■ GPIO_PIN6</li><li>■ GPIO_PIN7</li><li>■ GPIO_PIN8</li><li>■ GPIO_PIN9</li><li>■ GPIO_PIN10</li><li>■ GPIO_PIN11</li><li>■ GPIO_PIN12</li><li>■ GPIO_PIN13</li><li>■ GPIO_PIN14</li><li>■ GPIO_PIN15</li></ul>

**Returns**

One of the following:

- **GPIO\_INPUT\_PIN\_HIGH**
- **GPIO\_INPUT\_PIN\_LOW**  
indicating the status of the pin

#### 10.4.2.6 `uint_fast16_t GPIO_getInterruptStatus ( uint_fast8_t selectedPort, uint_fast16_t selectedPins )`

This function gets the interrupt status of the selected pin.

This function gets the interrupt status of the selected pin. Note that only Port 1, 2, A have this capability.

**Parameters**

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ <b>GPIO_PORT_P1</b></li> <li>■ <b>GPIO_PORT_P2</b></li> <li>■ <b>GPIO_PORT_PA</b></li> </ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ <b>GPIO_PIN0</b></li> <li>■ <b>GPIO_PIN1</b></li> <li>■ <b>GPIO_PIN2</b></li> <li>■ <b>GPIO_PIN3</b></li> <li>■ <b>GPIO_PIN4</b></li> <li>■ <b>GPIO_PIN5</b></li> <li>■ <b>GPIO_PIN6</b></li> <li>■ <b>GPIO_PIN7</b></li> <li>■ <b>GPIO_PIN8</b></li> <li>■ <b>GPIO_PIN9</b></li> <li>■ <b>GPIO_PIN10</b></li> <li>■ <b>GPIO_PIN11</b></li> <li>■ <b>GPIO_PIN12</b></li> <li>■ <b>GPIO_PIN13</b></li> <li>■ <b>GPIO_PIN14</b></li> <li>■ <b>GPIO_PIN15</b></li> </ul>

**Returns**

Logical OR of any of the following:

- **GPIO\_PIN0**
- **GPIO\_PIN1**
- **GPIO\_PIN2**

- GPIO\_PIN3
- GPIO\_PIN4
- GPIO\_PIN5
- GPIO\_PIN6
- GPIO\_PIN7
- GPIO\_PIN8
- GPIO\_PIN9
- GPIO\_PIN10
- GPIO\_PIN11
- GPIO\_PIN12
- GPIO\_PIN13
- GPIO\_PIN14
- GPIO\_PIN15

indicating the interrupt status of the selected pins [Default: 0]

Referenced by [GPIO\\_getEnabledInterruptStatus\(\)](#).

#### 10.4.2.7 void GPIO\_interruptEdgeSelect ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins*, uint\_fast8\_t *edgeSelect* )

This function selects on what edge the port interrupt flag should be set for a transition.

This function selects on what edge the port interrupt flag should be set for a transition. Values for *edgeSelect* should be GPIO\_LOW\_TO\_HIGH\_TRANSITION or GPIO\_HIGH\_TO\_LOW\_TRANSITION.

##### Parameters

<i>selectedPort</i>	<p>is the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_P3</li> <li>■ GPIO_PORT_P4</li> <li>■ GPIO_PORT_P5</li> <li>■ GPIO_PORT_P6</li> <li>■ GPIO_PORT_P7</li> <li>■ GPIO_PORT_P8</li> <li>■ GPIO_PORT_P9</li> <li>■ GPIO_PORT_P10</li> <li>■ GPIO_PORT_P11</li> <li>■ GPIO_PORT_PJ</li> </ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>
<i>edgeSelect</i>	<p>specifies what transition sets the interrupt flag Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_HIGH_TO_LOW_TRANSITION</li> <li>■ GPIO_LOW_TO_HIGH_TRANSITION</li> </ul>

Modified bits of **PxIES** register.

**Returns**

None

10.4.2.8 void GPIO\_registerInterrupt ( uint\_fast8\_t *selectedPort*, void(\*)(void) *intHandler* )

Registers an interrupt handler for the port interrupt.

**Parameters**

<i>selectedPort</i>	is the port to register the interrupt handler
<i>intHandler</i>	is a pointer to the function to be called when the port interrupt occurs.

This function registers the handler to be called when a port interrupt occurs. This function enables the global interrupt in the interrupt controller; specific GPIO interrupts must be enabled via [GPIO\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [GPIO\\_clearInterruptFlag\(\)](#).

Clock System can generate interrupts when

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.



**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

10.4.2.9 void GPIO\_setAsInputPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function configures the selected Pin as input pin.

This function selected pins on a selected port as input pins.

## Parameters

<i>selectedPort</i>	<p>is the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_P3</li> <li>■ GPIO_PORT_P4</li> <li>■ GPIO_PORT_P5</li> <li>■ GPIO_PORT_P6</li> <li>■ GPIO_PORT_P7</li> <li>■ GPIO_PORT_P8</li> <li>■ GPIO_PORT_P9</li> <li>■ GPIO_PORT_P10</li> <li>■ GPIO_PORT_P11</li> <li>■ GPIO_PORT_PJ</li> </ul>
<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>

Modified bits of **PxDIR** register, bits of **PxREN** register and bits of **PxSEL** register.

**Returns**

None

10.4.2.10 void GPIO\_setAsInputPinWithPullDownResistor ( uint\_fast8\_t *selectedPort*,  
uint\_fast16\_t *selectedPins* )

This function sets the selected Pin in input Mode with Pull Down resistor.

This function sets the selected Pin in input Mode with Pull Down resistor.

**Parameters**

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>
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Modified bits of **PxDIR** register, bits of **PxOUT** register and bits of **PxREN** register.

**Returns**

None

10.4.2.11 void GPIO\_setAsInputPinWithPullUpResistor ( uint\_fast8\_t *selectedPort*,  
uint\_fast16\_t *selectedPins* )

This function sets the selected Pin in input Mode with Pull Up resistor.

This function sets the selected Pin in input Mode with Pull Up resistor.

## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"><li>■ GPIO_PIN0</li><li>■ GPIO_PIN1</li><li>■ GPIO_PIN2</li><li>■ GPIO_PIN3</li><li>■ GPIO_PIN4</li><li>■ GPIO_PIN5</li><li>■ GPIO_PIN6</li><li>■ GPIO_PIN7</li><li>■ GPIO_PIN8</li><li>■ GPIO_PIN9</li><li>■ GPIO_PIN10</li><li>■ GPIO_PIN11</li><li>■ GPIO_PIN12</li><li>■ GPIO_PIN13</li><li>■ GPIO_PIN14</li><li>■ GPIO_PIN15</li></ul>

Modified bits of **PxDIR** register, bits of **PxOUT** register and bits of **PxREN** register.

**Returns**

None

10.4.2.12 void GPIO\_setAsOutputPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function configures the selected Pin as output pin.

This function selected pins on a selected port as output pins.

**Parameters**

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>
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Modified bits of **PxDIR** register and bits of **PxSEL** register.

**Returns**

None

10.4.2.13 void GPIO\_setAsPeripheralModuleFunctionInputPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins*, uint\_fast8\_t *mode* )

This function configures the peripheral module function in the input direction for the selected pin for either primary, secondary or ternary module function modes.

This function configures the peripheral module function in the input direction for the selected pin for either primary, secondary or ternary module function modes. Accepted values for mode are GPIO\_PRIMARY\_MODULE\_FUNCTION, GPIO\_SECONDARY\_MODULE\_FUNCTION, and GPIO\_TERTIARY\_MODULE\_FUNCTION

## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"><li>■ GPIO_PIN0</li><li>■ GPIO_PIN1</li><li>■ GPIO_PIN2</li><li>■ GPIO_PIN3</li><li>■ GPIO_PIN4</li><li>■ GPIO_PIN5</li><li>■ GPIO_PIN6</li><li>■ GPIO_PIN7</li><li>■ GPIO_PIN8</li><li>■ GPIO_PIN9</li><li>■ GPIO_PIN10</li><li>■ GPIO_PIN11</li><li>■ GPIO_PIN12</li><li>■ GPIO_PIN13</li><li>■ GPIO_PIN14</li><li>■ GPIO_PIN15</li></ul>



<i>mode</i>	is the specified mode that the pin should be configured for the module function. Valid values are: <ul style="list-style-type: none"> <li>■ <b>GPIO_PRIMARY_MODULE_FUNCTION</b></li> <li>■ <b>GPIO_SECONDARY_MODULE_FUNCTION</b></li> <li>■ <b>GPIO_TERTIARY_MODULE_FUNCTION</b></li> </ul>
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Modified bits of **PxDIR** register and bits of **PxSEL** register.

#### Returns

None

10.4.2.14 void GPIO\_setAsPeripheralModuleFunctionOutputPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins*, uint\_fast8\_t *mode* )

This function configures the peripheral module function in the output direction for the selected pin for either primary, secondary or ternary module function modes.

This function configures the peripheral module function in the output direction for the selected pin for either primary, secondary or ternary module function modes. Accepted values for mode are GPIO\_PRIMARY\_MODULE\_FUNCTION, GPIO\_SECONDARY\_MODULE\_FUNCTION, and GPIO\_TERTIARY\_MODULE\_FUNCTION

#### Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ <b>GPIO_PORT_P1</b></li> <li>■ <b>GPIO_PORT_P2</b></li> <li>■ <b>GPIO_PORT_P3</b></li> <li>■ <b>GPIO_PORT_P4</b></li> <li>■ <b>GPIO_PORT_P5</b></li> <li>■ <b>GPIO_PORT_P6</b></li> <li>■ <b>GPIO_PORT_P7</b></li> <li>■ <b>GPIO_PORT_P8</b></li> <li>■ <b>GPIO_PORT_P9</b></li> <li>■ <b>GPIO_PORT_P10</b></li> <li>■ <b>GPIO_PORT_P11</b></li> <li>■ <b>GPIO_PORT_PJ</b></li> </ul>
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<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"><li>■ GPIO_PIN0</li><li>■ GPIO_PIN1</li><li>■ GPIO_PIN2</li><li>■ GPIO_PIN3</li><li>■ GPIO_PIN4</li><li>■ GPIO_PIN5</li><li>■ GPIO_PIN6</li><li>■ GPIO_PIN7</li><li>■ GPIO_PIN8</li><li>■ GPIO_PIN9</li><li>■ GPIO_PIN10</li><li>■ GPIO_PIN11</li><li>■ GPIO_PIN12</li><li>■ GPIO_PIN13</li><li>■ GPIO_PIN14</li><li>■ GPIO_PIN15</li></ul>
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<i>mode</i>	is the specified mode that the pin should be configured for the module function. Valid values are: <ul style="list-style-type: none"> <li>■ <b>GPIO_PRIMARY_MODULE_FUNCTION</b></li> <li>■ <b>GPIO_SECONDARY_MODULE_FUNCTION</b></li> <li>■ <b>GPIO_TERTIARY_MODULE_FUNCTION</b></li> </ul>
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Modified bits of **PxDIR** register and bits of **PxSEL** register.

**Returns**

None

10.4.2.15 void GPIO\_setDriveStrengthHigh ( uint\_fast8\_t *selectedPort*, uint\_fast8\_t *selectedPins* )

This function sets the drive strength to high for the selected port

**Parameters**

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"> <li>■ <b>GPIO_PORT_P1,</b></li> <li>■ <b>GPIO_PORT_P2,</b></li> <li>■ <b>GPIO_PORT_P3,</b></li> <li>■ <b>GPIO_PORT_P4,</b></li> <li>■ <b>GPIO_PORT_P5,</b></li> <li>■ <b>GPIO_PORT_P6,</b></li> <li>■ <b>GPIO_PORT_P7,</b></li> <li>■ <b>GPIO_PORT_P8,</b></li> <li>■ <b>GPIO_PORT_P9,</b></li> <li>■ <b>GPIO_PORT_P10,</b></li> <li>■ <b>GPIO_PORT_PJ</b></li> </ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0,</li> <li>■ GPIO_PIN1,</li> <li>■ GPIO_PIN2,</li> <li>■ GPIO_PIN3,</li> <li>■ GPIO_PIN4,</li> <li>■ GPIO_PIN5,</li> <li>■ GPIO_PIN6,</li> <li>■ GPIO_PIN7,</li> <li>■ GPIO_PIN8,</li> <li>■ PIN_ALL8,</li> </ul>
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**Returns**

None

10.4.2.16 void GPIO\_setDriveStrengthLow ( uint\_fast8\_t *selectedPort*, uint\_fast8\_t *selectedPins* )

This function sets the drive strength to low for the selected port

**Parameters**

<i>selectedPort</i>	<p>is the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1,</li> <li>■ GPIO_PORT_P2,</li> <li>■ GPIO_PORT_P3,</li> <li>■ GPIO_PORT_P4,</li> <li>■ GPIO_PORT_P5,</li> <li>■ GPIO_PORT_P6,</li> <li>■ GPIO_PORT_P7,</li> <li>■ GPIO_PORT_P8,</li> <li>■ GPIO_PORT_P9,</li> <li>■ GPIO_PORT_P10,</li> <li>■ GPIO_PORT_PJ</li> </ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0,</li> <li>■ GPIO_PIN1,</li> <li>■ GPIO_PIN2,</li> <li>■ GPIO_PIN3,</li> <li>■ GPIO_PIN4,</li> <li>■ GPIO_PIN5,</li> <li>■ GPIO_PIN6,</li> <li>■ GPIO_PIN7,</li> <li>■ GPIO_PIN8,</li> <li>■ PIN_ALL8,</li> </ul>
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**Returns**

None

10.4.2.17 void GPIO\_setOutputHighOnPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function sets output HIGH on the selected Pin.

This function sets output HIGH on the selected port's pin.

**Parameters**

<i>selectedPort</i>	<p>is the selected port. Valid values are:</p> <ul style="list-style-type: none"> <li>■ GPIO_PORT_P1</li> <li>■ GPIO_PORT_P2</li> <li>■ GPIO_PORT_P3</li> <li>■ GPIO_PORT_P4</li> <li>■ GPIO_PORT_P5</li> <li>■ GPIO_PORT_P6</li> <li>■ GPIO_PORT_P7</li> <li>■ GPIO_PORT_P8</li> <li>■ GPIO_PORT_P9</li> <li>■ GPIO_PORT_P10</li> <li>■ GPIO_PORT_P11</li> <li>■ GPIO_PORT_PJ</li> </ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>
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Modified bits of **PxOUT** register.

**Returns**

None

10.4.2.18 void GPIO\_setOutputLowOnPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function sets output LOW on the selected Pin.

This function sets output LOW on the selected port's pin.

## Parameters

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
<i>selectedPins</i>	is the specified pin in the selected port. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"><li>■ GPIO_PIN0</li><li>■ GPIO_PIN1</li><li>■ GPIO_PIN2</li><li>■ GPIO_PIN3</li><li>■ GPIO_PIN4</li><li>■ GPIO_PIN5</li><li>■ GPIO_PIN6</li><li>■ GPIO_PIN7</li><li>■ GPIO_PIN8</li><li>■ GPIO_PIN9</li><li>■ GPIO_PIN10</li><li>■ GPIO_PIN11</li><li>■ GPIO_PIN12</li><li>■ GPIO_PIN13</li><li>■ GPIO_PIN14</li><li>■ GPIO_PIN15</li></ul>

**Returns**  
None

10.4.2.19 void GPIO\_toggleOutputOnPin ( uint\_fast8\_t *selectedPort*, uint\_fast16\_t *selectedPins* )

This function toggles the output on the selected Pin.

This function toggles the output on the selected port's pin.

**Parameters**

<i>selectedPort</i>	is the selected port. Valid values are: <ul style="list-style-type: none"><li>■ GPIO_PORT_P1</li><li>■ GPIO_PORT_P2</li><li>■ GPIO_PORT_P3</li><li>■ GPIO_PORT_P4</li><li>■ GPIO_PORT_P5</li><li>■ GPIO_PORT_P6</li><li>■ GPIO_PORT_P7</li><li>■ GPIO_PORT_P8</li><li>■ GPIO_PORT_P9</li><li>■ GPIO_PORT_P10</li><li>■ GPIO_PORT_P11</li><li>■ GPIO_PORT_PJ</li></ul>
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<i>selectedPins</i>	<p>is the specified pin in the selected port. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ GPIO_PIN0</li> <li>■ GPIO_PIN1</li> <li>■ GPIO_PIN2</li> <li>■ GPIO_PIN3</li> <li>■ GPIO_PIN4</li> <li>■ GPIO_PIN5</li> <li>■ GPIO_PIN6</li> <li>■ GPIO_PIN7</li> <li>■ GPIO_PIN8</li> <li>■ GPIO_PIN9</li> <li>■ GPIO_PIN10</li> <li>■ GPIO_PIN11</li> <li>■ GPIO_PIN12</li> <li>■ GPIO_PIN13</li> <li>■ GPIO_PIN14</li> <li>■ GPIO_PIN15</li> </ul>
---------------------	--

Modified bits of **PxOUT** register.

**Returns**

None

#### 10.4.2.20 void GPIO\_unregisterInterrupt ( uint\_fast8\_t *selectedPort* )

Unregisters the interrupt handler for the port.

**Parameters**

<i>selectedPort</i>	is the port to unregister the interrupt handler
---------------------	---

This function unregisters the handler to be called when a port interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 11 Inter-Integrated Circuit (I2C)

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## 11.1 I2C Module Operation

In I2C mode, the eUSCI\_B module provides an interface between the device and I2C-compatible devices connected by the two-wire I2C serial bus. External components attached to the I2C bus serially transmit and/or receive serial data to/from the eUSCI\_B module through the 2-wire I2C interface. The Inter-Integrated Circuit (I2C) API provides a set of functions for using the MSPWare I2C modules. Functions are provided to initialize the I2C modules, to send and receive data, obtain status, and to manage interrupts for the I2C modules. For the sake of simplicity and code readability, the EUSCI\_B module name has been omitted from the API name space.

The I2C module provide the ability to communicate to other IC devices over an I2C bus. The I2C bus is specified to support devices that can both transmit and receive (write and read) data. Also, devices on the I2C bus can be designated as either a master or a slave. The MSPWare L I2C modules support both sending and receiving data as either a master or a slave, and also support the simultaneous operation as both a master and a slave.

I2C module can generate interrupts. The I2C module configured as a master will generate interrupts when a transmit or receive operation is completed (or aborted due to an error). The I2C module configured as a slave will generate interrupts when data has been sent or requested by a master.

## 11.2 Master Operation

To drive the master module, the APIs need to be invoked in the following order

- **I2C\_initMaster**
- **I2C\_setSlaveAddress**
- **I2C\_setMode**
- **I2C\_enableModule**
- **I2C\_enableInterrupt** ( if interrupts are being used ) This may be followed by the APIs for transmit or receive as required

The user must first initialize the I2C module and configure it as a master with a call to `I2C_initMaster` . That function will set the clock and data rates. This is followed by a call to set the slave address with which the master intends to communicate with using `I2C_setSlaveAddress` . Then the mode of operation (transmit or receive) is chosen using `I2C_setMode` . The I2C module may now be enabled using `I2C_enableModule` . It is recommended to enable the I2C module before enabling the interrupts. Any transmission or reception of data may be initiated at this point after interrupts are enabled (if any).

The transaction can then be initiated on the bus by calling the transmit or receive related APIs as listed below.

#### **Master Single Byte Transmission**

- I2C\_masterSendSingleByte

#### **Master Multiple Byte Transmission**

- I2C\_masterSendMultiByteStart
- I2C\_masterSendMultiByteNext
- I2C\_masterSendMultiByteStop

#### **Master Single Byte Reception**

- I2C\_masterReceiveSingleByte

#### **Master Multiple Byte Reception**

- I2C\_masterReceiveStart
- I2C\_masterReceiveMultiByteNext
- I2C\_masterReceiveMultiByteFinish
- I2C\_masterReceiveMultiByteStop

For the interrupt-driven transaction, the user must register an interrupt handler for the I2C devices and enable the I2C interrupt.

## **11.3 Slave Operation**

To drive the slave module, the APIs need to be invoked in the following order

- **I2C\_initSlave**
- **I2C\_setMode**
- **I2C\_enableModule**
- **I2C\_enableInterrupt** ( if interrupts are being used )

The user must first call the I2C\_initSlave to initialize the slave module in I2C mode and set the slave address. This is followed by a call to set the mode of operation (transmit or receive). The I2C module may now be enabled using I2C\_enableModule . It is recommended to enable the I2C module before enabling the interrupts. Any transmission or reception of data may be initiated at this point after interrupts are enabled (if any).

The transaction can then be initiated on the bus by calling the transmit or receive related APIs as listed below.

#### **Slave Transmission API**

- I2C\_slavePutData

#### **Slave Reception API**

- I2C\_slaveGetData

For the interrupt-driven transaction, the user must register an interrupt handler for the I2C devices and enable the I2C interrupt.

## 11.4 Timeout Parameters

For serial transmission APIs (sending/receiving), a "timeout" API exists that will return control of execution back to the user application if a specified duration passes. The variable that is passed into these functions is a unit of time specified by how many "loop iterations" elapse before unsuccessful transmission of data.

## 11.5 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the I2C module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a simple example of how to setup the I2C module for master operation with a 400KHz clock.

First, below is an example of setting up the I2C module configuration structure:

```

/* I2C Master Configuration Parameter */
const eUSCI_I2C_MasterConfig i2cConfig =
{
    EUSCI_B_I2C_CLOCKSOURCE_SMCLK,           // SMCLK Clock Source
    3000000,                                  // SMCLK = 3MHz
    EUSCI_B_I2C_SET_DATA_RATE_400KBPS,      // Desired I2C Clock of 400khz
    0,                                        // No byte counter threshold
    EUSCI_B_I2C_NO_AUTO_STOP                 // No Autostop
};

```

Below are the actual DriverLib calls to configure/setup the I2C module:

```

/* Initializing I2C Master to SMCLK at 400kbs with no autostop */
MAP_I2C_initMaster(EUSCI_B0_BASE, &i2cConfig);

/* Specify slave address */
MAP_I2C_setSlaveAddress(EUSCI_B0_BASE, SLAVE_ADDRESS);

/* Set Master in transmit mode */
MAP_I2C_setMode(EUSCI_B0_BASE, EUSCI_B_I2C_TRANSMIT_MODE);

/* Enable I2C Module to start operations */
MAP_I2C_enableModule(EUSCI_B0_BASE);

/* Enable and clear the interrupt flag */
MAP_I2C_clearInterruptFlag(EUSCI_B0_BASE,
    EUSCI_B_I2C_TRANSMIT_INTERRUPT0 + EUSCI_B_I2C_NAK_INTERRUPT);

/* Enable master transmit interrupt */
MAP_I2C_enableInterrupt(EUSCI_B0_BASE,
    EUSCI_B_I2C_TRANSMIT_INTERRUPT0 + EUSCI_B_I2C_NAK_INTERRUPT);
MAP_Interrupt_enableInterrupt(INT_EUSCI_B0);

```

## 11.6 Definitions

### Data Structures

- struct [\\_eUSCI\\_I2C\\_MasterConfig](#)

### Functions

- void [I2C\\_clearInterruptFlag](#) (uint32\_t moduleInstance, uint\_fast16\_t mask)
- void [I2C\\_disableInterrupt](#) (uint32\_t moduleInstance, uint\_fast16\_t mask)
- void [I2C\\_disableModule](#) (uint32\_t moduleInstance)
- void [I2C\\_disableMultiMasterMode](#) (uint32\_t moduleInstance)
- void [I2C\\_enableInterrupt](#) (uint32\_t moduleInstance, uint\_fast16\_t mask)
- void [I2C\\_enableModule](#) (uint32\_t moduleInstance)
- void [I2C\\_enableMultiMasterMode](#) (uint32\_t moduleInstance)
- uint\_fast16\_t [I2C\\_getEnabledInterruptStatus](#) (uint32\_t moduleInstance)
- uint\_fast16\_t [I2C\\_getInterruptStatus](#) (uint32\_t moduleInstance, uint16\_t mask)
- uint\_fast8\_t [I2C\\_getMode](#) (uint32\_t moduleInstance)
- uint32\_t [I2C\\_getReceiveBufferAddressForDMA](#) (uint32\_t moduleInstance)
- uint32\_t [I2C\\_getTransmitBufferAddressForDMA](#) (uint32\_t moduleInstance)
- void [I2C\\_initMaster](#) (uint32\_t moduleInstance, const eUSCI\_I2C\_MasterConfig \*config)
- void [I2C\\_initSlave](#) (uint32\_t moduleInstance, uint\_fast16\_t slaveAddress, uint\_fast8\_t slaveAddressOffset, uint32\_t slaveOwnAddressEnable)
- uint8\_t [I2C\\_isBusBusy](#) (uint32\_t moduleInstance)
- bool [I2C\\_masterIsStartSent](#) (uint32\_t moduleInstance)
- uint8\_t [I2C\\_masterIsStopSent](#) (uint32\_t moduleInstance)
- uint8\_t [I2C\\_masterReceiveMultiByteFinish](#) (uint32\_t moduleInstance)
- bool [I2C\\_masterReceiveMultiByteFinishWithTimeout](#) (uint32\_t moduleInstance, uint8\_t \*txData, uint32\_t timeout)
- uint8\_t [I2C\\_masterReceiveMultiByteNext](#) (uint32\_t moduleInstance)
- void [I2C\\_masterReceiveMultiByteStop](#) (uint32\_t moduleInstance)
- uint8\_t [I2C\\_masterReceiveSingle](#) (uint32\_t moduleInstance)
- uint8\_t [I2C\\_masterReceiveSingleByte](#) (uint32\_t moduleInstance)
- void [I2C\\_masterReceiveStart](#) (uint32\_t moduleInstance)
- void [I2C\\_masterSendMultiByteFinish](#) (uint32\_t moduleInstance, uint8\_t txData)
- bool [I2C\\_masterSendMultiByteFinishWithTimeout](#) (uint32\_t moduleInstance, uint8\_t txData, uint32\_t timeout)
- void [I2C\\_masterSendMultiByteNext](#) (uint32\_t moduleInstance, uint8\_t txData)
- bool [I2C\\_masterSendMultiByteNextWithTimeout](#) (uint32\_t moduleInstance, uint8\_t txData, uint32\_t timeout)
- void [I2C\\_masterSendMultiByteStart](#) (uint32\_t moduleInstance, uint8\_t txData)
- bool [I2C\\_masterSendMultiByteStartWithTimeout](#) (uint32\_t moduleInstance, uint8\_t txData, uint32\_t timeout)
- void [I2C\\_masterSendMultiByteStop](#) (uint32\_t moduleInstance)
- bool [I2C\\_masterSendMultiByteStopWithTimeout](#) (uint32\_t moduleInstance, uint32\_t timeout)
- void [I2C\\_masterSendSingleByte](#) (uint32\_t moduleInstance, uint8\_t txData)
- bool [I2C\\_masterSendSingleByteWithTimeout](#) (uint32\_t moduleInstance, uint8\_t txData, uint32\_t timeout)
- void [I2C\\_masterSendStart](#) (uint32\_t moduleInstance)
- void [I2C\\_registerInterrupt](#) (uint32\_t moduleInstance, void(\*intHandler)(void))
- void [I2C\\_setMode](#) (uint32\_t moduleInstance, uint\_fast8\_t mode)
- void [I2C\\_setSlaveAddress](#) (uint32\_t moduleInstance, uint\_fast16\_t slaveAddress)
- uint8\_t [I2C\\_slaveGetData](#) (uint32\_t moduleInstance)
- void [I2C\\_slavePutData](#) (uint32\_t moduleInstance, uint8\_t transmitData)
- void [I2C\\_slaveSendNAK](#) (uint32\_t moduleInstance)
- void [I2C\\_unregisterInterrupt](#) (uint32\_t moduleInstance)

## 11.6.1 Detailed Description

The code for this module is contained in `driverlib/i2c.c`, with `driverlib/i2c.h` containing the API declarations for use by applications.

## 11.6.2 Function Documentation

### 11.6.2.1 void I2C\_clearInterruptFlag ( uint32\_t *moduleInstance*, uint\_fast16\_t *mask* )

Clears I2C interrupt sources.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
<i>mask</i>	is a bit mask of the interrupt sources to be cleared.

The I2C interrupt source is cleared, so that it no longer asserts. The highest interrupt flag is automatically cleared when an interrupt vector generator is used.

The mask parameter has the same definition as the mask parameter to [I2C\\_enableInterrupt\(\)](#).

Modified register is **UCBxIFG**.

#### Returns

None.

### 11.6.2.2 void I2C\_disableInterrupt ( uint32\_t *moduleInstance*, uint\_fast16\_t *mask* )

Disables individual I2C interrupt sources.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	---

<i>mask</i>	is the bit mask of the interrupt sources to be disabled.
-------------	--

Disables the indicated I2C interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_B\_I2C\_STOP\_INTERRUPT** - STOP condition interrupt
- **EUSCI\_B\_I2C\_START\_INTERRUPT** - START condition interrupt
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT0** - Transmit interrupt0
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT1** - Transmit interrupt1
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT2** - Transmit interrupt2
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT3** - Transmit interrupt3
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT0** - Receive interrupt0
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT1** - Receive interrupt1
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT2** - Receive interrupt2
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT3** - Receive interrupt3
- **EUSCI\_B\_I2C\_NAK\_INTERRUPT** - Not-acknowledge interrupt
- **EUSCI\_B\_I2C\_ARBITRATIONLOST\_INTERRUPT** - Arbitration lost interrupt
- **EUSCI\_B\_I2C\_BIT9\_POSITION\_INTERRUPT** - Bit position 9 interrupt enable
- **EUSCI\_B\_I2C\_CLOCK\_LOW\_TIMEOUT\_INTERRUPT** - Clock low timeout interrupt enable
- **EUSCI\_B\_I2C\_BYTE\_COUNTER\_INTERRUPT** - Byte counter interrupt enable

Modified register is **UCBxIE**.

#### Returns

None.

### 11.6.2.3 void I2C\_disableModule ( uint32\_t *moduleInstance* )

Disables the I2C block.

#### Parameters

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

This will disable operation of the I2C block. Modified bits are **UCSWRST** of **UCBxCTL1** register.

#### Returns

None.



11.6.2.4 void I2C\_disableMultiMasterMode ( uint32\_t *moduleInstance* )

Disables Multi Master Mode

## Parameters

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

At the end of this function, the I2C module is still disabled till I2C\_enableModule is invoked

Modified bits are **UCSWRST** of **OFS\_UCBxCTLW0**, **UCMM** bit of **UCBxCTLW0**

## Returns

None.

### 11.6.2.5 void I2C\_enableInterrupt ( uint32\_t *moduleInstance*, uint\_fast16\_t *mask* )

Enables individual I2C interrupt sources.

## Parameters

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
<i>mask</i>	is the bit mask of the interrupt sources to be enabled.

Enables the indicated I2C interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_B\_I2C\_STOP\_INTERRUPT** - STOP condition interrupt
- **EUSCI\_B\_I2C\_START\_INTERRUPT** - START condition interrupt
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT0** - Transmit interrupt0
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT1** - Transmit interrupt1
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT2** - Transmit interrupt2
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT3** - Transmit interrupt3
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT0** - Receive interrupt0
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT1** - Receive interrupt1

- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT2** - Receive interrupt2
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT3** - Receive interrupt3
- **EUSCI\_B\_I2C\_NAK\_INTERRUPT** - Not-acknowledge interrupt
- **EUSCI\_B\_I2C\_ARBITRATIONLOST\_INTERRUPT** - Arbitration lost interrupt
- **EUSCI\_B\_I2C\_BIT9\_POSITION\_INTERRUPT** - Bit position 9 interrupt enable
- **EUSCI\_B\_I2C\_CLOCK\_LOW\_TIMEOUT\_INTERRUPT** - Clock low timeout interrupt enable
- **EUSCI\_B\_I2C\_BYTE\_COUNTER\_INTERRUPT** - Byte counter interrupt enable

Modified registers are UCBxIFG and OFS\_UCBxIE.

**Returns**

None.

### 11.6.2.6 void I2C\_enableModule ( uint32\_t *moduleInstance* )

Enables the I2C block.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

This will enable operation of the I2C block. Modified bits are **UCSWRST** of **UCBxCTL1** register.

**Returns**

None.

### 11.6.2.7 void I2C\_enableMultiMasterMode ( uint32\_t *moduleInstance* )

Enables Multi Master Mode

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

At the end of this function, the I2C module is still disabled till I2C\_enableModule is invoked  
Modified bits are **UCSWRST** of **OFS\_UCBxCTLW0**, **UCMM** bit of **UCBxCTLW0**

#### Returns

None.

### 11.6.2.8 uint\_fast16\_t I2C\_getEnabledInterruptStatus ( uint32\_t *moduleInstance* )

Gets the current I2C interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

#### Parameters

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

#### Returns

the masked status of the interrupt flag

- **EUSCI\_B\_I2C\_STOP\_INTERRUPT** - STOP condition interrupt
- **EUSCI\_B\_I2C\_START\_INTERRUPT** - START condition interrupt
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT0** - Transmit interrupt0
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT1** - Transmit interrupt1
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT2** - Transmit interrupt2
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT3** - Transmit interrupt3
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT0** - Receive interrupt0
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT1** - Receive interrupt1
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT2** - Receive interrupt2
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT3** - Receive interrupt3
- **EUSCI\_B\_I2C\_NAK\_INTERRUPT** - Not-acknowledge interrupt
- **EUSCI\_B\_I2C\_ARBITRATIONLOST\_INTERRUPT** - Arbitration lost interrupt
- **EUSCI\_B\_I2C\_BIT9\_POSITION\_INTERRUPT** - Bit position 9 interrupt enable
- **EUSCI\_B\_I2C\_CLOCK\_LOW\_TIMEOUT\_INTERRUPT** - Clock low timeout interrupt enable
- **EUSCI\_B\_I2C\_BYTE\_COUNTER\_INTERRUPT** - Byte counter interrupt enable

References [I2C\\_getInterruptStatus\(\)](#).

### 11.6.2.9 uint\_fast16\_t I2C\_getInterruptStatus ( uint32\_t *moduleInstance*, uint16\_t *mask* )

Gets the current I2C interrupt status.

## Parameters

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
<i>mask</i>	<p>is the masked interrupt flag status to be returned. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_NAK_INTERRUPT</b> - Not-acknowledge interrupt</li> <li>■ <b>EUSCI_B_I2C_ARBITRATIONLOST_INTERRUPT</b> - Arbitration lost interrupt</li> <li>■ <b>EUSCI_B_I2C_STOP_INTERRUPT</b> - STOP condition interrupt</li> <li>■ <b>EUSCI_B_I2C_START_INTERRUPT</b> - START condition interrupt</li> <li>■ <b>EUSCI_B_I2C_TRANSMIT_INTERRUPT0</b> - Transmit interrupt0</li> <li>■ <b>EUSCI_B_I2C_TRANSMIT_INTERRUPT1</b> - Transmit interrupt1</li> <li>■ <b>EUSCI_B_I2C_TRANSMIT_INTERRUPT2</b> - Transmit interrupt2</li> <li>■ <b>EUSCI_B_I2C_TRANSMIT_INTERRUPT3</b> - Transmit interrupt3</li> <li>■ <b>EUSCI_B_I2C_RECEIVE_INTERRUPT0</b> - Receive interrupt0</li> <li>■ <b>EUSCI_B_I2C_RECEIVE_INTERRUPT1</b> - Receive interrupt1</li> <li>■ <b>EUSCI_B_I2C_RECEIVE_INTERRUPT2</b> - Receive interrupt2</li> <li>■ <b>EUSCI_B_I2C_RECEIVE_INTERRUPT3</b> - Receive interrupt3</li> <li>■ <b>EUSCI_B_I2C_BIT9_POSITION_INTERRUPT</b> - Bit position 9 interrupt</li> <li>■ <b>EUSCI_B_I2C_CLOCK_LOW_TIMEOUT_INTERRUPT</b> - Clock low timeout interrupt enable</li> <li>■ <b>EUSCI_B_I2C_BYTE_COUNTER_INTERRUPT</b> - Byte counter interrupt enable</li> </ul>

**Returns**

the masked status of the interrupt flag

- **EUSCI\_B\_I2C\_STOP\_INTERRUPT** - STOP condition interrupt
- **EUSCI\_B\_I2C\_START\_INTERRUPT** - START condition interrupt
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT0** - Transmit interrupt0
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT1** - Transmit interrupt1
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT2** - Transmit interrupt2
- **EUSCI\_B\_I2C\_TRANSMIT\_INTERRUPT3** - Transmit interrupt3
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT0** - Receive interrupt0
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT1** - Receive interrupt1
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT2** - Receive interrupt2
- **EUSCI\_B\_I2C\_RECEIVE\_INTERRUPT3** - Receive interrupt3
- **EUSCI\_B\_I2C\_NAK\_INTERRUPT** - Not-acknowledge interrupt
- **EUSCI\_B\_I2C\_ARBITRATIONLOST\_INTERRUPT** - Arbitration lost interrupt
- **EUSCI\_B\_I2C\_BIT9\_POSITION\_INTERRUPT** - Bit position 9 interrupt enable
- **EUSCI\_B\_I2C\_CLOCK\_LOW\_TIMEOUT\_INTERRUPT** - Clock low timeout interrupt enable
- **EUSCI\_B\_I2C\_BYTE\_COUNTER\_INTERRUPT** - Byte counter interrupt enable

Referenced by [I2C\\_getEnabledInterruptStatus\(\)](#).

### 11.6.2.10 uint\_fast8\_t I2C\_getMode ( uint32\_t moduleInstance )

Gets the mode of the I2C device.

Current I2C transmit/receive mode.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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Modified bits are **UCTR** of **UCBxCTL1** register.

**Returns**

None Return one of the following:

- **EUSCI\_B\_I2C\_TRANSMIT\_MODE**
  - **EUSCI\_B\_I2C\_RECEIVE\_MODE**
- indicating the current mode

11.6.2.11 uint32\_t I2C\_getReceiveBufferAddressForDMA ( uint32\_t *moduleInstance* )

Returns the address of the RX Buffer of the I2C for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

Returns the address of the I2C RX Buffer. This can be used in conjunction with the DMA to store the received data directly to memory.

**Returns**

NONE

11.6.2.12 `uint32_t I2C_getTransmitBufferAddressForDMA ( uint32_t moduleInstance )`

Returns the address of the TX Buffer of the I2C for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

Returns the address of the I2C TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Returns**

NONE

11.6.2.13 `void I2C_initMaster ( uint32_t moduleInstance, const eUSCI_I2C_MasterConfig * config )`

Initializes the I2C Master block.



## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>config</i>	Configuration structure for I2C master mode

**Configuration options for eUSCI\_I2C\_MasterConfig structure.**

## Parameters

<i>selectClockSource</i>	is the clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_CLOCKSOURCE_ACLK</b></li> <li>■ <b>EUSCI_B_I2C_CLOCKSOURCE_SMCLK</b></li> </ul>
<i>i2cClk</i>	is the rate of the clock supplied to the I2C module (the frequency in Hz of the clock source specified in selectClockSource).
<i>dataRate</i>	set up for selecting data transfer rate. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_SET_DATA_RATE_1MBPS</b></li> <li>■ <b>EUSCI_B_I2C_SET_DATA_RATE_400KBPS</b></li> <li>■ <b>EUSCI_B_I2C_SET_DATA_RATE_100KBPS</b></li> </ul>
<i>byteCounterThreshold</i>	sets threshold for automatic STOP or UCSTPIFG
<i>autoSTOPGeneration</i>	sets up the STOP condition generation. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_NO_AUTO_STOP</b></li> <li>■ <b>EUSCI_B_I2C_SET_BYTECOUNT_THRESHOLD_FLAG</b></li> <li>■ <b>EUSCI_B_I2C_SEND_STOP_AUTOMATICALLY_ON_BYTECOUNT_THRESHOLD</b></li> </ul>

This function initializes operation of the I2C Master block. Upon successful initialization of the I2C block, this function will have set the bus speed for the master; however I2C module is still disabled till I2C\_enableModule is invoked

Modified bits are **UCMST**, **UCMODE\_3**, **UCSYNC** of **UCBxCTL0** register **UCSSELx**, **UCSWRST**, of **UCBxCTL1** register **UCBxBR0** and **UCBxBR1** registers

**Returns**

None.

11.6.2.14 void I2C\_initSlave ( uint32\_t *moduleInstance*, uint\_fast16\_t *slaveAddress*,  
uint\_fast8\_t *slaveAddressOffset*, uint32\_t *slaveOwnAddressEnable* )

Initializes the I2C Slave block.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>slaveAddress</i>	7-bit or 10-bit slave address
<i>slaveAddressOffset</i>	Own address Offset referred to- 'x' value of UCBxI2COAx. Valid values are: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_OFFSET0,</b></li> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_OFFSET1,</b></li> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_OFFSET2,</b></li> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_OFFSET3</b></li> </ul>
<i>slaveOwnAddressEnable</i>	selects if the specified address is enabled or disabled. Valid values are: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_DISABLE,</b></li> <li>■ <b>EUSCI_B_I2C_OWN_ADDRESS_ENABLE</b></li> </ul>

This function initializes operation of the I2C as a Slave mode. Upon successful initialization of the I2C blocks, this function will have set the slave address but the I2C module is still disabled till I2C\_enableModule is invoked.

The parameter slaveAddress is the value that will be compared against the slave address sent by an I2C master.

Modified bits are **UCMODE\_3**, **UCSYNC** of **UCBxCTL0** register **UCSWRST** of **UCBxCTL1** register **UCBxI2COA** register

**Returns**

None.

### 11.6.2.15 uint8\_t I2C\_isBusBusy ( uint32\_t moduleInstance )

Indicates whether or not the I2C bus is busy.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function returns an indication of whether or not the I2C bus is busy. This function checks the status of the bus via UCBBUSY bit in UCBxSTAT register.

**Returns**

Returns EUSCI\_B\_I2C\_BUS\_BUSY if the I2C Master is busy; otherwise, returns EUSCI\_B\_I2C\_BUS\_NOT\_BUSY.

### 11.6.2.16 bool I2C\_masterIsStartSent ( uint32\_t *moduleInstance* )

Indicates whether Start got sent.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function returns an indication of whether or not Start got sent. This function checks the status of the bus via UCTXSTT bit in UCBxCTL1 register.

**Returns**

Returns true if the START has been sent, false if it is sending.

### 11.6.2.17 uint8\_t I2C\_masterIsStopSent ( uint32\_t *moduleInstance* )

Indicates whether STOP got sent.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function returns an indication of whether or not STOP got sent This function checks the status of the bus via UCTXSTP bit in UCBxCTL1 register.

**Returns**

Returns EUSCI\_B\_I2C\_STOP\_SEND\_COMPLETE if the I2C Master finished sending STOP; otherwise, returns EUSCI\_B\_I2C\_SENDING\_STOP.

### 11.6.2.18 uint8\_t I2C\_masterReceiveMultiByteFinish ( uint32\_t *moduleInstance* )

Finishes multi-byte reception at the Master end

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function is used by the Master module to initiate completion of a multi-byte reception This function

- Receives the current byte and initiates the STOP from Master to Slave

Modified bits are **UCTXSTP** bit of **UCBxCTL1**.

**Returns**

Received byte at Master end.

### 11.6.2.19 bool I2C\_masterReceiveMultiByteFinishWithTimeout ( uint32\_t *moduleInstance*, uint8\_t \* *txData*, uint32\_t *timeout* )

Finishes multi-byte reception at the Master end with timeout

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is a pointer to the location to store the received byte at master end
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module to initiate completion of a multi-byte reception This function

- Receives the current byte and initiates the STOP from Master to Slave

Modified bits are **UCTXSTP** bit of **UCBxCTL1**.

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.20 uint8\_t I2C\_masterReceiveMultiByteNext ( uint32\_t *moduleInstance* )

Starts multi-byte reception at the Master end one byte at a time

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
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This function is used by the Master module to receive each byte of a multi-byte reception This function reads currently received byte

Modified register is **UCBxRXBUF**.

**Returns**

Received byte at Master end.

### 11.6.2.21 void I2C\_masterReceiveMultiByteStop ( uint32\_t *moduleInstance* )

Sends the STOP at the end of a multi-byte reception at the Master end

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function is used by the Master module to initiate STOP

Modified bits are UCTXSTP bit of UCBxCTL1.

**Returns**

None.

### 11.6.2.22 uint8\_t I2C\_masterReceiveSingle ( uint32\_t *moduleInstance* )

Receives a byte that has been sent to the I2C Master Module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
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This function reads a byte of data from the I2C receive data Register.

**Returns**

Returns the byte received from by the I2C module, cast as an uint8\_t.

### 11.6.2.23 uint8\_t I2C\_masterReceiveSingleByte ( uint32\_t *moduleInstance* )

Does single byte reception from the slave

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

This function is used by the Master module to receive a single byte. This function:

- Sends START and STOP
- Waits for data reception
- Receives one byte from the Slave

Modified registers are **UCBxIE**, **UCBxCTL1**, **UCBxIFG**, **UCBxTXBUF**, **UCBxIE**

**Returns**

The byte that has been received from the slave

### 11.6.2.24 void I2C\_masterReceiveStart ( uint32\_t *moduleInstance* )

Starts reception at the Master end

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

This function is used by the Master module initiate reception of a single byte. This function

- Sends START



Modified bits are **UCTXSTT** bit of **UCBxCTL1**.

**Returns**

None.

### 11.6.2.25 void I2C\_masterSendMultiByteFinish ( uint32\_t *moduleInstance*, uint8\_t *txData* )

Finishes multi-byte transmission from Master to Slave

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the last data byte to be transmitted in a multi-byte transmission

This function is used by the Master module to send the last byte and STOP. This function

- Transmits the last data byte of a multi-byte transmission to the Slave
- Sends STOP

Modified registers are **UCBxTXBUF** and **UCBxCTL1**.

**Returns**

None.

### 11.6.2.26 bool I2C\_masterSendMultiByteFinishWithTimeout ( uint32\_t *moduleInstance*, uint8\_t *txData*, uint32\_t *timeout* )

Finishes multi-byte transmission from Master to Slave with timeout

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the last data byte to be transmitted in a multi-byte transmission
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module to send the last byte and STOP. This function

- Transmits the last data byte of a multi-byte transmission to the Slave
- Sends STOP

Modified registers are **UCBxTXBUF** and **UCBxCTL1**.

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.27 void I2C\_masterSendMultiByteNext ( uint32\_t *moduleInstance*, uint8\_t *txData* )

Continues multi-byte transmission from Master to Slave

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
<i>txData</i>	is the next data byte to be transmitted

This function is used by the Master module continue each byte of a multi-byte trasmission. This function

- Transmits each data byte of a multi-byte transmission to the Slave

Modified registers are **UCBxTXBUF**

**Returns**

None.

### 11.6.2.28 bool I2C\_masterSendMultiByteNextWithTimeout ( uint32\_t *moduleInstance*, uint8\_t *txData*, uint32\_t *timeout* )

Continues multi-byte transmission from Master to Slave with timeout

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the next data byte to be transmitted
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module continue each byte of a multi-byte transmission. This function

- Transmits each data byte of a multi-byte transmission to the Slave

Modified registers are **UCBxTXBUF**

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.29 void I2C\_masterSendMultiByteStart ( uint32\_t *moduleInstance*, uint8\_t *txData* )

Starts multi-byte transmission from Master to Slave

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the first data byte to be transmitted

This function is used by the Master module to send a single byte. This function

- Sends START
- Transmits the first data byte of a multi-byte transmission to the Slave

Modified registers are **UCBxIE**, **UCBxCTL1**, **UCBxIFG**, **UCBxTXBUF**, **UCBxIE**

**Returns**

None.

11.6.2.30 `bool I2C_masterSendMultiByteStartWithTimeout ( uint32_t moduleInstance,  
uint8_t txData, uint32_t timeout )`

Starts multi-byte transmission from Master to Slave with timeout

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the first data byte to be transmitted
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module to send a single byte. This function

- Sends START
- Transmits the first data byte of a multi-byte transmission to the Slave

Modified registers are **UCBxIE**, **UCBxCTL1**, **UCBxIFG**, **UCBxTXBUF**, **UCBxIE**

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.31 void I2C\_masterSendMultiByteStop ( uint32\_t *moduleInstance* )

Send STOP byte at the end of a multi-byte transmission from Master to Slave

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
-----------------------	--

This function is used by the Master module send STOP at the end of a multi-byte transmission

This function

- Send a STOP after current transmission is complete

Modified bits are **UCTXSTP** bit of **UCBxCTL1**.

**Returns**

None.

11.6.2.32 `bool I2C_masterSendMultiByteStopWithTimeout ( uint32_t moduleInstance,  
uint32_t timeout )`

Send STOP byte at the end of a multi-byte transmission from Master to Slave with timeout

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module send STOP at the end of a multi-byte transmission

This function

- Send a STOP after current transmission is complete

Modified bits are **UCTXSTP** bit of **UCBxCTL1**.

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.33 void I2C\_masterSendSingleByte ( uint32\_t moduleInstance, uint8\_t txData )

Does single byte transmission from Master to Slave

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the data byte to be transmitted

This function is used by the Master module to send a single byte. This function

- Sends START
- Transmits the byte to the Slave
- Sends STOP

Modified registers are **UCBxIE**, **UCBxCTL1**, **UCBxIFG**, **UCBxTXBUF**, **UCBxIE**

**Returns**

none

11.6.2.34 `bool I2C_masterSendSingleByteWithTimeout ( uint32_t moduleInstance, uint8_t txData, uint32_t timeout )`

Does single byte transmission from Master to Slave with timeout



**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>txData</i>	is the data byte to be transmitted
<i>timeout</i>	is the amount of time to wait until giving up

This function is used by the Master module to send a single byte. This function

- Sends START
- Transmits the byte to the Slave
- Sends STOP

Modified registers are **UCBxIE**, **UCBxCTL1**, **UCBxIFG**, **UCBxTXBUF**, **UCBxIE**

**Returns**

0x01 or 0x00URE of the transmission process.

### 11.6.2.35 void I2C\_masterSendStart ( uint32\_t *moduleInstance* )

This function is used by the Master module to initiate START

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
-----------------------	--

This function is used by the Master module to initiate STOP

Modified bits are UCTXSTT bit of UCBxCTLW0.

**Returns**

None.

11.6.2.36 void I2C\_registerInterrupt ( uint32\_t *moduleInstance*, void(\*)(void) *intHandler* )

Registers an interrupt handler for I2C interrupts.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>intHandler</i>	is a pointer to the function to be called when the timer capture compare interrupt occurs.

This function registers the handler to be called when an I2C interrupt occurs. This function enables the global interrupt in the interrupt controller; specific I2C interrupts must be enabled via [I2C\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [I2C\\_clearInterruptFlag\(\)](#).

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 11.6.2.37 void I2C\_setMode ( uint32\_t *moduleInstance*, uint\_fast8\_t *mode* )

Sets the mode of the I2C device

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>mode</i>	indicates whether module is in transmit/receive mode <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_I2C_TRANSMIT_MODE</b></li> <li>■ <b>EUSCI_B_I2C_RECEIVE_MODE</b> [Default value]</li> </ul>

Modified bits are **UCTR** of **UCBxCTL1** register

**Returns**

None.

### 11.6.2.38 void I2C\_setSlaveAddress ( uint32\_t *moduleInstance*, uint\_fast16\_t *slaveAddress* )

Sets the address that the I2C Master will place on the bus.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
<i>slaveAddress</i>	7-bit or 10-bit slave address

This function will set the address that the I2C Master will place on the bus when initiating a transaction. Modified register is **UCBxI2CSA** register

**Returns**

None.

### 11.6.2.39 uint8\_t I2C\_slaveGetData ( uint32\_t *moduleInstance* )

Receives a byte that has been sent to the I2C Module.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	---

This function reads a byte of data from the I2C receive data Register.

**Returns**

Returns the byte received from by the I2C module, cast as an uint8\_t. Modified bit is **UCBxRXBUF** register

11.6.2.40 void I2C\_slavePutData ( uint32\_t *moduleInstance*, uint8\_t *transmitData* )

Transmits a byte from the I2C Module.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
<i>transmitData</i>	data to be transmitted from the I2C module

This function will place the supplied data into I2C transmit data register to start transmission  
Modified register is **UCBxTXBUF** register

**Returns**

None.

#### 11.6.2.41 void I2C\_slaveSendNAK ( uint32\_t *moduleInstance* )

This function is used by the slave to send a NAK out over the I2C line

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.
-----------------------	--

**Returns**

None.

11.6.2.42 void I2C\_unregisterInterrupt ( uint32\_t *moduleInstance* )

Unregisters the interrupt handler for the timer

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI B (I2C) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</p>
-----------------------	--

This function unregisters the handler to be called when timer interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 12 Nested Vector Interrupt Controller (NVIC)

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## 12.1 Module Operation

The interrupt controller API provides a set of functions for dealing with the Nested Vectored Interrupt Controller (NVIC). Functions are provided to enable and disable interrupts, register interrupt handlers, and set the priority of interrupts.

The NVIC provides global interrupt masking, prioritization, and handler dispatching. Individual interrupt sources can be masked, and the processor interrupt can be globally masked as well (without affecting the individual source masks).

The NVIC is tightly coupled with the Cortex-M microprocessor. When the processor responds to an interrupt, the NVIC supplies the address of the function to handle the interrupt directly to the processor. This action eliminates the need for a global interrupt handler that queries the interrupt controller to determine the cause of the interrupt and branch to the appropriate handler, reducing interrupt response time.

The interrupt prioritization in the NVIC allows higher priority interrupts to be handled before lower priority interrupts, as well as allowing preemption of lower priority interrupt handlers by higher priority interrupts. Again, this helps reduce interrupt response time (for example, a 1 ms system control interrupt is not held off by the execution of a lower priority 1 second housekeeping interrupt handler).

Sub-prioritization is also possible; instead of having N bits of preemptable prioritization, the NVIC can be configured (via software) for N - M bits of preemptable prioritization and M bits of sub-priority. In this scheme, two interrupts with the same preemptable prioritization but different sub-priorities do not cause a preemption; tail chaining is used instead to process the two interrupts back-to-back.

If two interrupts with the same priority (and sub-priority if so configured) are asserted at the same time, the one with the lower interrupt number is processed first. The NVIC keeps track of the nesting of interrupt handlers, allowing the processor to return from interrupt context only once all nested and pending interrupts have been handled.

Interrupt handlers can be configured in one of two ways; statically at compile time or dynamically at run time. Static configuration of interrupt handlers is accomplished by editing the interrupt handler table in the application's startup code. When statically configured, the interrupts must be explicitly enabled in the NVIC via [Interrupt\\_enableInterrupt\(\)](#) before the processor can respond to the interrupt (in addition to any interrupt enabling required within the peripheral itself). Statically configuring the interrupt table provides the fastest interrupt response time because the stacking operation (a write to SRAM) can be performed in parallel with the interrupt handler table fetch (a read from Flash), as well as the prefetch of the interrupt handler itself (assuming it is also in Flash).

Alternatively, interrupts can be configured at run-time using [Interrupt\\_registerInterrupt\(\)](#). When using [Interrupt\\_registerInterrupt\(\)](#), the interrupt must also be enabled as before; when using the analogue in each individual driver, [Interrupt\\_enableInterrupt\(\)](#) is called by the driver and does not need to be called by the application. Run-time configuration of interrupts adds a small latency to



the interrupt response time because the stacking operation (a write to SRAM) and the interrupt handler table fetch (a read from SRAM) must be performed sequentially.

Run-time configuration of interrupt handlers requires that the interrupt handler table be placed on a 1-kB boundary in SRAM (typically this is at the beginning of SRAM). Failure to do so results in an incorrect vector address being fetched in response to an interrupt. The vector table is in a section called “vtable” and should be placed appropriately with a linker script.

## 12.2 Basic Operation Modes

The primary function of the interrupt controller API is to manage the interrupt vector table used by the NVIC to dispatch interrupt requests. Registering an interrupt handler is a simple matter of inserting the handler address into the table. By default, the table is filled with pointers to an internal handler that loops forever; it is an error for an interrupt to occur when there is no interrupt handler registered to process it. Therefore, interrupt sources should not be enabled before a handler has been registered, and interrupt sources should be disabled before a handler is unregistered. Interrupt handlers are managed with [Interrupt\\_registerInterrupt\(\)](#) and [Interrupt\\_unregisterInterrupt\(\)](#).

Each interrupt source can be individually enabled and disabled via [Interrupt\\_enableInterrupt\(\)](#) and [Interrupt\\_disableInterrupt\(\)](#). The processor interrupt can be enabled and disabled via [Interrupt\\_enableMaster\(\)](#) and [Interrupt\\_disableMaster\(\)](#); this does not affect the individual interrupt enable states. Masking of the processor interrupt can be used as a simple critical section (only an NMI can interrupt the processor while the processor interrupt is disabled), although masking the processor interrupt can have adverse effects on the interrupt response time.

The priority of each interrupt source can be set and examined via [Interrupt\\_setPriority\(\)](#) and [Interrupt\\_getPriority\(\)](#). The priority assignments are defined by the hardware; the upper N bits of the 8-bit priority are examined to determine the priority of an interrupt (for the MSP432 family, N is 3). This protocol allows priorities to be defined without knowledge of the exact number of supported priorities; moving to a device with more or fewer priority bits is made easier as the interrupt source continues to have a similar level of priority. Smaller priority numbers correspond to higher interrupt priority, so 0 is the highest priority.

## 12.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the Interrupt module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure interrupt priorities. For a set of more detailed code examples, please refer to the code examples in the examples/ directory of the MSPWare release:

```
/* Configuring interrupt priorities */
MAP_Interrupt_setPriority(INT_EUSCIB0, 0x20);
MAP_Interrupt_setPriority(INT_EUSCIA0, 0x40);
```

## 12.4 Definitions

### Functions

- void `Interrupt_disableInterrupt` (uint32\_t interruptNumber)
- bool `Interrupt_disableMaster` (void)
- void `Interrupt_disableSleepOnIsrExit` (void)
- void `Interrupt_enableInterrupt` (uint32\_t interruptNumber)
- bool `Interrupt_enableMaster` (void)
- void `Interrupt_enableSleepOnIsrExit` (void)
- uint8\_t `Interrupt_getPriority` (uint32\_t interruptNumber)
- uint32\_t `Interrupt_getPriorityGrouping` (void)
- uint8\_t `Interrupt_getPriorityMask` (void)
- uint32\_t `Interrupt_getVectorTableAddress` (void)
- bool `Interrupt_isEnabled` (uint32\_t interruptNumber)
- void `Interrupt_pendInterrupt` (uint32\_t interruptNumber)
- void `Interrupt_registerInterrupt` (uint32\_t interruptNumber, void(\*intHandler)(void))
- void `Interrupt_setPriority` (uint32\_t interruptNumber, uint8\_t priority)
- void `Interrupt_setPriorityGrouping` (uint32\_t bits)
- void `Interrupt_setPriorityMask` (uint8\_t priorityMask)
- void `Interrupt_setVectorTableAddress` (uint32\_t addr)
- void `Interrupt_unpendInterrupt` (uint32\_t interruptNumber)
- void `Interrupt_unregisterInterrupt` (uint32\_t interruptNumber)

### 12.4.1 Detailed Description

The code for this module is contained in `driverlib/interrupt.c`, with `driverlib/interrupt.h` containing the API declarations for use by applications.

## 12.4.2 Function Documentation

### 12.4.2.1 void Interrupt\_disableInterrupt ( uint32\_t *interruptNumber* )

Disables an interrupt.

#### Parameters

<i>interruptNumber</i>	specifies the interrupt to be disabled.
------------------------	---

The specified interrupt is disabled in the interrupt controller. Other enables for the interrupt (such as at the peripheral level) are unaffected by this function.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

#### Returns

None.

Referenced by [ADC14\\_unregisterInterrupt\(\)](#), [AES256\\_unregisterInterrupt\(\)](#), [COMP\\_E\\_unregisterInterrupt\(\)](#), [CS\\_unregisterInterrupt\(\)](#), [DMA\\_unregisterInterrupt\(\)](#), [FlashCtl\\_unregisterInterrupt\(\)](#), [GPIO\\_unregisterInterrupt\(\)](#), [I2C\\_unregisterInterrupt\(\)](#), [MPU\\_disableInterrupt\(\)](#), [PCM\\_unregisterInterrupt\(\)](#), [PSS\\_unregisterInterrupt\(\)](#), [RTC\\_C\\_unregisterInterrupt\(\)](#), [SPI\\_unregisterInterrupt\(\)](#), [Timer32\\_unregisterInterrupt\(\)](#), [Timer\\_A\\_unregisterInterrupt\(\)](#), [UART\\_unregisterInterrupt\(\)](#), and [WDT\\_A\\_unregisterInterrupt\(\)](#).

### 12.4.2.2 bool Interrupt\_disableMaster ( void )

Disables the processor interrupt.

This function prevents the processor from receiving interrupts. This function does not affect the set of interrupts enabled in the interrupt controller; it just gates the single interrupt from the controller to the processor.

#### Returns

Returns **true** if interrupts were already disabled when the function was called or **false** if they were initially enabled.

Referenced by [FlashCtl\\_eraseSector\(\)](#), [FlashCtl\\_performMassErase\(\)](#), [FlashCtl\\_programMemory\(\)](#), [FlashCtl\\_verifyMemory\(\)](#), [PCM\\_gotoLPM0InterruptSafe\(\)](#), [PCM\\_gotoLPM3InterruptSafe\(\)](#), and [PCM\\_gotoLPM4InterruptSafe\(\)](#).

### 12.4.2.3 void Interrupt\_disableSleepOnIsrExit ( void )

Disables the processor to sleep when exiting an ISR.

#### Returns

None

### 12.4.2.4 void Interrupt\_enableInterrupt ( uint32\_t *interruptNumber* )

Enables an interrupt.

**Parameters**

<i>interruptNumber</i>	specifies the interrupt to be enabled.
------------------------	--

The specified interrupt is enabled in the interrupt controller. Other enables for the interrupt (such as at the peripheral level) are unaffected by this function.

Valid values will vary from part to part, so it is important to check the device specific datasheet, however for MSP432 101 the following values can be provided:

- **FAULT\_NMI**
- **FAULT\_HARD**
- **FAULT\_MPU**
- **FAULT\_BUS**
- **FAULT\_USAGE**
- **FAULT\_SVCALL**
- **FAULT\_DEBUG**
- **FAULT\_PENDSV**
- **FAULT\_SYSTICK**
- **INT\_PSS**
- **INT\_CS**
- **INT\_PCM**
- **INT\_WDT\_A**
- **INT\_FPU**
- **INT\_FLCTL**
- **INT\_COMP0**
- **INT\_COMP1**
- **INT\_TA0\_0**
- **INT\_TA0\_N**
- **INT\_TA1\_0**
- **INT\_TA1\_N**
- **INT\_TA2\_0**
- **INT\_TA2\_N**
- **INT\_TA3\_0**
- **INT\_TA3\_N**
- **INT\_EUSCIA0**
- **INT\_EUSCIA1**
- **INT\_EUSCIA2**
- **INT\_EUSCIA3**
- **INT\_EUSCIB0**
- **INT\_EUSCIB1**
- **INT\_EUSCIB2**
- **INT\_EUSCIB3**
- **INT\_ADC14**

- INT\_T32\_INT1
- INT\_T32\_INT2
- INT\_T32\_INTC
- INT\_AES
- INT\_RTCC
- INT\_DMA\_ERR
- INT\_DMA\_INT3
- INT\_DMA\_INT2
- INT\_DMA\_INT1
- INT\_DMA\_INT0
- INT\_PORT1
- INT\_PORT2
- INT\_PORT3
- INT\_PORT4
- INT\_PORT5
- INT\_PORT6

**Returns**

None.

Referenced by [ADC14\\_registerInterrupt\(\)](#), [AES256\\_registerInterrupt\(\)](#), [COMP\\_E\\_registerInterrupt\(\)](#), [CS\\_registerInterrupt\(\)](#), [DMA\\_registerInterrupt\(\)](#), [FlashCtl\\_registerInterrupt\(\)](#), [GPIO\\_registerInterrupt\(\)](#), [I2C\\_registerInterrupt\(\)](#), [MPU\\_enableInterrupt\(\)](#), [PCM\\_registerInterrupt\(\)](#), [PSS\\_registerInterrupt\(\)](#), [RTC\\_C\\_registerInterrupt\(\)](#), [SPI\\_registerInterrupt\(\)](#), [Timer32\\_registerInterrupt\(\)](#), [Timer\\_A\\_registerInterrupt\(\)](#), [UART\\_registerInterrupt\(\)](#), and [WDT\\_A\\_registerInterrupt\(\)](#).

#### 12.4.2.5 bool Interrupt\_enableMaster ( void )

Enables the processor interrupt.

This function allows the processor to respond to interrupts. This function does not affect the set of interrupts enabled in the interrupt controller; it just gates the single interrupt from the controller to the processor.

**Returns**

Returns **true** if interrupts were disabled when the function was called or **false** if they were initially enabled.

Referenced by [FlashCtl\\_eraseSector\(\)](#), [FlashCtl\\_performMassErase\(\)](#), [FlashCtl\\_programMemory\(\)](#), [FlashCtl\\_verifyMemory\(\)](#), [PCM\\_gotoLPM0InterruptSafe\(\)](#), [PCM\\_gotoLPM3InterruptSafe\(\)](#), and [PCM\\_gotoLPM4InterruptSafe\(\)](#).

#### 12.4.2.6 void Interrupt\_enableSleepOnIsrExit ( void )

Enables the processor to sleep when exiting an ISR. For low power operation, this is ideal as power cycles are not wasted with the processing required for waking up from an ISR and going back to sleep.

**Returns**

None

#### 12.4.2.7 uint8\_t Interrupt\_getPriority ( uint32\_t *interruptNumber* )

Gets the priority of an interrupt.

**Parameters**

<i>interruptNumber</i>	specifies the interrupt in question.
------------------------	--------------------------------------

This function gets the priority of an interrupt. See [Interrupt\\_setPriority\(\)](#) for a definition of the priority value.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

**Returns**

Returns the interrupt priority, or -1 if an invalid interrupt was specified.

#### 12.4.2.8 uint32\_t Interrupt\_getPriorityGrouping ( void )

Gets the priority grouping of the interrupt controller.

This function returns the split between preemptable priority levels and sub-priority levels in the interrupt priority specification.

**Returns**

The number of bits of preemptable priority.

#### 12.4.2.9 uint8\_t Interrupt\_getPriorityMask ( void )

Gets the priority masking level

This function gets the current setting of the interrupt priority masking level. The value returned is the priority level such that all interrupts of that and lesser priority are masked. A value of 0 means that priority masking is disabled.

Smaller numbers correspond to higher interrupt priorities. So for example a priority level mask of 4 allows interrupts of priority level 0-3, and interrupts with a numerical priority of 4 and greater are blocked.

The hardware priority mechanism only looks at the upper N bits of the priority level (where N is 3 for the MSP432 family), so any prioritization must be performed in those bits.

**Returns**

Returns the value of the interrupt priority level mask.

#### 12.4.2.10 uint32\_t Interrupt\_getVectorTableAddress ( void )

Returns the address of the interrupt vector table.

##### Returns

Address of the vector table.

#### 12.4.2.11 bool Interrupt\_isEnabled ( uint32\_t *interruptNumber* )

Returns if a peripheral interrupt is enabled.

##### Parameters

<i>interruptNumber</i>	specifies the interrupt to check.
------------------------	-----------------------------------

This function checks if the specified interrupt is enabled in the interrupt controller.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

##### Returns

A non-zero value if the interrupt is enabled.

#### 12.4.2.12 void Interrupt\_pendInterrupt ( uint32\_t *interruptNumber* )

Pends an interrupt.

##### Parameters

<i>interruptNumber</i>	specifies the interrupt to be pended.
------------------------	---------------------------------------

The specified interrupt is pended in the interrupt controller. Pending an interrupt causes the interrupt controller to execute the corresponding interrupt handler at the next available time, based on the current interrupt state priorities. For example, if called by a higher priority interrupt handler, the specified interrupt handler is not called until after the current interrupt handler has completed execution. The interrupt must have been enabled for it to be called.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

##### Returns

None.

#### 12.4.2.13 void Interrupt\_registerInterrupt ( uint32\_t *interruptNumber*, void(\*)*(void)* *intHandler* )

Registers a function to be called when an interrupt occurs.

##### Parameters

<i>interruptNumber</i>	specifies the interrupt in question.
<i>intHandler</i>	is a pointer to the function to be called.

**Note**

The use of this function (directly or indirectly via a peripheral driver interrupt register function) moves the interrupt vector table from flash to SRAM. Therefore, care must be taken when linking the application to ensure that the SRAM vector table is located at the beginning of SRAM; otherwise the NVIC does not look in the correct portion of memory for the vector table (it requires the vector table be on a 1 kB memory alignment). Normally, the SRAM vector table is so placed via the use of linker scripts. See the discussion of compile-time versus run-time interrupt handler registration in the introduction to this chapter.

This function is only used if the customer wants to specify the interrupt handler at run time. In most cases, this is done through means of the user setting the ISR function pointer in the startup file. Refer Refer to the Module Operation section for more details.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

**Returns**

None.

Referenced by [ADC14\\_registerInterrupt\(\)](#), [AES256\\_registerInterrupt\(\)](#), [COMP\\_E\\_registerInterrupt\(\)](#), [CS\\_registerInterrupt\(\)](#), [DMA\\_registerInterrupt\(\)](#), [FlashCtl\\_registerInterrupt\(\)](#), [GPIO\\_registerInterrupt\(\)](#), [I2C\\_registerInterrupt\(\)](#), [MPU\\_registerInterrupt\(\)](#), [PCM\\_registerInterrupt\(\)](#), [PSS\\_registerInterrupt\(\)](#), [RTC\\_C\\_registerInterrupt\(\)](#), [SPI\\_registerInterrupt\(\)](#), [SysTick\\_registerInterrupt\(\)](#), [Timer32\\_registerInterrupt\(\)](#), [Timer\\_A\\_registerInterrupt\(\)](#), [UART\\_registerInterrupt\(\)](#), and [WDT\\_A\\_registerInterrupt\(\)](#).

#### 12.4.2.14 void Interrupt\_setPriority ( uint32\_t *interruptNumber*, uint8\_t *priority* )

Sets the priority of an interrupt.

**Parameters**

<i>interruptNumber</i>	specifies the interrupt in question.
<i>priority</i>	specifies the priority of the interrupt.

This function is used to set the priority of an interrupt. When multiple interrupts are asserted simultaneously, the ones with the highest priority are processed before the lower priority interrupts. Smaller numbers correspond to higher interrupt priorities; priority 0 is the highest interrupt priority.

The hardware priority mechanism only looks at the upper N bits of the priority level (where N is 3 for the MSP432 family), so any prioritization must be performed in those bits. The remaining bits can be used to sub-prioritize the interrupt sources, and may be used by the hardware priority mechanism on a future part. This arrangement allows priorities to migrate to different NVIC implementations without changing the gross prioritization of the interrupts.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

**Returns**

None.



#### 12.4.2.15 void Interrupt\_setPriorityGrouping ( uint32\_t *bits* )

Sets the priority grouping of the interrupt controller.

**Parameters**

<i>bits</i>	specifies the number of bits of preemptable priority.
-------------	---

This function specifies the split between preemptable priority levels and sub-priority levels in the interrupt priority specification. The range of the grouping values are dependent upon the hardware implementation; on the MSP432 family, three bits are available for hardware interrupt prioritization and therefore priority grouping values of three through seven have the same effect.

**Returns**

None.

12.4.2.16 void Interrupt\_setPriorityMask ( uint8\_t *priorityMask* )

Sets the priority masking level

**Parameters**

<i>priorityMask</i>	is the priority level that is masked.
---------------------	---------------------------------------

This function sets the interrupt priority masking level so that all interrupts at the specified or lesser priority level are masked. Masking interrupts can be used to globally disable a set of interrupts with priority below a predetermined threshold. A value of 0 disables priority masking.

Smaller numbers correspond to higher interrupt priorities. So for example a priority level mask of 4 allows interrupts of priority level 0-3, and interrupts with a numerical priority of 4 and greater are blocked.

The hardware priority mechanism only looks at the upper N bits of the priority level (where N is 3 for the MSP432 family), so any prioritization must be performed in those bits.

**Returns**

None.

12.4.2.17 void Interrupt\_setVectorTableAddress ( uint32\_t *addr* )

Sets the address of the vector table. This function is for advanced users who might want to switch between multiple instances of vector tables (perhaps between flash/ram).

**Parameters**

<i>addr</i>	is the new address of the vector table.
-------------	---

**Returns**

None.

12.4.2.18 void Interrupt\_unpendInterrupt ( uint32\_t *interruptNumber* )

Un-pends an interrupt.

**Parameters**

<i>interruptNumber</i>	specifies the interrupt to be un-pended.
------------------------	--

The specified interrupt is un-pended in the interrupt controller. This will cause any previously generated interrupts that have not been handled yet (due to higher priority interrupts or the interrupt no having been enabled yet) to be discarded.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

**Returns**

None.

### 12.4.2.19 void Interrupt\_unregisterInterrupt ( uint32\_t *interruptNumber* )

Unregisters the function to be called when an interrupt occurs.

**Parameters**

<i>interruptNumber</i>	specifies the interrupt in question.
------------------------	--------------------------------------

This function is used to indicate that no handler should be called when the given interrupt is asserted to the processor. The interrupt source is automatically disabled (via [Interrupt\\_disableInterrupt\(\)](#)) if necessary.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

See [Interrupt\\_enableInterrupt](#) for details about the interrupt parameter

**Returns**

None.

Referenced by [ADC14\\_unregisterInterrupt\(\)](#), [AES256\\_unregisterInterrupt\(\)](#), [COMP\\_E\\_unregisterInterrupt\(\)](#), [CS\\_unregisterInterrupt\(\)](#), [DMA\\_unregisterInterrupt\(\)](#), [FlashCtl\\_unregisterInterrupt\(\)](#), [GPIO\\_unregisterInterrupt\(\)](#), [I2C\\_unregisterInterrupt\(\)](#), [MPU\\_unregisterInterrupt\(\)](#), [PCM\\_unregisterInterrupt\(\)](#), [PSS\\_unregisterInterrupt\(\)](#), [RTC\\_C\\_unregisterInterrupt\(\)](#), [SPI\\_unregisterInterrupt\(\)](#), [SysTick\\_unregisterInterrupt\(\)](#), [Timer32\\_unregisterInterrupt\(\)](#), [Timer\\_A\\_unregisterInterrupt\(\)](#), [UART\\_unregisterInterrupt\(\)](#), and [WDT\\_A\\_unregisterInterrupt\(\)](#).

# 13 Memory Protection Unit (MPU)

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## 13.1 Module Operation

The Memory Protection Unit (MPU) API provides functions to configure the MPU. The MPU is tightly coupled to the Cortex-M processor core and provides a means to establish access permissions on regions of memory.

Up to eight memory regions can be defined. Each region has a base address and a size. The size is specified as a power of 2 between 32 bytes and 4 GB, inclusive. The region's base address must be aligned to the size of the region. Each region also has access permissions. Code execution can be allowed or disallowed for a region. A region can be configured for read-only access, read/write access, or no access for both privileged and user modes. Access permissions can be used to create an environment where only kernel or system code can access certain hardware registers or sections of code.

The MPU creates 8 sub-regions within each region. Any sub-region or combination of sub-regions can be disabled, allowing creation of "holes" or complex overlaying regions with different permissions. The sub-regions can also be used to create an unaligned beginning or ending of a region by disabling one or more of the leading or trailing sub-regions.

Once the regions are defined and the MPU is enabled, any access violation of a region causes a memory management fault, and the fault handler is acted.

## 13.2 Module Operation

The MPU APIs provide a means to enable and configure the MPU and memory protection regions.

Generally, the memory protection regions should be defined before enabling the MPU. The regions can be configured by calling `MPU_setRegion()` once for each region to be configured.

A region that is defined by `MPU_setRegion()` can be initially enabled or disabled. If the region is not initially enabled, it can be enabled later by calling `MPU_enableRegion()`. An enabled region can be disabled by calling `MPU_disableRegion()`. When a region is disabled, its configuration is preserved as long as it is not overwritten. In this case, it can be enabled again with `MPU_enableRegion()` without the need to reconfigure the region.

Care must be taken when setting up a protection region using `MPU_setRegion()`. The function writes to multiple registers and is not protected from interrupts. Therefore, it is possible that an interrupt which accesses a region may occur while that region is in the process of being changed. The safest way to protect against this is to make sure that a region is always disabled before making any changes. Otherwise, it is up to the caller to ensure that `MPU_setRegion()` is always called from within code that cannot be interrupted, or from code that is not affected if an interrupt occurs while the region attributes are being changed.

The attributes of a region that have already been programmed can be retrieved and saved using

the [MPU\\_getRegionCount\(\)](#) function. This function is intended to save the attributes in a format that can be used later to reload the region using the [MPU\\_setRegion\(\)](#) function. Note that the enable state of the region is saved with the attributes and takes effect when the region is reloaded.

When one or more regions are defined, the MPU can be enabled by calling [MPU\\_enableModule\(\)](#). This function turns on the MPU and also defines the behavior in privileged mode and in the Hard Fault and NMI fault handlers. The MPU can be configured so that when in privileged mode and no regions are enabled, a default memory map is applied. If this feature is not enabled, then a memory management fault is generated if the MPU is enabled and no regions are configured and enabled. The MPU can also be set to use a default memory map when in the Hard Fault or NMI handlers, instead of using the configured regions. All of these features are selected when calling [MPU\\_enableModule\(\)](#). When the MPU is enabled, it can be disabled by calling [MPU\\_disableModule\(\)](#).

Finally, if the application is using run-time interrupt registration (see [Interrupt\\_registerInterrupt\(\)](#)), then the function [MPU\\_registerInterrupt\(\)](#) can be used to install the fault handler which is called whenever a memory protection violation occurs. This function also enables the fault handler. If compile-time interrupt registration is used, then the [Interrupt\\_enableInterrupt\(\)](#) function with the parameter **FAULT\_MPU** must be used to enable the memory management fault handler. When the memory management fault handler has been installed with [MPU\\_disableModule\(\)](#), it can be removed by calling [MPU\\_unregisterInterrupt\(\)](#).

## 13.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the MPU module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the MPU module to define a new memory region and set it as read only:

## 13.4 Definitions

### Functions

- void [MPU\\_disableInterrupt](#) (void)
- void [MPU\\_disableModule](#) (void)
- void [MPU\\_disableRegion](#) (uint32\_t region)
- void [MPU\\_enableInterrupt](#) (void)
- void [MPU\\_enableModule](#) (uint32\_t mpuConfig)
- void [MPU\\_enableRegion](#) (uint32\_t region)
- void [MPU\\_getRegion](#) (uint32\_t region, uint32\_t \*addr, uint32\_t \*pflags)
- uint32\_t [MPU\\_getRegionCount](#) (void)
- void [MPU\\_registerInterrupt](#) (void(\*intHandler)(void))
- void [MPU\\_setRegion](#) (uint32\_t region, uint32\_t addr, uint32\_t flags)
- void [MPU\\_unregisterInterrupt](#) (void)

### 13.4.1 Detailed Description

The code for this module is contained in `driverlib/mpu.c`, with `driverlib/mpu.h` containing the API declarations for use by applications.

## 13.4.2 Function Documentation

### 13.4.2.1 void MPU\_disableInterrupt ( void )

Disables the interrupt for the memory management fault.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#).

### 13.4.2.2 void MPU\_disableModule ( void )

Disables the MPU for use.

This function disables the Cortex-M memory protection unit. When the MPU is disabled, the default memory map is used and memory management faults are not generated.

**Returns**

None.

### 13.4.2.3 void MPU\_disableRegion ( uint32\_t *region* )

Disables a specific region.

**Parameters**

<i>region</i>	is the region number to disable. Valid values are between 0 and 7 inclusively.
---------------	--

This function is used to disable a previously enabled memory protection region. The region remains configured if it is not overwritten with another call to [MPU\\_setRegion\(\)](#), and can be enabled again by calling [MPU\\_enableRegion\(\)](#).

**Returns**

None.

### 13.4.2.4 void MPU\_enableInterrupt ( void )

Enables the interrupt for the memory management fault.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#).

### 13.4.2.5 void MPU\_enableModule ( uint32\_t *mpuConfig* )

Enables and configures the MPU for use.

**Parameters**

<i>mpuConfig</i>	is the logical OR of the possible configurations.
------------------	---

This function enables the Cortex-M memory protection unit. It also configures the default behavior when in privileged mode and while handling a hard fault or NMI. Prior to enabling the MPU, at least one region must be set by calling [MPU\\_setRegion\(\)](#) or else by enabling the default region for privileged mode by passing the **MPU\_CONFIG\_PRIV\_DEFAULT** flag to [MPU\\_enableModule\(\)](#). Once the MPU is enabled, a memory management fault is generated for memory access violations.

The *mpuConfig* parameter should be the logical OR of any of the following:

- **MPU\_CONFIG\_PRIV\_DEFAULT** enables the default memory map when in privileged mode and when no other regions are defined. If this option is not enabled, then there must be at least one valid region already defined when the MPU is enabled.
- **MPU\_CONFIG\_HARDFLT\_NMI** enables the MPU while in a hard fault or NMI exception handler. If this option is not enabled, then the MPU is disabled while in one of these exception handlers and the default memory map is applied.
- **MPU\_CONFIG\_NONE** chooses none of the above options. In this case, no default memory map is provided in privileged mode, and the MPU is not enabled in the fault handlers.

**Returns**

None.

#### 13.4.2.6 void MPU\_enableRegion ( uint32\_t *region* )

Enables a specific region.

**Parameters**

<i>region</i>	is the region number to enable. Valid values are between 0 and 7 inclusively.
---------------	---

This function is used to enable a memory protection region. The region should already be configured with the [MPU\\_setRegion\(\)](#) function. Once enabled, the memory protection rules of the region are applied and access violations cause a memory management fault.

**Returns**

None.

#### 13.4.2.7 void MPU\_getRegion ( uint32\_t *region*, uint32\_t \* *addr*, uint32\_t \* *pflags* )

Gets the current settings for a specific region.

**Parameters**

<i>region</i>	is the region number to get. Valid values are between 0 and 7 inclusively.
<i>addr</i>	points to storage for the base address of the region.



<i>pflags</i>	points to the attribute flags for the region.
---------------	---

This function retrieves the configuration of a specific region. The meanings and format of the parameters is the same as that of the [MPU\\_setRegion\(\)](#) function.

This function can be used to save the configuration of a region for later use with the [MPU\\_setRegion\(\)](#) function. The region's enable state is preserved in the attributes that are saved.

**Returns**

None.

#### 13.4.2.8 uint32\_t MPU\_getRegionCount ( void )

Gets the count of regions supported by the MPU.

This function is used to get the total number of regions that are supported by the MPU, including regions that are already programmed.

**Returns**

The number of memory protection regions that are available for programming using [MPU\\_setRegion\(\)](#).

#### 13.4.2.9 void MPU\_registerInterrupt ( void(\*)(void) intHandler )

Registers an interrupt handler for the memory management fault.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the memory management fault occurs.
-------------------	--

This function sets and enables the handler to be called when the MPU generates a memory management fault due to a protection region access violation.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_registerInterrupt\(\)](#).

#### 13.4.2.10 void MPU\_setRegion ( uint32\_t region, uint32\_t addr, uint32\_t flags )

Sets up the access rules for a specific region.

**Parameters**

<i>region</i>	is the region number to set up.
---------------	---------------------------------

<i>addr</i>	is the base address of the region. It must be aligned according to the size of the region specified in flags.
<i>flags</i>	is a set of flags to define the attributes of the region.

This function sets up the protection rules for a region. The region has a base address and a set of attributes including the size. The base address parameter, *addr*, must be aligned according to the size, and the size must be a power of 2.

#### Parameters

<i>region</i>	is the region number to set. Valid values are between 0 and 7 inclusively.
---------------	--

The *flags* parameter is the logical OR of all of the attributes of the region. It is a combination of choices for region size, execute permission, read/write permissions, disabled sub-regions, and a flag to determine if the region is enabled.

The size flag determines the size of a region and must be one of the following:

- MPU\_RGN\_SIZE\_32B
- MPU\_RGN\_SIZE\_64B
- MPU\_RGN\_SIZE\_128B
- MPU\_RGN\_SIZE\_256B
- MPU\_RGN\_SIZE\_512B
- MPU\_RGN\_SIZE\_1K
- MPU\_RGN\_SIZE\_2K
- MPU\_RGN\_SIZE\_4K
- MPU\_RGN\_SIZE\_8K
- MPU\_RGN\_SIZE\_16K
- MPU\_RGN\_SIZE\_32K
- MPU\_RGN\_SIZE\_64K
- MPU\_RGN\_SIZE\_128K
- MPU\_RGN\_SIZE\_256K
- MPU\_RGN\_SIZE\_512K
- MPU\_RGN\_SIZE\_1M
- MPU\_RGN\_SIZE\_2M
- MPU\_RGN\_SIZE\_4M
- MPU\_RGN\_SIZE\_8M
- MPU\_RGN\_SIZE\_16M
- MPU\_RGN\_SIZE\_32M
- MPU\_RGN\_SIZE\_64M
- MPU\_RGN\_SIZE\_128M
- MPU\_RGN\_SIZE\_256M
- MPU\_RGN\_SIZE\_512M
- MPU\_RGN\_SIZE\_1G
- MPU\_RGN\_SIZE\_2G
- MPU\_RGN\_SIZE\_4G

The execute permission flag must be one of the following:

- **MPU\_RGN\_PERM\_EXEC** enables the region for execution of code
- **MPU\_RGN\_PERM\_NOEXEC** disables the region for execution of code

The read/write access permissions are applied separately for the privileged and user modes. The read/write access flags must be one of the following:

- **MPU\_RGN\_PERM\_PRV\_NO\_USR\_NO** - no access in privileged or user mode
- **MPU\_RGN\_PERM\_PRV\_RW\_USR\_NO** - privileged read/write, user no access
- **MPU\_RGN\_PERM\_PRV\_RW\_USR\_RO** - privileged read/write, user read-only
- **MPU\_RGN\_PERM\_PRV\_RW\_USR\_RW** - privileged read/write, user read/write
- **MPU\_RGN\_PERM\_PRV\_RO\_USR\_NO** - privileged read-only, user no access
- **MPU\_RGN\_PERM\_PRV\_RO\_USR\_RO** - privileged read-only, user read-only

The region is automatically divided into 8 equally-sized sub-regions by the MPU. Sub-regions can only be used in regions of size 256 bytes or larger. Any of these 8 sub-regions can be disabled, allowing for creation of “holes” in a region which can be left open, or overlaid by another region with different attributes. Any of the 8 sub-regions can be disabled with a logical OR of any of the following flags:

- **MPU\_SUB\_RGN\_DISABLE\_0**
- **MPU\_SUB\_RGN\_DISABLE\_1**
- **MPU\_SUB\_RGN\_DISABLE\_2**
- **MPU\_SUB\_RGN\_DISABLE\_3**
- **MPU\_SUB\_RGN\_DISABLE\_4**
- **MPU\_SUB\_RGN\_DISABLE\_5**
- **MPU\_SUB\_RGN\_DISABLE\_6**
- **MPU\_SUB\_RGN\_DISABLE\_7**

Finally, the region can be initially enabled or disabled with one of the following flags:

- **MPU\_RGN\_ENABLE**
- **MPU\_RGN\_DISABLE**

As an example, to set a region with the following attributes: size of 32 KB, execution enabled, read-only for both privileged and user, one sub-region disabled, and initially enabled; the *flags* parameter would have the following value:

```
(MPU_RGN_SIZE_32K | MPU_RGN_PERM_EXEC | MPU_RGN_PERM_PRV_RO_USR_RO |
MPU_SUB_RGN_DISABLE_2 | MPU_RGN_ENABLE)
```

#### Note

This function writes to multiple registers and is not protected from interrupts. It is possible that an interrupt which accesses a region may occur while that region is in the process of being changed. The safest way to handle this is to disable a region before changing it. Refer to the discussion of this in the API Detailed Description section.

#### Returns

None.

### 13.4.2.11 void MPU\_unregisterInterrupt ( void )

Unregisters an interrupt handler for the memory management fault.

This function disables and clears the handler to be called when a memory management fault occurs.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_unregisterInterrupt\(\)](#).

## 14 Power Control Module (PCM)

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### 14.1 Module Operation

The Power Control Manager (PCM) module for DriverLib is meant to simplify the management of power states and provide a level of intelligence to users for switching between power states.

### 14.2 Switching States

One of the most useful features of the PCM module is the ability for the user to switch between power states without having to worry about the logic requirements of the state transitions. By using the `PCM_setPowerState` function, DriverLib will take in a parameter for the power state and automatically handle all of the state transitions. Say that the user wants to switch to use the DCDC converter with a voltage level of `VCORE1` (`PCM_AM_DCDC_VCORE1`). Say that that same user is currently in the default mode of using the LDO with a voltage level of `VCORE0` (`PCM_AM_LDO_VCORE0`). Normally, the user would have to take into account that there is a state transition that must happen to `PCM_AM_LDO_VCORE1`, however with the `PCM_setPowerState` API the user does not need to worry about this. The call to change the power state in this example would be:

```
PCM_setPowerState(PCM_AM_DCDC_VCORE1);
```

### 14.3 Switching Modes/Levels

In addition to being able to switch between individual power states, the PCM DriverLib API module also gives the user the ability to switch between different power modes and levels. This gives the user a more granular approach to power management and allows for a more refined customization of the power driver.

For changing between power levels, the user will be able to switch back and forth between **PCM\_VCORE0** and **PCM\_VCORE1** using the `PCM_setCoreVoltageLevel` function. While using this function it is important to note that the underlying power mode will be preserved. For example, if `PCM_setCoreVoltageLevel` is called with the **PCM\_VCORE1** parameter while the device is in **PCM\_AM\_LDO\_VCORE0** mode, the power state will be changed to **PCM\_AM\_LDO\_VCORE1**. If the same API is called with the same parameter in **PCM\_AM\_DCDC\_VCORE0** mode, the power state will be changed to **PCM\_AM\_DCDC\_VCORE1** mode.

The same preservation logic also applies while switching between power modes. If the `PCM_setPowerMode` function is called with the `PCM_DCDC_MODE` parameter while the device is in `PCM_AM_LDO_VCORE0` mode, the device will change to `PCM_AM_DCDC_VCORE0` mode (leaving the voltage level unchanged).

## 14.4 Low Power Mode and State Retention

In addition to being able to manipulate individual states/modes/levels, APIs are also provided to simplify entry into the low power modes of MSP432.

### Low Power Entry Functions:

- `PCM_gotoLPM0`
- `PCM_gotoLPM3`
- `PCM_shutdownDevice`

When using these low power modes entry functions, it is important to note that the original state of the device before low power mode entry is retained. After the device wakes up from low power mode, the original power mode is restored. For example, say that the device is in `PCM_AM_DCDC_VCORE0` mode and then the user calls the `PCM_gotoLPM3` API. Since MSP432 devices are not allowed to go into LPM3 while in a DCDC power mode, the API will have the intelligence to first change into `PCM_AM_LDO_VCORE0` mode, and then go to LPM3. When the device wakes up, the API will automatically switch back to `PCM_AM_DCDC_VCORE0` mode. If the user wants to go into DSL in the previous example without the state preservation, the `PCM_setPowerState` function should be used with the `PCM_LPM3` parameter.

## 14.5 Enabling/Disabling Rude Mode

If the user calls a low power entry function that disables a clock source while an active peripheral is accessing the clock source, by default MSP432 will not allow the transition. This can be enabled/disabled by using the `PCM_enableRudeMode` and `PCM_disableRudeMode` functions respectively. By using these functions, the user can set the device to "force" its way into the low power mode by forcibly halting any dependent clock resource.

## 14.6 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the PCM module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to change power levels with the PCM module. This is done in order to facilitate a higher frequency of 48Mhz. For a set of more detailed code examples, please refer to the code examples in the examples/ directory of the MSPWare release:

```
/* Re-enabling port pin interrupt */
MAP_GPIO_clearInterruptFlag(GPIO_PORT_P1, GPIO_PIN1);
MAP_Interrupt_enableInterrupt(INT_PORT1);
MAP_Interrupt_enableMaster();

/* Change to new power state */
MAP_PCM_setPowerState(powerStates[curPowerState]);
```

## 14.7 Definitions

### Functions

- void [PCM\\_clearInterruptFlag](#) (uint32\_t flags)
- void [PCM\\_disableInterrupt](#) (uint32\_t flags)
- void [PCM\\_disableRudeMode](#) (void)
- void [PCM\\_enableInterrupt](#) (uint32\_t flags)
- void [PCM\\_enableRudeMode](#) (void)
- uint8\_t [PCM\\_getCoreVoltageLevel](#) (void)
- uint32\_t [PCM\\_getEnabledInterruptStatus](#) (void)
- uint32\_t [PCM\\_getInterruptStatus](#) (void)
- uint8\_t [PCM\\_getPowerMode](#) (void)
- uint8\_t [PCM\\_getPowerState](#) (void)
- bool [PCM\\_gotoLPM0](#) (void)
- bool [PCM\\_gotoLPM0InterruptSafe](#) (void)
- bool [PCM\\_gotoLPM3](#) (void)
- bool [PCM\\_gotoLPM3InterruptSafe](#) (void)
- bool [PCM\\_gotoLPM4](#) (void)
- bool [PCM\\_gotoLPM4InterruptSafe](#) (void)
- void [PCM\\_registerInterrupt](#) (void(\*intHandler)(void))
- bool [PCM\\_setCoreVoltageLevel](#) (uint\_fast8\_t voltageLevel)
- bool [PCM\\_setCoreVoltageLevelNonBlocking](#) (uint\_fast8\_t voltageLevel)
- bool [PCM\\_setCoreVoltageLevelWithTimeout](#) (uint\_fast8\_t voltageLevel, uint32\_t timeOut)
- bool [PCM\\_setPowerMode](#) (uint\_fast8\_t powerMode)
- bool [PCM\\_setPowerModeNonBlocking](#) (uint\_fast8\_t powerMode)
- bool [PCM\\_setPowerModeWithTimeout](#) (uint\_fast8\_t powerMode, uint32\_t timeOut)
- bool [PCM\\_setPowerState](#) (uint\_fast8\_t powerState)
- bool [PCM\\_setPowerStateNonBlocking](#) (uint\_fast8\_t powerState)
- bool [PCM\\_setPowerStateWithTimeout](#) (uint\_fast8\_t powerState, uint32\_t timeout)
- bool [PCM\\_shutdownDevice](#) (uint32\_t shutdownMode)
- void [PCM\\_unregisterInterrupt](#) (void)

### 14.7.1 Detailed Description

The code for this module is contained in `driverlib/pcm.c`, with `driverlib/pcm.h` containing the API declarations for use by applications.



## 14.7.2 Function Documentation

### 14.7.2.1 void PCM\_clearInterruptFlag ( uint32\_t flags )

Clears power system interrupt sources.

The specified power system interrupt sources are cleared, so that they no longer assert. This function must be called in the interrupt handler to keep it from being called again immediately upon exit.

#### Note

Because there is a write buffer in the Cortex-M processor, it may take several clock cycles before the interrupt source is actually cleared. Therefore, it is recommended that the interrupt source be cleared early in the interrupt handler (as opposed to the very last action) to avoid returning from the interrupt handler before the interrupt source is actually cleared. Failure to do so may result in the interrupt handler being immediately reentered (because the interrupt controller still sees the interrupt source asserted).

#### Parameters

<i>flags</i>	is a bit mask of the interrupt sources to be cleared. Must be a logical OR of <ul style="list-style-type: none"> <li>■ <b>PCM_DCDCERROR,</b></li> <li>■ <b>PCM_AM_INVALIDTRANSITION,</b></li> <li>■ <b>PCM_SM_INVALIDCLOCK,</b></li> <li>■ <b>PCM_SM_INVALIDTRANSITION</b></li> </ul>
--------------	---

#### Note

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

#### Returns

None.

### 14.7.2.2 void PCM\_disableInterrupt ( uint32\_t flags )

Disables individual power control interrupt sources.

#### Parameters

<i>flags</i>	is a bit mask of the interrupt sources to be enabled. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ <b>PCM_DCDCERROR,</b></li> <li>■ <b>PCM_AM_INVALIDTRANSITION,</b></li> <li>■ <b>PCM_SM_INVALIDCLOCK,</b></li> <li>■ <b>PCM_SM_INVALIDTRANSITION</b></li> </ul>
--------------	--

This function disables the indicated power control interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**

None.

## 14.7.2.3 void PCM\_disableRudeMode ( void )

Disables "rude mode" entry into LPM3 and shutdown modes. With this mode disabled, an entry into shutdown or LPM3 will wait for any active clock requests to free up before going into LPM3 or shutdown.

**Returns**

None

## 14.7.2.4 void PCM\_enableInterrupt ( uint32\_t flags )

Enables individual power control interrupt sources.

**Parameters**

<i>flags</i>	is a bit mask of the interrupt sources to be enabled. Must be a logical OR of: <ul style="list-style-type: none"> <li>■ PCM_DCDCEERROR,</li> <li>■ PCM_AM_INVALIDTRANSITION,</li> <li>■ PCM_SM_INVALIDCLOCK,</li> <li>■ PCM_SM_INVALIDTRANSITION</li> </ul>
--------------	---

This function enables the indicated power control interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

**Returns**

None.

## 14.7.2.5 void PCM\_enableRudeMode ( void )

Enables "rude mode" entry into LPM3 and shutdown modes. With this mode enabled, an entry into shutdown or LPM3 will occur even if there are clock systems active. The system will forcibly turn off all clock/systems when going into these modes.

**Returns**

None

#### 14.7.2.6 uint8\_t PCM\_getCoreVoltageLevel ( void )

Returns the current powers state of the system see the PCM\_setCoreVoltageLevel function for specific information about the modes.

**Returns**

The current voltage of the system

Possible return values include:

- PCM\_VCORE0
- PCM\_VCORE1
- PCM\_VCORELPM3

References [PCM\\_getPowerState\(\)](#).

#### 14.7.2.7 uint32\_t PCM\_getEnabledInterruptStatus ( void )

Gets the current interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Returns**

The current interrupt status, enumerated as a bit field of:

- PCM\_DCDCERROR,
- PCM\_AM\_INVALIDTRANSITION,
- PCM\_SM\_INVALIDCLOCK,
- PCM\_SM\_INVALIDTRANSITION

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

References [PCM\\_getInterruptStatus\(\)](#).

#### 14.7.2.8 uint32\_t PCM\_getInterruptStatus ( void )

Gets the current interrupt status.

**Returns**

The current interrupt status, enumerated as a bit field of:

- PCM\_DCDCERROR,
- PCM\_AM\_INVALIDTRANSITION,
- PCM\_SM\_INVALIDCLOCK,
- PCM\_SM\_INVALIDTRANSITION

**Note**

The interrupt sources vary based on the part in use. Please consult the data sheet for the part you are using to determine which interrupt sources are available.

Referenced by [PCM\\_getEnabledInterruptStatus\(\)](#).

#### 14.7.2.9 uint8\_t PCM\_getPowerMode ( void )

Returns the current powers state of the system see the **PCM\_setPowerState** function for specific information about the modes.

**Returns**

The current power mode of the system

References [PCM\\_getPowerState\(\)](#).

Referenced by [PCM\\_gotoLPM3\(\)](#).

#### 14.7.2.10 uint8\_t PCM\_getPowerState ( void )

Returns the current powers state of the system see the **PCMChangePowerState** function for specific information about the states.

Refer to [PCM\\_setPowerState](#) for possible return values.

**Returns**

The current power state of the system

Referenced by [PCM\\_getCoreVoltageLevel\(\)](#), [PCM\\_getPowerMode\(\)](#), and [PCM\\_gotoLPM3\(\)](#).

#### 14.7.2.11 bool PCM\_gotoLPM0 ( void )

Transitions the device into LPM0.

Refer to the device specific data sheet for specifics about low power modes.

**Returns**

false if sleep state cannot be entered, true otherwise.

Referenced by [PCM\\_gotoLPM0InterruptSafe\(\)](#).

#### 14.7.2.12 bool PCM\_gotoLPM0InterruptSafe ( void )

Transitions the device into LPM0 while maintaining a safe interrupt handling mentality. This function is meant to be used in situations where the user wants to go to sleep, however does not want to go to "miss" any interrupts due to the fact that going to LPM0 is not an atomic operation. This function will modify the PRIMASK and on exit of the program the master interrupts will be disabled.

Refer to the device specific data sheet for specifics about low power modes.

**Returns**

false if sleep state cannot be entered, true otherwise.

References [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [PCM\\_gotoLPM0\(\)](#).

#### 14.7.2.13 bool PCM\_gotoLPM3 ( void )

Transitions the device into LPM3

Refer to the device specific data sheet for specifics about low power modes. Note that since LPM3 cannot be entered from a DCDC power modes, the power mode is first switched to LDO operation (if in DCDC mode), the deep sleep is entered, and the DCDC mode is restored on wake up.

**Returns**

false if sleep state cannot be entered, true otherwise.

References [PCM\\_getPowerMode\(\)](#), [PCM\\_getPowerState\(\)](#), [PCM\\_setPowerMode\(\)](#), and [PCM\\_setPowerState\(\)](#).

Referenced by [PCM\\_gotoLPM3InterruptSafe\(\)](#), and [PCM\\_gotoLPM4\(\)](#).

#### 14.7.2.14 bool PCM\_gotoLPM3InterruptSafe ( void )

Transitions the device into LPM3 while maintaining a safe interrupt handling mentality. This function is meant to be used in situations where the user wants to go to LPM3, however does not want to go to "miss" any interrupts due to the fact that going to LPM3 is not an atomic operation. This function will modify the PRIMASK and on exit of the program the master interrupts will be disabled.

Refer to the device specific data sheet for specifics about low power modes. Note that since LPM3 cannot be entered from a DCDC power modes, the power mode is first switched to LDO operation (if in DCDC mode), the deep sleep is entered, and the DCDC mode is restored on wake up.

**Returns**

false if sleep state cannot be entered, true otherwise.

References [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [PCM\\_gotoLPM3\(\)](#).

#### 14.7.2.15 bool PCM\_gotoLPM4 ( void )

Transitions the device into LPM4. LPM4 is the exact same with LPM3, just with RTC\_C and WDT\_A disabled. When waking up, RTC\_C and WDT\_A will remain disabled until reconfigured by the user.

**Returns**

false if sleep state cannot be entered, true otherwise.

References [PCM\\_gotoLPM3\(\)](#), [RTC\\_C\\_holdClock\(\)](#), and [WDT\\_A\\_holdTimer\(\)](#).

Referenced by [PCM\\_gotoLPM4InterruptSafe\(\)](#).

#### 14.7.2.16 bool PCM\_gotoLPM4InterruptSafe ( void )

Transitions the device into LPM4 while maintaining a safe interrupt handling mentality. This function is meant to be used in situations where the user wants to go to LPM4, however does not want to go to "miss" any interrupts due to the fact that going to LPM4 is not an atomic operation.

This function will modify the PRIMASK and on exit of the program the master interrupts will be disabled.

Refer to the device specific data sheet for specifics about low power modes. Note that since LPM3 cannot be entered from a DCDC power modes, the power mode is first switched to LDO operation (if in DCDC mode), the deep sleep is entered, and the DCDC mode is restored on wake up.

#### Returns

false if sleep state cannot be entered, true otherwise.

References [Interrupt\\_disableMaster\(\)](#), [Interrupt\\_enableMaster\(\)](#), and [PCM\\_gotoLPM4\(\)](#).

### 14.7.2.17 void PCM\_registerInterrupt ( void(\*)(void) *intHandler* )

Registers an interrupt handler for the power system interrupt.

#### Parameters

<i>intHandler</i>	is a pointer to the function to be called when the power system interrupt occurs.
-------------------	---

This function registers the handler to be called when a clock system interrupt occurs. This function enables the global interrupt in the interrupt controller; specific PCM interrupts must be enabled via [PCM\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [PCM\\_clearInterruptFlag](#).

#### See Also

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

#### Returns

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 14.7.2.18 bool PCM\_setCoreVoltageLevel ( uint\_fast8\_t *voltageLevel* )

Sets the core voltage level (*V<sub>core</sub>*). The function will take care of all power state transitions needed to shift between core voltage levels. Because transitions between voltage levels may require changes power modes, the power mode might temporarily be change. The power mode will be returned to the original state (with the new voltage level) at the end of a successful execution of this function.

Refer to the device specific data sheet for specifics about core voltage levels.

#### Parameters

<i>voltageLevel</i>	The voltage level to be shifted to. <ul style="list-style-type: none"> <li>■ <b>PCM_VCORE0</b>,</li> <li>■ <b>PCM_VCORE1</b></li> </ul>
---------------------	---

#### Returns

true if voltage level set, false otherwise.

#### 14.7.2.19 bool PCM\_setCoreVoltageLevelNonBlocking ( uint\_fast8\_t *voltageLevel* )

Sets the core voltage level (Vcore). This function is similar to PCM\_setCoreVoltageLevel, however there are no polling flags to ensure a state has changed. Execution is returned back to the calling program correctly. For MSP432, changing into different power modes/states require very specific logic. This function will initiate only one state transition and then return. It is up to the user to keep calling this function until the correct power state has been achieved.

Refer to the device specific data sheet for specifics about core voltage levels.

##### Parameters

<i>voltageLevel</i>	The voltage level to be shifted to. <ul style="list-style-type: none"> <li>■ PCM_VCORE0,</li> <li>■ PCM_VCORE1</li> </ul>
---------------------	--

##### Returns

true if voltage level set, false otherwise.

#### 14.7.2.20 bool PCM\_setCoreVoltageLevelWithTimeout ( uint\_fast8\_t *voltageLevel*, uint32\_t *timeOut* )

Sets the core voltage level (Vcore). This function will take care of all power state transitions needed to shift between core voltage levels. Because transitions between voltage levels may require changes power modes, the power mode might temporarily be change. The power mode will be returned to the original state (with the new voltage level) at the end of a successful execution of this function.

This function is similar to PCMSetCoreVoltageLevel, however a timeout mechanism is used.

Refer to the device specific data sheet for specifics about core voltage levels.

##### Parameters

<i>voltageLevel</i>	The voltage level to be shifted to. <ul style="list-style-type: none"> <li>■ PCM_VCORE0,</li> <li>■ PCM_VCORE1</li> </ul>
<i>timeOut</i>	Number of loop iterations to timeout when checking for power state transitions. This should be used for debugging initial power/hardware configurations. After a stable hardware base is established, the PCMSetCoreVoltageLevel function should be used

##### Returns

true if voltage level set, false otherwise.

#### 14.7.2.21 bool PCM\_setPowerMode ( uint\_fast8\_t *powerMode* )

Switches between power modes. This function will take care of all power state transitions needed to shift between power modes. Note for changing to DCDC mode, specific hardware considerations are required.

Refer to the device specific data sheet for specifics about power modes.



**Parameters**

<i>powerMode</i>	The voltage modes to be shifted to. Valid values are: <ul style="list-style-type: none"> <li>■ <b>PCM_LDO_MODE,</b></li> <li>■ <b>PCM_DCDC_MODE,</b></li> <li>■ <b>PCM_LF_MODE</b></li> </ul>
------------------	---

**Returns**

true if power mode is set, false otherwise.

Referenced by [PCM\\_gotoLPM3\(\)](#).

#### 14.7.2.22 bool PCM\_setPowerModeNonBlocking ( uint\_fast8\_t *powerMode* )

Sets the core voltage level (Vcore). This function is similar to PCM\_setPowerMode, however there are no polling flags to ensure a state has changed. Execution is returned back to the calling program correctly. For MSP432, changing into different power modes/states require very specific logic. This function will initiate only one state transition and then return. It is up to the user to keep calling this function until the correct power state has been achieved.

Refer to the device specific data sheet for specifics about core voltage levels.

**Parameters**

<i>powerMode</i>	The voltage modes to be shifted to. Valid values are: <ul style="list-style-type: none"> <li>■ <b>PCM_LDO_MODE,</b></li> <li>■ <b>PCM_DCDC_MODE,</b></li> <li>■ <b>PCM_LF_MODE</b></li> </ul>
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**Returns**

true if power mode change was initiated, false otherwise

#### 14.7.2.23 bool PCM\_setPowerModeWithTimeout ( uint\_fast8\_t *powerMode*, uint32\_t *timeOut* )

Switches between power modes. This function will take care of all power state transitions needed to shift between power modes. Note for changing to DCDC mode, specific hardware considerations are required.

This function is similar to PCMSetPowerMode, however a timeout mechanism is used.

Refer to the device specific data sheet for specifics about power modes.

**Parameters**

<i>powerMode</i>	The voltage modes to be shifted to. Valid values are: <ul style="list-style-type: none"> <li>■ <b>PCM_LDO_MODE</b>,</li> <li>■ <b>PCM_DCDC_MODE</b>,</li> <li>■ <b>PCM_LF_MODE</b></li> </ul>
<i>timeOut</i>	Number of loop iterations to timeout when checking for power state transitions. This should be used for debugging initial power/hardware configurations. After a stable hardware base is established, the PCMSetPowerMode function should be used

**Returns**

true if power mode is set, false otherwise.

#### 14.7.2.24 bool PCM\_setPowerState ( uint\_fast8\_t *powerState* )

Switches between power states. This is a convenience function that combines the functionality of PCM\_setPowerMode and PCM\_setCoreVoltageLevel as well as the LPM0/LPM3 functions.

Refer to the device specific data sheet for specifics about power states.

**Parameters**

<i>powerState</i>	The voltage modes to be shifted to. Valid values are: <ul style="list-style-type: none"> <li>■ <b>PCM_AM_LDO_VCORE0</b>, [Active Mode, LDO, VCORE0]</li> <li>■ <b>PCM_AM_LDO_VCORE1</b>, [Active Mode, LDO, VCORE1]</li> <li>■ <b>PCM_AM_DCDC_VCORE0</b>, [Active Mode, DCDC, VCORE0]</li> <li>■ <b>PCM_AM_DCDC_VCORE1</b>, [Active Mode, DCDC, VCORE1]</li> <li>■ <b>PCM_AM_LF_VCORE0</b>, [Active Mode, Low Frequency, VCORE0]</li> <li>■ <b>PCM_AM_LF_VCORE1</b>, [Active Mode, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM0_LDO_VCORE0</b>, [LMP0, LDO, VCORE0]</li> <li>■ <b>PCM_LPM0_LDO_VCORE1</b>, [LMP0, LDO, VCORE1]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE0</b>, [LMP0, DCDC, VCORE0]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE1</b>, [LMP0, DCDC, VCORE1]</li> <li>■ <b>PCM_LPM0_LF_VCORE0</b>, [LMP0, Low Frequency, VCORE0]</li> <li>■ <b>PCM_LPM0_LF_VCORE1</b>, [LMP0, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM3</b>, [LPM3]</li> <li>■ <b>PCM_LPM35_VCORE0</b>, [LPM3.5 VCORE 0]</li> <li>■ <b>PCM_LPM4</b>, [LPM4]</li> <li>■ <b>PCM_LPM45</b>, [LPM4.5]</li> </ul>
-------------------	---

**Returns**

true if power state is set, false otherwise.

Referenced by [PCM\\_gotoLPM3\(\)](#).

### 14.7.2.25 bool PCM\_setPowerStateNonBlocking ( uint\_fast8\_t *powerState* )

Sets the power state of the part. This function is similar to PCM\_getPowerState, however there are no polling flags to ensure a state has changed. Execution is returned back to the calling program correctly. For MSP432, changing into different power modes/states require very specific logic. This function will initiate only one state transition and then return. It is up to the user to keep calling this function until the correct power state has been achieved.

Refer to the device specific data sheet for specifics about core voltage levels.

#### Parameters

<i>powerState</i>	<p>The voltage modes to be shifted to. Valid values are:</p> <ul style="list-style-type: none"> <li>■ <b>PCM_AM_LDO_VCORE0</b>, [Active Mode, LDO, VCORE0]</li> <li>■ <b>PCM_AM_LDO_VCORE1</b>, [Active Mode, LDO, VCORE1]</li> <li>■ <b>PCM_AM_DCDC_VCORE0</b>, [Active Mode, DCDC, VCORE0]</li> <li>■ <b>PCM_AM_DCDC_VCORE1</b>, [Active Mode, DCDC, VCORE1]</li> <li>■ <b>PCM_AM_LF_VCORE0</b>, [Active Mode, Low Frequency, VCORE0]</li> <li>■ <b>PCM_AM_LF_VCORE1</b>, [Active Mode, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM0_LDO_VCORE0</b>, [LMP0, LDO, VCORE0]</li> <li>■ <b>PCM_LPM0_LDO_VCORE1</b>, [LMP0, LDO, VCORE1]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE0</b>, [LMP0, DCDC, VCORE0]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE1</b>, [LMP0, DCDC, VCORE1]</li> <li>■ <b>PCM_LPM0_LF_VCORE0</b>, [LMP0, Low Frequency, VCORE0]</li> <li>■ <b>PCM_LPM0_LF_VCORE1</b>, [LMP0, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM3</b>, [LPM3]</li> <li>■ <b>PCM_LPM35_VCORE0</b>, [LPM3.5 VCORE 0]</li> <li>■ <b>PCM_LPM45</b>, [LPM4.5]</li> </ul>
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#### Returns

true if power state change was initiated, false otherwise

### 14.7.2.26 bool PCM\_setPowerStateWithTimeout ( uint\_fast8\_t *powerState*, uint32\_t *timeout* )

Switches between power states. This is a convenience function that combines the functionality of PCM\_setPowerMode and PCM\_setCoreVoltageLevel as well as the LPM modes.

This function is similar to PCM\_setPowerState, however a timeout mechanism is used.

Refer to the device specific data sheet for specifics about power states.

#### Parameters

<i>powerState</i>	<p>The voltage modes to be shifted to. Valid values are:</p> <ul style="list-style-type: none"> <li>■ <b>PCM_AM_LDO_VCORE0</b>, [Active Mode, LDO, VCORE0]</li> <li>■ <b>PCM_AM_LDO_VCORE1</b>, [Active Mode, LDO, VCORE1]</li> <li>■ <b>PCM_AM_DCDC_VCORE0</b>, [Active Mode, DCDC, VCORE0]</li> <li>■ <b>PCM_AM_DCDC_VCORE1</b>, [Active Mode, DCDC, VCORE1]</li> <li>■ <b>PCM_AM_LF_VCORE0</b>, [Active Mode, Low Frequency, VCORE0]</li> <li>■ <b>PCM_AM_LF_VCORE1</b>, [Active Mode, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM0_LDO_VCORE0</b>, [LMP0, LDO, VCORE0]</li> <li>■ <b>PCM_LPM0_LDO_VCORE1</b>, [LMP0, LDO, VCORE1]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE0</b>, [LMP0, DCDC, VCORE0]</li> <li>■ <b>PCM_LPM0_DCDC_VCORE1</b>, [LMP0, DCDC, VCORE1]</li> <li>■ <b>PCM_LPM0_LF_VCORE0</b>, [LMP0, Low Frequency, VCORE0]</li> <li>■ <b>PCM_LPM0_LF_VCORE1</b>, [LMP0, Low Frequency, VCORE1]</li> <li>■ <b>PCM_LPM3</b>, [LPM3]</li> <li>■ <b>PCM_LPM35_VCORE0</b>, [LPM3.5 VCORE 0]</li> <li>■ <b>PCM_LPM4</b>, [LPM4]</li> <li>■ <b>PCM_LPM45</b>, [LPM4.5]</li> </ul>
<i>timeout</i>	<p>Number of loop iterations to timeout when checking for power state transitions. This should be used for debugging initial power/hardware configurations. After a stable hardware base is established, the PCMSetPowerMode function should be used</p>

**Returns**

true if power state is set, false otherwise. It is important to note that if a timeout occurs, false will be returned, however the power state at this point is not guaranteed to be the same as the state prior to the function call

#### 14.7.2.27 bool PCM\_shutdownDevice ( uint32\_t shutdownMode )

Transitions the device into LPM3.5/LPM4.5 mode.

Refer to the device specific data sheet for specifics about shutdown modes.

The following events will cause a wake up from LPM3.5 mode:

- Device reset
- External reset RST
- Enabled RTC, WDT, and wake-up I/O only interrupt events

The following events will cause a wake up from the LPM4.5 mode:

- Device reset
- External reset RST
- Wake-up I/O only interrupt events

**Parameters**

<i>shutdownMode</i>	Specific mode to go to. Valid values are: <ul style="list-style-type: none"><li>■ <b>PCM_LPM35_VCORE0</b></li><li>■ <b>PCM_LPM45</b></li></ul>
---------------------	--

**Returns**

false if shutdown state cannot be entered, true otherwise.

#### 14.7.2.28 void PCM\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the power system.

This function unregisters the handler to be called when a power system interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 15 Port Mapper (PMAP)

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## 15.1 Module Operation

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port pins.

The port mapping controller features are:

- Configuration protected by write access key.
- Default mapping provided for each port pin (device-dependent, the device pinout in the device-specific data sheet).
- Mapping can be reconfigured during runtime.
- Each output signal can be mapped to several output pins.

## 15.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the PMAP module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to use the PMAP module to redirect the output of a TimerA CCR register.

First is the array configuration to remap the port:

```
/* Port mapper configuration register */
const uint8_t port_mapping[] =
{
    //Port P2:
    PM_NONE, PM_NONE, PM_NONE, PM_NONE, PM_TA1CCR1A, PM_NONE, PM_NONE,
    PM_NONE
};
```

Next is the call to the actual PMAP API that persists the configuration:

```
/* Remapping TACCR0 to P2.4 */
MAP_PMAP_configurePorts((const uint8_t *) port_mapping, PMAP_P2MAP, 1,
    PMAP_DISABLE_RECONFIGURATION);
```

## 15.3 Definitions

### Functions

- void [PMAP\\_configurePorts](#) (const uint8\_t \*portMapping, uint8\_t pxMAPy, uint8\_t numberOfPorts, uint8\_t portMapReconfigure)

### 15.3.1 Detailed Description

The code for this module is contained in `driverlib/pmap.c`, with `driverlib/pmap.h` containing the API declarations for use by applications.

## 15.3.2 Function Documentation

15.3.2.1 void PMAP\_configurePorts ( const uint8\_t \* *portMapping*, uint8\_t *pxMAPy*, uint8\_t *numberOfPorts*, uint8\_t *portMapReconfigure* )

This function configures the MSP432 Port Mapper

### Parameters

<i>portMapping</i>	is the pointer to init Data
<i>pxMAPy</i>	is the Port Mapper to initialize
<i>numberOfPorts</i>	is the number of Ports to initialize
<i>portMapRecon- figure</i>	is used to enable/disable reconfiguration Valid values are <b>PMAP_ENABLE_RECONFIGURATION</b> <b>PMAP_DISABLE_RECONFIGURATION</b> [Default value] Modified registers are <b>PMAPKEYID</b> , <b>PMAPCTL</b>

### Returns

None



# 16 Power Supply System (PSS)

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## 16.1 Module Operation

The PSS module for the DriverLib allows the user to fully configure/setup the various analog power sources on the MSP432 device. This mainly involves enabling and disabling the high side supervisor/monitor. Performance modes of both the high side power supply can be configured and manipulated in order to optimize power efficiency. Additionally, the PSS interrupt can be configured to fire an interrupt on a power supply violation.

## 16.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the PSS module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to disable the high side power supervisor:

```
MAP_PSS_enableHighSide();
```

## 16.3 Definitions

### Functions

- void [PSS\\_clearInterruptFlag](#) (void)
- void [PSS\\_disableForcedDCDCOperation](#) (void)
- void [PSS\\_disableHighSide](#) (void)
- void [PSS\\_disableHighSideMonitor](#) (void)
- void [PSS\\_disableHighSidePinToggle](#) (void)
- void [PSS\\_disableInterrupt](#) (void)
- void [PSS\\_enableForcedDCDCOperation](#) (void)
- void [PSS\\_enableHighSide](#) (void)
- void [PSS\\_enableHighSideMonitor](#) (void)
- void [PSS\\_enableHighSidePinToggle](#) (bool activeLow)
- void [PSS\\_enableInterrupt](#) (void)
- uint\_fast8\_t [PSS\\_getHighSidePerformanceMode](#) (void)
- uint\_fast8\_t [PSS\\_getHighSideVoltageTrigger](#) (void)
- uint32\_t [PSS\\_getInterruptStatus](#) (void)
- void [PSS\\_registerInterrupt](#) (void(\*intHandler)(void))
- void [PSS\\_setHighSidePerformanceMode](#) (uint\_fast8\_t powerMode)
- void [PSS\\_setHighSideVoltageTrigger](#) (uint\_fast8\_t triggerVoltage)
- void [PSS\\_unregisterInterrupt](#) (void)

### 16.3.1 Detailed Description

The code for this module is contained in `driverlib/pss.c`, with `driverlib/pss.h` containing the API declarations for use by applications.

## 16.3.2 Function Documentation

### 16.3.2.1 void PSS\_clearInterruptFlag ( void )

Clears power supply system interrupt source.

**Returns**

None.

### 16.3.2.2 void PSS\_disableForcedDCDCOperation ( void )

Disables the "forced" mode of the DCDC regulator. In this mode, the fail safe mechanism that disables the regulator to LDO mode when the supply voltage falls below the minimum supply voltage required for DCDC operation is turned on.

**Returns**

None.

### 16.3.2.3 void PSS\_disableHighSide ( void )

Disables high side voltage supervisor/monitor.

**Returns**

None.

### 16.3.2.4 void PSS\_disableHighSideMonitor ( void )

Switches the high side of the power supply system to be a supervisor instead of a monitor

**Returns**

None.

### 16.3.2.5 void PSS\_disableHighSidePinToggle ( void )

Disables output of the High Side interrupt flag on the device **SVMHOUT** pin

**Returns**

None.

### 16.3.2.6 void PSS\_disableInterrupt ( void )

Disables the power supply system interrupt source.

**Returns**

None.

## 16.3.2.7 void PSS\_enableForcedDCDCOperation ( void )

Enables the "forced" mode of the DCDC regulator. In this mode, the fail safe mechanism that disables the regulator to LDO mode when the supply voltage falls below the minimum supply voltage required for DCDC operation is turned off.

**Returns**

None.

## 16.3.2.8 void PSS\_enableHighSide ( void )

Enables high side voltage supervisor/monitor.

**Returns**

None.

## 16.3.2.9 void PSS\_enableHighSideMonitor ( void )

Sets the high side voltage supervisor to monitor mode

**Returns**

None.

16.3.2.10 void PSS\_enableHighSidePinToggle ( bool *activeLow* )

Enables output of the High Side interrupt flag on the device **SVMHOUT** pin

**Parameters**

<i>activeLow</i>	True if the signal should be logic low when SVSMHIFG is set. False if signal should be high when <b>SVSMHIFG</b> is set.
------------------	--

**Returns**

None.

## 16.3.2.11 void PSS\_enableInterrupt ( void )

Enables the power supply system interrupt source.

**Returns**

None.

16.3.2.12 `uint_fast8_t PSS_getHighSidePerformanceMode ( void )`

Gets the performance mode of the high side voltage regulator. Refer to the user's guide for specific information about information about the different performance modes.

**Returns**

Performance mode of the voltage regulator

16.3.2.13 `uint_fast8_t PSS_getHighSideVoltageTrigger ( void )`

Returns the voltage level at which the high side of the device voltage regulator triggers a reset.

**Returns**

The voltage level that the high side voltage supervisor/monitor triggers a reset. This value is represented as an unsigned eight bit integer where only the lowest three bits are most significant. See [PSS\\_setHighSideVoltageTrigger](#) for information regarding the return value

16.3.2.14 `uint32_t PSS_getInterruptStatus ( void )`

Gets the current interrupt status.

**Returns**

The current interrupt status ( `PSS_SVSMH` )

16.3.2.15 `void PSS_registerInterrupt ( void(*)(void) intHandler )`

Registers an interrupt handler for the power supply system interrupt.

**Parameters**

<code><i>intHandler</i></code>	is a pointer to the function to be called when the power supply system interrupt occurs.
--------------------------------	--

This function registers the handler to be called when a power supply system interrupt occurs. This function enables the global interrupt in the interrupt controller; specific PSS interrupts must be enabled via [PSS\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [PSS\\_clearInterruptFlag\(\)](#).

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 16.3.2.16 void PSS\_setHighSidePerformanceMode ( uint\_fast8\_t *powerMode* )

Sets the performance mode of the high side regulator. Full performance mode allows for the best response times while normal performance mode is optimized for the lowest possible current consumption.

**Parameters**

<i>powerMode</i>	is the performance mode to set. Valid values are one of the following: <ul style="list-style-type: none"> <li>■ <b>PSS_FULL_PERFORMANCE_MODE,</b></li> <li>■ <b>PSS_NORMAL_PERFORMANCE_MODE</b></li> </ul>
------------------	--

**Returns**

None.

16.3.2.17 void PSS\_setHighSideVoltageTrigger ( uint\_fast8\_t *triggerVoltage* )

Sets the voltage level at which the high side of the device voltage regulator triggers a reset. This value is represented as an unsigned eight bit integer where only the lowest three bits are most significant.

**Parameters**

<i>triggerVoltage</i>	Voltage level in which high side supervisor/monitor triggers a reset. See the device specific data sheet for details on these voltage levels.
-----------------------	---

Typical values will vary from part to part (so it is very important to check the SVSH section of the data sheet. For reference only, the typical MSP432 101 values are listed below:

- 0 → 1.57V
- 1 → 1.62V
- 2 → 1.83V
- 3 → 2V
- 4 → 2.25V
- 5 → 2.4V
- 6 → 2.6V
- 7 → 2.8V

**Returns**

None.

## 16.3.2.18 void PSS\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the power supply system

This function unregisters the handler to be called when a power supply system interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 17 Reference Module (REF\_A)

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## 17.1 Module Operation

The Internal Reference (REF\_A) API provides a set of functions for using the MSPWare REF\_A modules. Functions are provided to setup and enable use of the Reference voltage, enable or disable the internal temperature sensor, and view the status of the inner workings of the REF module.

The reference module (REF\_A) is responsible for generation of all critical reference voltages that can be used by various analog peripherals in a given device. The heart of the reference system is the bandgap from which all other references are derived by unity or non-inverting gain stages. The REFGEN sub-system consists of the bandgap, the bandgap bias, and the non-inverting buffer stage which generates the three primary voltage reference available in the system, namely 1.2 V, 1.45, 2.0 V, and 2.5 V. In addition, when enabled, a buffered bandgap voltage is available.

## 17.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the REF\_A module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to enable the REF\_A module for a 2.5v reference:

```
/* Setting reference voltage to 2.5 and enabling reference */
MAP_REF_A_setReferenceVoltage(REF_A_VREF2_5V);
MAP_REF_A_enableReferenceVoltage();
```



## 17.3 Definitions

### Functions

- void [REF\\_A\\_disableReferenceVoltage](#) (void)
- void [REF\\_A\\_disableReferenceVoltageOutput](#) (void)
- void [REF\\_A\\_disableTempSensor](#) (void)
- void [REF\\_A\\_enableReferenceVoltage](#) (void)
- void [REF\\_A\\_enableReferenceVoltageOutput](#) (void)
- void [REF\\_A\\_enableTempSensor](#) (void)
- uint\_fast8\_t [REF\\_A\\_getBandgapMode](#) (void)
- bool [REF\\_A\\_getBufferedBandgapVoltageStatus](#) (void)
- bool [REF\\_A\\_getVariableReferenceVoltageStatus](#) (void)
- bool [REF\\_A\\_isBandgapActive](#) (void)
- bool [REF\\_A\\_isRefGenActive](#) (void)
- bool [REF\\_A\\_isRefGenBusy](#) (void)
- void [REF\\_A\\_setBufferedBandgapVoltageOneTimeTrigger](#) (void)
- void [REF\\_A\\_setReferenceVoltage](#) (uint\_fast8\_t referenceVoltageSelect)
- void [REF\\_A\\_setReferenceVoltageOneTimeTrigger](#) (void)

### 17.3.1 Detailed Description

The code for this module is contained in `driverlib/ref_a.c`, with `driverlib/ref_a.h` containing the API declarations for use by applications.

## 17.3.2 Function Documentation

### 17.3.2.1 void REF\_A\_disableReferenceVoltage ( void )

Disables the reference voltage.

This function is used to disable the generated reference voltage. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFON** of **REFCTL0** register.

#### Returns

none

### 17.3.2.2 void REF\_A\_disableReferenceVoltageOutput ( void )

Disables the reference voltage as an output to a pin.

This function is used to disables the reference voltage being generated to be given to an output pin. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFOUT** of **REFCTL0** register.

#### Returns

none

### 17.3.2.3 void REF\_A\_disableTempSensor ( void )

Disables the internal temperature sensor to save power consumption.

This function is used to turn off the internal temperature sensor to save on power consumption. The temperature sensor is enabled by default. Please note, that giving ADC12 module control over the REF module, the state of the temperature sensor is dependent on the controls of the ADC12 module. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFTCOFF** of **REFCTL0** register.

#### Returns

none

### 17.3.2.4 void REF\_A\_enableReferenceVoltage ( void )

Enables the reference voltage to be used by peripherals.

This function is used to enable the generated reference voltage to be used other peripherals or by an output pin, if enabled. Please note, that giving ADC12 module control over the REF module, the state of the reference voltage is dependent on the controls of the ADC12 module. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFON** of **REFCTL0** register.

**Returns**

none

**17.3.2.5 void REF\_A\_enableReferenceVoltageOutput ( void )**

Outputs the reference voltage to an output pin.

This function is used to output the reference voltage being generated to an output pin. Please note, the output pin is device specific. Please note, that giving ADC12 module control over the REF module, the state of the reference voltage as an output to a pin is dependent on the controls of the ADC12 module. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFOUT** of **REFCTL0** register.

**Returns**

none

**17.3.2.6 void REF\_A\_enableTempSensor ( void )**

Enables the internal temperature sensor.

This function is used to turn on the internal temperature sensor to use by other peripherals. The temperature sensor is enabled by default. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_A\_BUSY**, this function will have no effect.

Modified bits are **REFTCOFF** of **REFCTL0** register.

**Returns**

none

**17.3.2.7 uint\_fast8\_t REF\_A\_getBandgapMode ( void )**

Returns the bandgap mode of the REF module.

This function is used to return the bandgap mode of the REF module, requested by the peripherals using the bandgap. If a peripheral requests static mode, then the bandgap mode will be static for all modules, whereas if all of the peripherals using the bandgap request sample mode, then that will be the mode returned. Sample mode allows the bandgap to be active only when necessary to save on power consumption, static mode requires the bandgap to be active until no peripherals are using it anymore.

**Returns**

The bandgap mode of the REF module:

- **REF\_A\_STATICMODE** if the bandgap is operating in static mode
- **REF\_A\_SAMPLEMODE** if the bandgap is operating in sample mode

### 17.3.2.8 bool REF\_A\_getBufferedBandgapVoltageStatus ( void )

Returns the busy status of the reference generator in the REF module.

This function is used to return the busy status of the buffered bandgap voltage in the REF module. If the ref. generator is on and ready to use, then the status will be seen as active.

**Returns**

true if the buffered bandgap voltage is ready to be used, false otherwise

### 17.3.2.9 bool REF\_A\_getVariableReferenceVoltageStatus ( void )

Returns the busy status of the variable reference voltage in the REF module.

This function is used to return the busy status of the variable reference voltage in the REF module. If the ref. generator is on and ready to use, then the status will be seen as active.

**Returns**

true if the variable bandgap voltage is ready to be used, false otherwise

### 17.3.2.10 bool REF\_A\_isBandgapActive ( void )

Returns the active status of the bandgap in the REF module.

This function is used to return the active status of the bandgap in the REF module. If the bandgap is in use by a peripheral, then the status will be seen as active.

**Returns**

true if the bandgap is being used, false otherwise

### 17.3.2.11 bool REF\_A\_isRefGenActive ( void )

Returns the active status of the reference generator in the REF module.

This function is used to return the active status of the reference generator in the REF module. If the ref. generator is on and ready to use, then the status will be seen as active.

**Returns**

true if the reference generator is active, false otherwise.

### 17.3.2.12 bool REF\_A\_isRefGenBusy ( void )

Returns the busy status of the reference generator in the REF module.

This function is used to return the busy status of the reference generator in the REF module. If the ref. generator is in use by a peripheral, then the status will be seen as busy.

**Returns**

true if the reference generator is being used, false otherwise.

## 17.3.2.13 void REF\_A\_setBufferedBandgapVoltageOneTimeTrigger ( void )

Enables the one-time trigger of the buffered bandgap voltage.

Triggers the one-time generation of the buffered bandgap voltage. Once the buffered bandgap voltage request is set, this bit is cleared by hardware

Modified bits are **RefGOT** of **REFCTL0** register.

**Returns**

none

17.3.2.14 void REF\_A\_setReferenceVoltage ( uint\_fast8\_t *referenceVoltageSelect* )

Sets the reference voltage for the voltage generator.

**Parameters**

<i>referenceVoltageSelect</i>	is the desired voltage to generate for a reference voltage. Valid values are: <ul style="list-style-type: none"> <li>■ <b>REF_A_VREF1_2V</b> [Default]</li> <li>■ <b>REF_A_VREF1_45V</b></li> <li>■ <b>REF_A_VREF2_5V</b> Modified bits are <b>REFVSEL</b> of <b>REFCTL0</b> register.</li> </ul>
-------------------------------	---

This function sets the reference voltage generated by the voltage generator to be used by other peripherals. This reference voltage will only be valid while the REF module is in control. Please note, if the [REF\\_A\\_isRefGenBusy\(\)](#) returns **REF\_BUSY**, this function will have no effect.

**Returns**

none

## 17.3.2.15 void REF\_A\_setReferenceVoltageOneTimeTrigger ( void )

Enables the one-time trigger of the reference voltage.

Triggers the one-time generation of the variable reference voltage. Once the reference voltage request is set, this bit is cleared by hardware

Modified bits are **REFGENOT** of **REFCTL0** register.

**Returns**

none

## 18 Reset Controller (ResetCtl)

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### 18.1 Module Operation

The DriverLib APIs for the MSP432 Reset Control are a set of power functions that enables programmers to manipulate all aspects of a system reset. The user is able to initiate both hard and soft resets as well as determine the cause of a prior system reset.

### 18.2 Reset Sources

Reset sources will vary from device to device (see the device specific datasheet for the reset source mappings relevant to your device). The ResetCtl for DriverLib defines a set of generic reset sources (such as RESET\_SRC\_0). In practice, it is a good idea to use a define statement to match these to a specific reset source. For example, MSP432's mapping could look something similar to the following:

```
#define RESET_SYSTEM_SRC    RESET_SRC_0
#define RESET_WDTTIME_SRC  RESET_SRC_1
#define RESET_WDTPW_SRC    RESET_SRC_2
#define RESET_CS_SRC       RESET_SRC_3
#define RESET_PCM_SRC      RESET_SRC_14
#define RESET_SYS_SRC      RESET_SRC_15
```

By defining these extra set of macros, the user code that accesses the DriverLib ResetCtl APIs are more legible. For example, when checking to see if a device was reset because of a CS violation (such as a XTAL fault), the user could write code similar to the following:

```
if(ResetCtl_getSoftResetSource() == RESET_CS_SRC)
{
    // Do reset handling here
}
```

### 18.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the ResetCtl module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing an ISR that initiates a software reset of the device. The idea here is that a push button could cause a software initiated reset.

```
/* GPIO ISR */
void PORT1_IRQHandler(void)
{
    uint32_t status;

    status = MAP_GPIO_getEnabledInterruptStatus(GPIO_PORT_P1);
    MAP_GPIO_clearInterruptFlag(GPIO_PORT_P1, status);

    /* Initiated a hard reset */
    if(status & GPIO_PIN1)
    {
        MAP_ResetCtl_initiateHardReset();
    }
}
```

## 18.4 Definitions

### Functions

- void [ResetCtl\\_clearHardResetSource](#) (uint32\_t mask)
- void [ResetCtl\\_clearPCMFlags](#) (void)
- void [ResetCtl\\_clearPSSFlags](#) (void)
- void [ResetCtl\\_clearSoftResetSource](#) (uint32\_t mask)
- uint32\_t [ResetCtl\\_getHardResetSource](#) (void)
- uint32\_t [ResetCtl\\_getPCMSource](#) (void)
- uint32\_t [ResetCtl\\_getPSSSource](#) (void)
- uint32\_t [ResetCtl\\_getSoftResetSource](#) (void)
- void [ResetCtl\\_initiateHardReset](#) (void)
- void [ResetCtl\\_initiateHardResetWithSource](#) (uint32\_t source)
- void [ResetCtl\\_initiateSoftReset](#) (void)
- void [ResetCtl\\_initiateSoftResetWithSource](#) (uint32\_t source)

### 18.4.1 Detailed Description

The code for this module is contained in `driverlib/reset.c`, with `driverlib/reset.h` containing the API declarations for use by applications.



## 18.4.2 Function Documentation

### 18.4.2.1 void ResetCtl\_clearHardResetSource ( uint32\_t mask )

Clears the reset sources associated with at hard reset

#### Parameters

<i>mask</i>	<p>- Bitwise OR of any of the following values:</p> <ul style="list-style-type: none"> <li>■ RESET_SRC_0,</li> <li>■ RESET_SRC_1,</li> <li>■ RESET_SRC_2,</li> <li>■ RESET_SRC_3,</li> <li>■ RESET_SRC_4,</li> <li>■ RESET_SRC_5,</li> <li>■ RESET_SRC_6,</li> <li>■ RESET_SRC_7,</li> <li>■ RESET_SRC_8,</li> <li>■ RESET_SRC_9,</li> <li>■ RESET_SRC_10,</li> <li>■ RESET_SRC_11,</li> <li>■ RESET_SRC_12,</li> <li>■ RESET_SRC_13,</li> <li>■ RESET_SRC_14,</li> <li>■ RESET_SRC_15</li> </ul>
-------------	---

#### Returns

none

### 18.4.2.2 void ResetCtl\_clearPCMFlags ( void )

Clears the corresponding PCM reset source flags

#### Returns

none

### 18.4.2.3 void ResetCtl\_clearPSSFlags ( void )

Clears the PSS reset source flags

#### Returns

none

18.4.2.4 void ResetCtl\_clearSoftResetSource ( uint32\_t *mask* )

Clears the reset sources associated with at soft reset

## Parameters

<i>mask</i>	<p>- Bitwise OR of any of the following values:</p> <ul style="list-style-type: none"> <li>■ RESET_SRC_0,</li> <li>■ RESET_SRC_1,</li> <li>■ RESET_SRC_2,</li> <li>■ RESET_SRC_3,</li> <li>■ RESET_SRC_4,</li> <li>■ RESET_SRC_5,</li> <li>■ RESET_SRC_6,</li> <li>■ RESET_SRC_7,</li> <li>■ RESET_SRC_8,</li> <li>■ RESET_SRC_9,</li> <li>■ RESET_SRC_10,</li> <li>■ RESET_SRC_11,</li> <li>■ RESET_SRC_12,</li> <li>■ RESET_SRC_13,</li> <li>■ RESET_SRC_14,</li> <li>■ RESET_SRC_15</li> </ul>
-------------	---

**Returns**

none

## 18.4.2.5 uint32\_t ResetCtl\_getHardResetSource ( void )

Retrieves previous hard reset sources

**Returns**

the bitwise or of previous reset sources. These sources must be cleared using the [ResetCtl\\_clearHardResetSource](#) function to be cleared. Possible values include:

- RESET\_SRC\_0,
- RESET\_SRC\_1,
- RESET\_SRC\_2,
- RESET\_SRC\_3,
- RESET\_SRC\_4,
- RESET\_SRC\_5,
- RESET\_SRC\_6,
- RESET\_SRC\_7,
- RESET\_SRC\_8,
- RESET\_SRC\_9,
- RESET\_SRC\_10,
- RESET\_SRC\_11,
- RESET\_SRC\_12,

- RESET\_SRC\_13,
- RESET\_SRC\_14,
- RESET\_SRC\_15

#### 18.4.2.6 uint32\_t ResetCtl\_getPCMSource ( void )

Indicates the last cause of a power-on reset (POR) due to PCM operation.

##### Returns

Bitwise OR of any of the following values:

- RESET\_LPM35,
- RESET\_LPM45

#### 18.4.2.7 uint32\_t ResetCtl\_getPSSSource ( void )

Indicates the last cause of a power-on reset (POR) due to PSS operation. Note that the bits returned from this function may be set in different combinations. When a cold power up occurs, the value of all the values ORed together could be returned as a cold power up causes these conditions.

##### Returns

Bitwise OR of any of the following values:

- RESET\_VCCDET,
- RESET\_SVSH\_TRIP,
- RESET\_BGREF\_BAD

#### 18.4.2.8 uint32\_t ResetCtl\_getSoftResetSource ( void )

Retrieves previous soft reset sources

##### Returns

the bitwise or of previous reset sources. These sources must be cleared using the [ResetCtl\\_clearSoftResetSource](#) function to be cleared. Possible values include:

- RESET\_SRC\_0,
- RESET\_SRC\_1,
- RESET\_SRC\_2,
- RESET\_SRC\_3,
- RESET\_SRC\_4,
- RESET\_SRC\_5,
- RESET\_SRC\_6,
- RESET\_SRC\_7,
- RESET\_SRC\_8,
- RESET\_SRC\_9,
- RESET\_SRC\_10,
- RESET\_SRC\_11,

- RESET\_SRC\_12,
- RESET\_SRC\_13,
- RESET\_SRC\_14,
- RESET\_SRC\_15

#### 18.4.2.9 void ResetCtl\_initiateHardReset ( void )

Initiates a hard system reset.

##### Returns

none

#### 18.4.2.10 void ResetCtl\_initiateHardResetWithSource ( uint32\_t source )

Initiates a hard system reset with a particular source given. This source is generic and can be assigned by the user.

##### Parameters

<i>source</i>	<p>- Valid values are one the following values:</p> <ul style="list-style-type: none"> <li>■ RESET_SRC_0,</li> <li>■ RESET_SRC_1,</li> <li>■ RESET_SRC_2,</li> <li>■ RESET_SRC_3,</li> <li>■ RESET_SRC_4,</li> <li>■ RESET_SRC_5,</li> <li>■ RESET_SRC_6,</li> <li>■ RESET_SRC_7,</li> <li>■ RESET_SRC_8,</li> <li>■ RESET_SRC_9,</li> <li>■ RESET_SRC_10,</li> <li>■ RESET_SRC_11,</li> <li>■ RESET_SRC_12,</li> <li>■ RESET_SRC_13,</li> <li>■ RESET_SRC_14,</li> <li>■ RESET_SRC_15</li> </ul>
---------------	---

##### Returns

none

## 18.4.2.11 void ResetCtl\_initiateSoftReset ( void )

Initiates a soft system reset.

**Returns**  
none

18.4.2.12 void ResetCtl\_initiateSoftResetWithSource ( uint32\_t *source* )

Initiates a soft system reset with a particular source given. This source is generic and can be assigned by the user.

**Parameters**

<i>source</i>	<p>Source of the reset. Valid values are:</p> <ul style="list-style-type: none"> <li>■ RESET_SRC_0,</li> <li>■ RESET_SRC_1,</li> <li>■ RESET_SRC_2,</li> <li>■ RESET_SRC_3,</li> <li>■ RESET_SRC_4,</li> <li>■ RESET_SRC_5,</li> <li>■ RESET_SRC_6,</li> <li>■ RESET_SRC_7,</li> <li>■ RESET_SRC_8,</li> <li>■ RESET_SRC_9,</li> <li>■ RESET_SRC_10,</li> <li>■ RESET_SRC_11,</li> <li>■ RESET_SRC_12,</li> <li>■ RESET_SRC_13,</li> <li>■ RESET_SRC_14,</li> <li>■ RESET_SRC_15</li> </ul>
---------------	---

**Returns**  
none

# 19 Real Time Clock (RTC\_C)

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## 19.1 Module Operation

The Real Time Clock (RTC\_C) API provides a set of functions for using the MSPWare L RTC\_C modules. Functions are provided to calibrate the clock, initialize the RTC\_C modules in Calendar mode, and setup conditions for, and enable, interrupts for the RTC\_C modules.

The RTC\_C module provides the ability to keep track of the current time and date in calendar mode.

The RTC\_C module generates multiple interrupts. There are 2 interrupts that can be defined in calendar mode, and 1 interrupt in counter mode for counter overflow, as well as an interrupt for each prescaler.

## 19.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the RTC\_C module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the RTC\_C module and create a calendar event.

The following is the configuration structure that sets the date:

```

/* Time is November 12th 1955 10:03:00 PM */
const RTC_C_Calendar currentTime =
{
    0x00,
    0x03,
    0x22,
    0x12,
    0x11,
    0x1955
};

```

Next are the actual calls to DriverLib that configure the module:

```

/* Initializing RTC with current time as described in time in
 * definitions section */
MAP_RTC_C_initCalendar(&currentTime, RTC_C_FORMAT_BCD);

/* Setup Calendar Alarm for 10:04pm (for the flux capacitor) */
MAP_RTC_C_setCalendarAlarm(0x04, 0x22, RTC_C_ALARMCONDITION_OFF,
    RTC_C_ALARMCONDITION_OFF);

/* Specify an interrupt to assert every minute */
MAP_RTC_C_setCalendarEvent(RTC_C_CALENDAREVENT_MINUTECHANGE);

/* Enable interrupt for RTC Ready Status, which asserts when the RTC
 * Calendar registers are ready to read.
 * Also, enable interrupts for the Calendar alarm and Calendar event. */
MAP_RTC_C_clearInterruptFlag(
    RTC_C_CLOCK_READ_READY_INTERRUPT | RTC_C_TIME_EVENT_INTERRUPT
    | RTC_C_CLOCK_ALARM_INTERRUPT);
MAP_RTC_C_enableInterrupt(
    RTC_C_CLOCK_READ_READY_INTERRUPT | RTC_C_TIME_EVENT_INTERRUPT
    | RTC_C_CLOCK_ALARM_INTERRUPT);

/* Start RTC Clock */
MAP_RTC_C_startClock();

```



## 19.3 Definitions

### Functions

- void [RTC\\_C\\_clearInterruptFlag](#) (uint\_fast8\_t interruptFlagMask)
- uint16\_t [RTC\\_C\\_convertBCDToBinary](#) (uint16\_t valueToConvert)
- uint16\_t [RTC\\_C\\_convertBinaryToBCD](#) (uint16\_t valueToConvert)
- void [RTC\\_C\\_definePrescaleEvent](#) (uint\_fast8\_t prescaleSelect, uint\_fast8\_t prescaleEventDivider)
- void [RTC\\_C\\_disableInterrupt](#) (uint8\_t interruptMask)
- void [RTC\\_C\\_enableInterrupt](#) (uint8\_t interruptMask)
- RTC\_C\_Calendar [RTC\\_C\\_getCalendarTime](#) (void)
- uint\_fast8\_t [RTC\\_C\\_getEnabledInterruptStatus](#) (void)
- uint\_fast8\_t [RTC\\_C\\_getInterruptStatus](#) (void)
- uint\_fast8\_t [RTC\\_C\\_getPrescaleValue](#) (uint\_fast8\_t prescaleSelect)
- void [RTC\\_C\\_holdClock](#) (void)
- void [RTC\\_C\\_initCalendar](#) (const RTC\_C\_Calendar \*calendarTime, uint\_fast16\_t formatSelect)
- void [RTC\\_C\\_registerInterrupt](#) (void(\*intHandler)(void))
- void [RTC\\_C\\_setCalendarAlarm](#) (uint\_fast8\_t minutesAlarm, uint\_fast8\_t hoursAlarm, uint\_fast8\_t dayOfWeekAlarm, uint\_fast8\_t dayOfMonthAlarm)
- void [RTC\\_C\\_setCalendarEvent](#) (uint\_fast16\_t eventSelect)
- void [RTC\\_C\\_setCalibrationData](#) (uint\_fast8\_t offsetDirection, uint\_fast8\_t offsetValue)
- void [RTC\\_C\\_setCalibrationFrequency](#) (uint\_fast16\_t frequencySelect)
- void [RTC\\_C\\_setPrescaleValue](#) (uint\_fast8\_t prescaleSelect, uint\_fast8\_t prescaleCounterValue)
- bool [RTC\\_C\\_setTemperatureCompensation](#) (uint\_fast16\_t offsetDirection, uint\_fast8\_t offsetValue)
- void [RTC\\_C\\_startClock](#) (void)
- void [RTC\\_C\\_unregisterInterrupt](#) (void)

### 19.3.1 Detailed Description

The code for this module is contained in `driverlib/rtc_c.c`, with `driverlib/rtc_c.h` containing the API declarations for use by applications.

## 19.3.2 Function Documentation

### 19.3.2.1 void RTC\_C\_clearInterruptFlag ( uint\_fast8\_t *interruptFlagMask* )

Clears selected RTC interrupt flags.

#### Parameters

<i>interruptFlag-Mask</i>	<p>is a bit mask of the interrupt flags to be cleared. Mask Value is the logical OR of any of the following</p> <ul style="list-style-type: none"> <li>■ <b>RTC_C_TIME_EVENT_INTERRUPT</b> - asserts when counter overflows in counter mode or when Calendar event condition defined by <code>defineCalendarEvent()</code> is met.</li> <li>■ <b>RTC_C_CLOCK_ALARM_INTERRUPT</b> - asserts when alarm condition in Calendar mode is met.</li> <li>■ <b>RTC_C_CLOCK_READ_READY_INTERRUPT</b> - asserts when Calendar registers are settled.</li> <li>■ <b>RTC_C_PRESCALE_TIMER0_INTERRUPT</b> - asserts when Prescaler 0 event condition is met.</li> <li>■ <b>RTC_C_PRESCALE_TIMER1_INTERRUPT</b> - asserts when Prescaler 1 event condition is met.</li> <li>■ <b>RTC_C_OSCILLATOR_FAULT_INTERRUPT</b> - asserts if there is a problem with the 32kHz oscillator, while the RTC is running.</li> </ul>
---------------------------	---

This function clears the RTC interrupt flag is cleared, so that it no longer asserts.

#### Returns

None

### 19.3.2.2 uint16\_t RTC\_C\_convertBCDToBinary ( uint16\_t *valueToConvert* )

Returns the given BCD value in Binary Format

#### Parameters

<i>valueToConvert</i>	is the raw value in BCD format to convert to Binary.
-----------------------	--

This function converts BCD values to Binary format.

#### Returns

The Binary version of the `valueToConvert` parameter.

### 19.3.2.3 uint16\_t RTC\_C\_convertBinaryToBCD ( uint16\_t *valueToConvert* )

Returns the given Binary value in BCD Format

**Parameters**

<i>valueToConvert</i>	is the raw value in Binary format to convert to BCD.
-----------------------	--

This function converts Binary values to BCD format.

**Returns**

The BCD version of the *valueToConvert* parameter.

### 19.3.2.4 void RTC\_C\_definePrescaleEvent ( uint\_fast8\_t *prescaleSelect*, uint\_fast8\_t *prescaleEventDivider* )

Sets up an interrupt condition for the selected Prescaler.

**Parameters**

<i>prescaleSelect</i>	is the prescaler to define an interrupt for. Valid values are <ul style="list-style-type: none"> <li>■ RTC_C_PRESCALE_0</li> <li>■ RTC_C_PRESCALE_1</li> </ul>
<i>prescaleEvent-Divider</i>	is a divider to specify when an interrupt can occur based on the clock source of the selected prescaler. (Does not affect timer of the selected prescaler). Valid values are <ul style="list-style-type: none"> <li>■ RTC_C_PSEVENTDIVIDER_2 [Default]</li> <li>■ RTC_C_PSEVENTDIVIDER_4</li> <li>■ RTC_C_PSEVENTDIVIDER_8</li> <li>■ RTC_C_PSEVENTDIVIDER_16</li> <li>■ RTC_C_PSEVENTDIVIDER_32</li> <li>■ RTC_C_PSEVENTDIVIDER_64</li> <li>■ RTC_C_PSEVENTDIVIDER_128</li> <li>■ RTC_C_PSEVENTDIVIDER_256</li> </ul>

This function sets the condition for an interrupt to assert based on the individual prescalers.

**Returns**

None

19.3.2.5 void RTC\_C\_disableInterrupt ( uint8\_t *interruptMask* )

Disables selected RTC interrupt sources.

**Parameters**

<i>interruptMask</i>	<p>is a bit mask of the interrupts to disable. Mask Value is the logical OR of any of the following</p> <ul style="list-style-type: none"> <li>■ <b>RTC_C_TIME_EVENT_INTERRUPT</b> - asserts when counter overflows in counter mode or when Calendar event condition defined by <code>defineCalendarEvent()</code> is met.</li> <li>■ <b>RTC_C_CLOCK_ALARM_INTERRUPT</b> - asserts when alarm condition in Calendar mode is met.</li> <li>■ <b>RTC_CLOCK_READ_READY_INTERRUPT</b> - asserts when Calendar registers are settled.</li> <li>■ <b>RTC_C_PRESCALE_TIMER0_INTERRUPT</b> - asserts when Prescaler 0 event condition is met.</li> <li>■ <b>RTC_C_PRESCALE_TIMER1_INTERRUPT</b> - asserts when Prescaler 1 event condition is met.</li> <li>■ <b>RTC_C_OSCILLATOR_FAULT_INTERRUPT</b> - asserts if there is a problem with the 32kHz oscillator, while the RTC is running.</li> </ul>
----------------------	---

This function disables the selected RTC interrupt source. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Returns**

None

19.3.2.6 void RTC\_C\_enableInterrupt ( uint8\_t *interruptMask* )

Enables selected RTC interrupt sources.

**Parameters**

<i>interruptMask</i>	<p>is a bit mask of the interrupts to enable. Mask Value is the logical OR of any of the following</p> <ul style="list-style-type: none"> <li>■ <b>RTC_C_TIME_EVENT_INTERRUPT</b> - asserts when counter overflows in counter mode or when Calendar event condition defined by <code>defineCalendarEvent()</code> is met.</li> <li>■ <b>RTC_C_CLOCK_ALARM_INTERRUPT</b> - asserts when alarm condition in Calendar mode is met.</li> <li>■ <b>RTC_C_CLOCK_READ_READY_INTERRUPT</b> - asserts when Calendar registers are settled.</li> <li>■ <b>RTC_C_PRESCALE_TIMER0_INTERRUPT</b> - asserts when Prescaler 0 event condition is met.</li> <li>■ <b>RTC_C_PRESCALE_TIMER1_INTERRUPT</b> - asserts when Prescaler 1 event condition is met.</li> <li>■ <b>RTC_C_OSCILLATOR_FAULT_INTERRUPT</b> - asserts if there is a problem with the 32kHz oscillator, while the RTC is running.</li> </ul>
----------------------	--

This function enables the selected RTC interrupt source. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Returns**

None

### 19.3.2.7 RTC\_C\_Calendar RTC\_C\_getCalendarTime ( void )

Returns the Calendar Time stored in the Calendar registers of the RTC.

This function returns the current Calendar time in the form of a Calendar structure.

**Returns**

A Calendar structure containing the current time.

### 19.3.2.8 uint\_fast8\_t RTC\_C\_getEnabledInterruptStatus ( void )

Returns the status of the interrupts flags masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Returns**

A bit mask of the selected interrupt flag's status. Mask Value is the logical OR of any of the following

- **RTC\_TIME\_EVENT\_INTERRUPT** - asserts when counter overflows in counter mode or when Calendar event condition defined by `defineCalendarEvent()` is met.
- **RTC\_CLOCK\_ALARM\_INTERRUPT** - asserts when alarm condition in Calendar mode is met.
- **RTC\_CLOCK\_READ\_READY\_INTERRUPT** - asserts when Calendar registers are settled.

- **RTC\_C\_PRESCALE\_TIMER0\_INTERRUPT** - asserts when Prescaler 0 event condition is met.
- **RTC\_C\_PRESCALE\_TIMER1\_INTERRUPT** - asserts when Prescaler 1 event condition is met.
- **RTC\_OSCILLATOR\_FAULT\_INTERRUPT** - asserts if there is a problem with the 32kHz oscillator, while the RTC is running.

References [RTC\\_C\\_getInterruptStatus\(\)](#).

### 19.3.2.9 uint\_fast8\_t RTC\_C\_getInterruptStatus ( void )

Returns the status of the interrupts flags.

#### Returns

A bit mask of the selected interrupt flag's status. Mask Value is the logical OR of any of the following

- **RTC\_C\_TIME\_EVENT\_INTERRUPT** - asserts when counter overflows in counter mode or when Calendar event condition defined by `defineCalendarEvent()` is met.
- **RTC\_C\_CLOCK\_ALARM\_INTERRUPT** - asserts when alarm condition in Calendar mode is met.
- **RTC\_C\_CLOCK\_READ\_READY\_INTERRUPT** - asserts when Calendar registers are settled.
- **RTC\_C\_PRESCALE\_TIMER0\_INTERRUPT** - asserts when Prescaler 0 event condition is met.
- **RTC\_C\_PRESCALE\_TIMER1\_INTERRUPT** - asserts when Prescaler 1 event condition is met.
- **RTC\_C\_OSCILLATOR\_FAULT\_INTERRUPT** - asserts if there is a problem with the 32kHz oscillator, while the RTC is running.

Referenced by [RTC\\_C\\_getEnabledInterruptStatus\(\)](#).

### 19.3.2.10 uint\_fast8\_t RTC\_C\_getPrescaleValue ( uint\_fast8\_t *prescaleSelect* )

Returns the selected Prescaler value.

#### Parameters

<i>prescaleSelect</i>	is the prescaler to obtain the value of. Valid values are <ul style="list-style-type: none"> <li>■ <b>RTC_C_PRESCALE_0</b></li> <li>■ <b>RTC_C_PRESCALE_1</b></li> </ul>
-----------------------	--

This function returns the value of the selected prescale counter register. The counter should be held before reading. If in counter mode, the individual prescaler can be held, while in Calendar mode the whole RTC must be held.

#### Returns

The value of the specified Prescaler count register

## 19.3.2.11 void RTC\_C\_holdClock ( void )

Holds the RTC.

This function sets the RTC main hold bit to disable RTC functionality.

**Returns**

None

Referenced by [PCM\\_gotoLPM4\(\)](#).

19.3.2.12 void RTC\_C\_initCalendar ( const RTC\_C\_Calendar \* *calendarTime*,  
uint\_fast16\_t *formatSelect* )

Initializes the settings to operate the RTC in Calendar mode.

**Parameters**

<i>calendarTime</i>	is the structure containing the values for the Calendar to be initialized to. Valid values should be of type Calendar and should contain the following members and corresponding values: <ul style="list-style-type: none"> <li>■ <b>seconds</b> between 0-59</li> <li>■ <b>minutes</b> between 0-59</li> <li>■ <b>hours</b> between 0-24</li> <li>■ <b>dayOfWeek</b> between 0-6</li> <li>■ <b>dayOfMonth</b> between 0-31</li> <li>■ <b>year</b> between 0-4095</li> </ul>
---------------------	--

**Note**

Values beyond the ones specified may result in erratic behavior.

**Parameters**

<i>formatSelect</i>	is the format for the Calendar registers to use. Valid values are <ul style="list-style-type: none"> <li>■ <b>RTC_FORMAT_BINARY</b> [Default]</li> <li>■ <b>RTC_FORMAT_BCD</b></li> </ul>
---------------------	---

This function initializes the Calendar mode of the RTC module.

**Returns**

None

19.3.2.13 void RTC\_C\_registerInterrupt ( void(\*) (void) *intHandler* )

Registers an interrupt handler for the RTC interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the RTC interrupt occurs.
-------------------	--

This function registers the handler to be called when a RTC interrupt occurs. This function enables the global interrupt in the interrupt controller; specific AES interrupts must be enabled via `RTC_enableInterrupt()`. It is the interrupt handler's responsibility to clear the interrupt source via `RTC_clearInterruptFlag()`.

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

### 19.3.2.14 void RTC\_C\_setCalendarAlarm ( uint\_fast8\_t *minutesAlarm*, uint\_fast8\_t *hoursAlarm*, uint\_fast8\_t *dayOfWeekAlarm*, uint\_fast8\_t *dayOfMonthAlarm* )

Sets and Enables the desired Calendar Alarm settings.

**Parameters**

<i>minutesAlarm</i>	is the alarm condition for the minutes. Valid values are <ul style="list-style-type: none"> <li>■ An integer between 0-59, OR</li> <li>■ <b>RTC_C_ALARMCONDITION_OFF</b> [Default]</li> </ul>
<i>hoursAlarm</i>	is the alarm condition for the hours. Valid values are <ul style="list-style-type: none"> <li>■ An integer between 0-24, OR</li> <li>■ <b>RTC_C_ALARMCONDITION_OFF</b> [Default]</li> </ul>
<i>day-OfWeekAlarm</i>	is the alarm condition for the day of week. Valid values are <ul style="list-style-type: none"> <li>■ An integer between 0-6, OR</li> <li>■ <b>RTC_C_ALARMCONDITION_OFF</b> [Default]</li> </ul>
<i>dayOfmonthAlarm</i>	is the alarm condition for the day of the month. Valid values are <ul style="list-style-type: none"> <li>■ An integer between 0-31, OR</li> <li>■ <b>RTC_C_ALARMCONDITION_OFF</b> [Default]</li> </ul>

This function sets a Calendar interrupt condition to assert the RTCAIFG interrupt flag. The condition is a logical and of all of the parameters. For example if the minutes and hours alarm is set, then the interrupt will only assert when the minutes AND the hours change to the specified setting. Use the `RTC_ALARM_OFF` for any alarm settings that should not be apart of the alarm condition.

**Returns**

None

### 19.3.2.15 void RTC\_C\_setCalendarEvent ( uint\_fast16\_t *eventSelect* )

Sets a single specified Calendar interrupt condition.



**Parameters**

<i>eventSelect</i>	is the condition selected. Valid values are <ul style="list-style-type: none"> <li>■ <b>RTC_C_CALENDAREVENT_MINUTECHANGE</b> - assert interrupt on every minute</li> <li>■ <b>RTC_C_CALENDAREVENT_HOURLCHANGE</b> - assert interrupt on every hour</li> <li>■ <b>RTC_C_CALENDAREVENT_NOON</b> - assert interrupt when hour is 12</li> <li>■ <b>RTC_C_CALENDAREVENT_MIDNIGHT</b> - assert interrupt when hour is 0</li> </ul>
--------------------	--

This function sets a specified event to assert the RTCTEVIFG interrupt. This interrupt is independent from the Calendar alarm interrupt.

**Returns**

None

### 19.3.2.16 void RTC\_C\_setCalibrationData ( uint\_fast8\_t *offsetDirection*, uint\_fast8\_t *offsetValue* )

Sets the specified calibration for the RTC.

**Parameters**

<i>offsetDirection</i>	is the direction that the calibration offset will go. Valid values are <ul style="list-style-type: none"> <li>■ <b>RTC_C_CALIBRATION_DOWN1PPM</b> - calibrate at steps of -1</li> <li>■ <b>RTC_C_CALIBRATION_UP1PPM</b> - calibrat at steps of +1</li> </ul>
<i>offsetValue</i>	is the value that the offset will be a factor of; a valid value is any integer from 1-240.

This function sets the calibration offset to make the RTC as accurate as possible. The *offsetDirection* can be either +1-ppm or -1-ppm, and the *offsetValue* should be from 1-240 and is multiplied by the direction setting (i.e. +1-ppm \* 8 (*offsetValue*) = +8-ppm).

**Returns**

None

### 19.3.2.17 void RTC\_C\_setCalibrationFrequency ( uint\_fast16\_t *frequencySelect* )

Allows and Sets the frequency output to RTCLK pin for calibration measurement.

**Parameters**

<i>frequencySelect</i>	is the frequency output to RTCLK. Valid values are <ul style="list-style-type: none"> <li>■ <b>RTC_C_CALIBRATIONFREQ_OFF</b> - turn off calibration output [Default]</li> <li>■ <b>RTC_C_CALIBRATIONFREQ_512HZ</b> - output signal at 512Hz for calibration</li> <li>■ <b>RTC_C_CALIBRATIONFREQ_256HZ</b> - output signal at 256Hz for calibration</li> <li>■ <b>RTC_C_CALIBRATIONFREQ_1HZ</b> - output signal at 1Hz for calibration</li> </ul>
------------------------	--

This function sets a frequency to measure at the RTCLK output pin. After testing the set frequency, the calibration could be set accordingly.

**Returns**

None

19.3.2.18 void RTC\_C\_setPrescaleValue ( uint\_fast8\_t *prescaleSelect*, uint\_fast8\_t *prescaleCounterValue* )

Sets the selected Prescaler value.

**Parameters**

<i>prescaleSelect</i>	is the prescaler to set the value for. Valid values are <ul style="list-style-type: none"> <li>■ RTC_C_PRESCALE_0</li> <li>■ RTC_C_PRESCALE_1</li> </ul>
<i>prescaleCounterValue</i>	is the specified value to set the prescaler to; a valid value is any integer from 0-255.

This function sets the prescale counter value. Before setting the prescale counter, it should be held.

**Returns**

None

19.3.2.19 bool RTC\_C\_setTemperatureCompensation ( uint\_fast16\_t *offsetDirection*, uint\_fast8\_t *offsetValue* )

Sets the specified temperature compensation for the RTC.

**Parameters**

<i>offsetDirection</i>	is the direction that the calibration offset will go. Valid values are <ul style="list-style-type: none"> <li>■ RTC_C_COMPENSATION_DOWN1PPM - calibrate at steps of -1</li> <li>■ RTC_C_COMPENSATION_UP1PPM - calibrate at steps of +1</li> </ul>
<i>offsetValue</i>	is the value that the offset will be a factor of; a value is any integer from 1-240.

This function sets the calibration offset to make the RTC as accurate as possible. The *offsetDirection* can be either +1-ppm or -1-ppm, and the *offsetValue* should be from 1-240 and is multiplied by the direction setting (i.e. +1-ppm \* 8 (*offsetValue*) = +8-ppm).

**Returns**

true if calibration was set, false if it could not be set

19.3.2.20 void RTC\_C\_startClock ( void )

Starts the RTC.

This function clears the RTC main hold bit to allow the RTC to function.

**Returns**

None

19.3.2.21 void RTC\_C\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the RTC interrupt

This function unregisters the handler to be called when RTC interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 20 Serial Peripheral Interface (SPI)

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### 20.1 Module Operation

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Note for simplicity, the module name EUSCI\_A and EUSCI\_B have been omitted from the API names.

This library provides the API for handling a 3-wire SPI communication

The SPI module can be configured as either a master or a slave device.

The SPI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the SSI module's input clock.

### 20.2 Basic Operation Modes

To use the module as a master, the user must call `SPI_masterInit()` to configure the SPI Master. This is followed by enabling the SPI module using `SPI_enable()`. The interrupts are then enabled (if needed). It is recommended to enable the SPI module before enabling the interrupts. A data transmit is then initiated using `SPI_transmitData` and then when the receive flag is set, the received data is read using `SPI_receiveData` and this indicates that an RX/TX operation is complete.

To use the module as a slave, initialization is done using `SPI_initSlave` and this is followed by enabling the module using `SPI_enableModule`. Following this, the interrupts may be enabled as needed. When the receive flag is set, data is first transmitted using `SPI_transmitData` and this is followed by a data reception by `SPI_receiveData`.

## 20.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the SPI module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the SPI module in 3wire master mode.

In the code snippet below, the configuration settings for SPI in 3wire master mode can be seen:

```

/* SPI Master Configuration Parameter */
const eUSCI_SPI_MasterConfig spiMasterConfig =
{
    EUSCI_B_SPI_CLOCKSOURCE_SMCLK,           // SMCLK Clock Source
    3000000,                                  // SMCLK = DCO = 3MHZ
    500000,                                    // SPICLK = 500khz
    EUSCI_B_SPI_MSB_FIRST,                   // MSB First
    EUSCI_B_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT, // Phase
    EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_HIGH, // High polarity
    EUSCI_B_SPI_3PIN                          // 3Wire SPI Mode
};

```

In this code snippet, the SPI module is configured and enabled for 3wire SPI operation using the DriverLib APIs:

```

/* Selecting P1.5 P1.6 and P1.7 in SPI mode */
GPIO_setAsPeripheralModuleFunctionInputPin(GPIO_PORT_P1,
    GPIO_PIN5 | GPIO_PIN6 | GPIO_PIN7,  GPIO_PRIMARY_MODULE_FUNCTION);

/* Configuring SPI in 3wire master mode */
SPI_initMaster(EUSCI_B0_BASE, &spiMasterConfig);

/* Enable SPI module */
SPI_enableModule(EUSCI_B0_BASE);

/* Enabling interrupts */
SPI_enableInterrupt(EUSCI_B0_BASE,  EUSCI_B_SPI_RECEIVE_INTERRUPT);
Interrupt_enableInterrupt(INT_EUSCIB0);
Interrupt_enableSleepOnIsrExit();

```

## 20.4 Definitions

### Data Structures

- struct [\\_eUSCI\\_SPI\\_MasterConfig](#)
- struct [\\_eUSCI\\_SPI\\_SlaveConfig](#)

### Functions

- void [EUSCI\\_A\\_SPI\\_changeClockPhasePolarity](#) (uint32\_t baseAddress, uint16\_t clockPhase, uint16\_t clockPolarity)
- void [EUSCI\\_A\\_SPI\\_clearInterruptFlag](#) (uint32\_t baseAddress, uint8\_t mask)
- void [EUSCI\\_A\\_SPI\\_disable](#) (uint32\_t baseAddress)
- void [EUSCI\\_A\\_SPI\\_disableInterrupt](#) (uint32\_t baseAddress, uint8\_t mask)
- void [EUSCI\\_A\\_SPI\\_enable](#) (uint32\_t baseAddress)
- void [EUSCI\\_A\\_SPI\\_enableInterrupt](#) (uint32\_t baseAddress, uint8\_t mask)
- uint8\_t [EUSCI\\_A\\_SPI\\_getInterruptStatus](#) (uint32\_t baseAddress, uint8\_t mask)
- uint32\_t [EUSCI\\_A\\_SPI\\_getReceiveBufferAddressForDMA](#) (uint32\_t baseAddress)
- uint32\_t [EUSCI\\_A\\_SPI\\_getTransmitBufferAddressForDMA](#) (uint32\_t baseAddress)
- bool [EUSCI\\_A\\_SPI\\_isBusy](#) (uint32\_t baseAddress)
- void [EUSCI\\_A\\_SPI\\_masterChangeClock](#) (uint32\_t baseAddress, uint32\_t clockSourceFrequency, uint32\_t desiredSpiClock)
- uint8\_t [EUSCI\\_A\\_SPI\\_receiveData](#) (uint32\_t baseAddress)
- void [EUSCI\\_A\\_SPI\\_select4PinFunctionality](#) (uint32\_t baseAddress, uint8\_t select4PinFunctionality)
- bool [EUSCI\\_A\\_SPI\\_slaveInit](#) (uint32\_t baseAddress, uint16\_t msbFirst, uint16\_t clockPhase, uint16\_t clockPolarity, uint16\_t spiMode)
- void [EUSCI\\_A\\_SPI\\_transmitData](#) (uint32\_t baseAddress, uint8\_t transmitData)
- void [EUSCI\\_B\\_SPI\\_changeClockPhasePolarity](#) (uint32\_t baseAddress, uint16\_t clockPhase, uint16\_t clockPolarity)
- void [EUSCI\\_B\\_SPI\\_clearInterruptFlag](#) (uint32\_t baseAddress, uint8\_t mask)
- void [EUSCI\\_B\\_SPI\\_disable](#) (uint32\_t baseAddress)
- void [EUSCI\\_B\\_SPI\\_disableInterrupt](#) (uint32\_t baseAddress, uint8\_t mask)
- void [EUSCI\\_B\\_SPI\\_enable](#) (uint32\_t baseAddress)
- void [EUSCI\\_B\\_SPI\\_enableInterrupt](#) (uint32\_t baseAddress, uint8\_t mask)
- uint8\_t [EUSCI\\_B\\_SPI\\_getInterruptStatus](#) (uint32\_t baseAddress, uint8\_t mask)
- uint32\_t [EUSCI\\_B\\_SPI\\_getReceiveBufferAddressForDMA](#) (uint32\_t baseAddress)
- uint32\_t [EUSCI\\_B\\_SPI\\_getTransmitBufferAddressForDMA](#) (uint32\_t baseAddress)
- bool [EUSCI\\_B\\_SPI\\_isBusy](#) (uint32\_t baseAddress)
- void [EUSCI\\_B\\_SPI\\_masterChangeClock](#) (uint32\_t baseAddress, uint32\_t clockSourceFrequency, uint32\_t desiredSpiClock)
- uint8\_t [EUSCI\\_B\\_SPI\\_receiveData](#) (uint32\_t baseAddress)
- void [EUSCI\\_B\\_SPI\\_select4PinFunctionality](#) (uint32\_t baseAddress, uint8\_t select4PinFunctionality)
- bool [EUSCI\\_B\\_SPI\\_slaveInit](#) (uint32\_t baseAddress, uint16\_t msbFirst, uint16\_t clockPhase, uint16\_t clockPolarity, uint16\_t spiMode)
- void [EUSCI\\_B\\_SPI\\_transmitData](#) (uint32\_t baseAddress, uint8\_t transmitData)
- void [SPI\\_changeClockPhasePolarity](#) (uint32\_t moduleInstance, uint\_fast16\_t clockPhase, uint\_fast16\_t clockPolarity)
- void [SPI\\_changeMasterClock](#) (uint32\_t moduleInstance, uint32\_t clockSourceFrequency, uint32\_t desiredSpiClock)
- void [SPI\\_clearInterruptFlag](#) (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void [SPI\\_disableInterrupt](#) (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void [SPI\\_disableModule](#) (uint32\_t moduleInstance)

- void [SPI\\_enableInterrupt](#) (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void [SPI\\_enableModule](#) (uint32\_t moduleInstance)
- uint\_fast8\_t [SPI\\_getEnabledInterruptStatus](#) (uint32\_t moduleInstance)
- uint\_fast8\_t [SPI\\_getInterruptStatus](#) (uint32\_t moduleInstance, uint16\_t mask)
- uint32\_t [SPI\\_getReceiveBufferAddressForDMA](#) (uint32\_t moduleInstance)
- uint32\_t [SPI\\_getTransmitBufferAddressForDMA](#) (uint32\_t moduleInstance)
- bool [SPI\\_initMaster](#) (uint32\_t moduleInstance, const [eUSCI\\_SPI\\_MasterConfig](#) \*config)
- bool [SPI\\_initSlave](#) (uint32\_t moduleInstance, const [eUSCI\\_SPI\\_SlaveConfig](#) \*config)
- uint\_fast8\_t [SPI\\_isBusy](#) (uint32\_t moduleInstance)
- uint8\_t [SPI\\_receiveData](#) (uint32\_t moduleInstance)
- void [SPI\\_registerInterrupt](#) (uint32\_t moduleInstance, void(\*intHandler)(void))
- void [SPI\\_selectFourPinFunctionality](#) (uint32\_t moduleInstance, uint\_fast8\_t select4PinFunctionality)
- void [SPI\\_transmitData](#) (uint32\_t moduleInstance, uint\_fast8\_t transmitData)
- void [SPI\\_unregisterInterrupt](#) (uint32\_t moduleInstance)

## 20.4.1 Detailed Description

The code for this module is contained in `driverlib/spi.c`, with `driverlib/spi.h` containing the API declarations for use by applications.

## 20.4.2 Function Documentation

20.4.2.1 void EUSCI\_A\_SPI\_changeClockPhasePolarity ( uint32\_t *baseAddress*, uint16\_t *clockPhase*, uint16\_t *clockPolarity* )

Changes the SPI colock phase and polarity. At the end of this function call, SPI module is left enabled.

### Parameters

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>clockPhase</i>	is clock phase select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default]</li> <li>■ EUSCI_A_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_A_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default]</li> </ul>

Modified bits are **EUSCI\_A\_CTLW0\_CKPL**, **EUSCI\_A\_CTLW0\_CKPH** and **UCSWRST** of **UCAxCTLW0** register.

### Returns

None

Referenced by [SPI\\_changeClockPhasePolarity\(\)](#).

20.4.2.2 void EUSCI\_A\_SPI\_clearInterruptFlag ( uint32\_t *baseAddress*, uint8\_t *mask* )

Clears the selected SPI interrupt status flag.

### Parameters

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>mask</i>	is the masked interrupt flag to be cleared. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_TRANSMIT_INTERRUPT</li> <li>■ EUSCI_A_SPI_RECEIVE_INTERRUPT</li> </ul>

Modified bits of **UCAxIFG** register.



**Returns**

None

Referenced by [SPI\\_clearInterruptFlag\(\)](#).20.4.2.3 void EUSCI\_A\_SPI\_disable ( uint32\_t *baseAddress* )

Disables the SPI block.

This will disable operation of the SPI block.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

Modified bits are **UCSWRST** of **UCAxCTLW0** register.**Returns**

None

Referenced by [SPI\\_disableModule\(\)](#).20.4.2.4 void EUSCI\_A\_SPI\_disableInterrupt ( uint32\_t *baseAddress*, uint8\_t *mask* )

Disables individual SPI interrupt sources.

Disables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>mask</i>	is the bit mask of the interrupt sources to be disabled. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_TRANSMIT_INTERRUPT</li> <li>■ EUSCI_A_SPI_RECEIVE_INTERRUPT</li> </ul>

Modified bits of **UCAxIE** register.**Returns**

None

Referenced by [SPI\\_disableInterrupt\(\)](#).20.4.2.5 void EUSCI\_A\_SPI\_enable ( uint32\_t *baseAddress* )

Enables the SPI block.

This will enable operation of the SPI block.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

Modified bits are **UCSWRST** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_enableModule\(\)](#).

#### 20.4.2.6 void EUSCI\_A\_SPI\_enableInterrupt ( uint32\_t *baseAddress*, uint8\_t *mask* )

Enables individual SPI interrupt sources.

Enables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. Does not clear interrupt flags.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>mask</i>	is the bit mask of the interrupt sources to be enabled. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A_SPI_TRANSMIT_INTERRUPT</b></li> <li>■ <b>EUSCI_A_SPI_RECEIVE_INTERRUPT</b></li> </ul>

Modified bits of **UCAxIFG** register and bits of **UCAxIE** register.

**Returns**

None

Referenced by [SPI\\_enableInterrupt\(\)](#).

#### 20.4.2.7 uint8\_t EUSCI\_A\_SPI\_getInterruptStatus ( uint32\_t *baseAddress*, uint8\_t *mask* )

Gets the current SPI interrupt status.

This returns the interrupt status for the SPI module based on which flag is passed.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>mask</i>	is the masked interrupt flag status to be returned. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A_SPI_TRANSMIT_INTERRUPT</b></li> <li>■ <b>EUSCI_A_SPI_RECEIVE_INTERRUPT</b></li> </ul>

**Returns**

Logical OR of any of the following:

- **EUSCI\_A\_SPI\_TRANSMIT\_INTERRUPT**
  - **EUSCI\_A\_SPI\_RECEIVE\_INTERRUPT**
- indicating the status of the masked interrupts

Referenced by [SPI\\_getInterruptStatus\(\)](#).

#### 20.4.2.8 uint32\_t EUSCI\_A\_SPI\_getReceiveBufferAddressForDMA ( uint32\_t *baseAddress* )

Returns the address of the RX Buffer of the SPI for the DMA module.

Returns the address of the SPI RX Buffer. This can be used in conjunction with the DMA to store the received data directly to memory.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

**Returns**

the address of the RX Buffer

Referenced by [SPI\\_getReceiveBufferAddressForDMA\(\)](#).

#### 20.4.2.9 uint32\_t EUSCI\_A\_SPI\_getTransmitBufferAddressForDMA ( uint32\_t *baseAddress* )

Returns the address of the TX Buffer of the SPI for the DMA module.

Returns the address of the SPI TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

**Returns**

the address of the TX Buffer

Referenced by [SPI\\_getTransmitBufferAddressForDMA\(\)](#).

#### 20.4.2.10 bool EUSCI\_A\_SPI\_isBusy ( uint32\_t *baseAddress* )

Indicates whether or not the SPI bus is busy.

This function returns an indication of whether or not the SPI bus is busy. This function checks the status of the bus via UCBBUSY bit

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

**Returns**

true if busy, false otherwise

Referenced by [SPI\\_isBusy\(\)](#).

#### 20.4.2.11 void EUSCI\_A\_SPI\_masterChangeClock ( uint32\_t *baseAddress*, uint32\_t *clockSourceFrequency*, uint32\_t *desiredSpiClock* )

Initializes the SPI Master clock. At the end of this function call, SPI module is left enabled.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>clockSourceFrequency</i>	is the frequency of the selected clock source
<i>desiredSpiClock</i>	is the desired clock rate for SPI communication

Modified bits are **UCSWRST** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_changeMasterClock\(\)](#).

#### 20.4.2.12 uint8\_t EUSCI\_A\_SPI\_receiveData ( uint32\_t *baseAddress* )

Receives a byte that has been sent to the SPI Module.

This function reads a byte of data from the SPI receive data Register.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
--------------------	--

**Returns**

Returns the byte received from by the SPI module, cast as an uint8\_t.

Referenced by [SPI\\_receiveData\(\)](#).

#### 20.4.2.13 void EUSCI\_A\_SPI\_select4PinFunctionality ( uint32\_t *baseAddress*, uint8\_t *select4PinFunctionality* )

Selects 4Pin Functionality.

This function should be invoked only in 4-wire mode. Invoking this function has no effect in 3-wire mode.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>select4PinFunctionality</i>	selects 4 pin functionality Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_PREVENT_CONFLICTS_WITH_OTHER_MASTERS</li> <li>■ EUSCI_A_SPI_ENABLE_SIGNAL_FOR_4WIRE_SLAVE</li> </ul>

Modified bits are **UCSTEM** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_selectFourPinFunctionality\(\)](#).

20.4.2.14 `bool EUSCI_A_SPI_slaveInit ( uint32_t baseAddress, uint16_t msbFirst, uint16_t clockPhase, uint16_t clockPolarity, uint16_t spiMode )`

Initializes the SPI Slave block.

Upon successful initialization of the SPI slave block, this function will have initialized the slave block, but the SPI Slave block still remains disabled and must be enabled with [EUSCI\\_A\\_SPI\\_enable\(\)](#)

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI Slave module.
<i>msbFirst</i>	controls the direction of the receive and transmit shift register. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_MSB_FIRST</li> <li>■ EUSCI_A_SPI_LSB_FIRST [Default]</li> </ul>
<i>clockPhase</i>	is clock phase select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default]</li> <li>■ EUSCI_A_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_A_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default]</li> </ul>
<i>spiMode</i>	is SPI mode select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_A_SPI_3PIN</li> <li>■ EUSCI_A_SPI_4PIN_UCxSTE_ACTIVE_HIGH</li> <li>■ EUSCI_A_SPI_4PIN_UCxSTE_ACTIVE_LOW</li> </ul>

Modified bits are **EUSCI\_A\_CTLW0\_MSB**, **EUSCI\_A\_CTLW0\_MST**, **EUSCI\_A\_CTLW0\_SEVENBIT**, **EUSCI\_A\_CTLW0\_CKPL**, **EUSCI\_A\_CTLW0\_CKPH**, **UCMODE** and **UCSWRST** of **UCAxCTLW0** register.

**Returns**

STATUS\_SUCCESS

20.4.2.15 void EUSCI\_A\_SPI\_transmitData ( uint32\_t *baseAddress*, uint8\_t *transmitData* )

Transmits a byte from the SPI Module.

This function will place the supplied data into SPI transmit data register to start transmission.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_A_SPI module.
<i>transmitData</i>	data to be transmitted from the SPI module

**Returns**

None

Referenced by [SPI\\_transmitData\(\)](#).

20.4.2.16 void EUSCI\_B\_SPI\_changeClockPhasePolarity ( uint32\_t *baseAddress*, uint16\_t *clockPhase*, uint16\_t *clockPolarity* )

Changes the SPI clock phase and polarity. At the end of this function call, SPI module is left enabled.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>clockPhase</i>	is clock phase select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default]</li> <li>■ EUSCI_B_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default]</li> </ul>

Modified bits are **EUSCI\_A\_CTLW0\_CKPL**, **EUSCI\_A\_CTLW0\_CKPH** and **UCSWRST** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_changeClockPhasePolarity\(\)](#).

20.4.2.17 void EUSCI\_B\_SPI\_clearInterruptFlag ( uint32\_t *baseAddress*, uint8\_t *mask* )

Clears the selected SPI interrupt status flag.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>mask</i>	is the masked interrupt flag to be cleared. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_TRANSMIT_INTERRUPT</li> <li>■ EUSCI_B_SPI_RECEIVE_INTERRUPT</li> </ul>

Modified bits of **UCAxIFG** register.

**Returns**

None

Referenced by [SPI\\_clearInterruptFlag\(\)](#).

#### 20.4.2.18 void EUSCI\_B\_SPI\_disable ( uint32\_t *baseAddress* )

Disables the SPI block.

This will disable operation of the SPI block.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

Modified bits are **UCSWRST** of **UCBxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_disableModule\(\)](#).

#### 20.4.2.19 void EUSCI\_B\_SPI\_disableInterrupt ( uint32\_t *baseAddress*, uint8\_t *mask* )

Disables individual SPI interrupt sources.

Disables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>mask</i>	is the bit mask of the interrupt sources to be disabled. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_TRANSMIT_INTERRUPT</li> <li>■ EUSCI_B_SPI_RECEIVE_INTERRUPT</li> </ul>

Modified bits of **UCAxIE** register.

**Returns**

None

Referenced by [SPI\\_disableInterrupt\(\)](#).

20.4.2.20 void EUSCI\_B\_SPI\_enable ( uint32\_t *baseAddress* )

Enables the SPI block.

This will enable operation of the SPI block.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

Modified bits are **UCSWRST** of **UCBxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_enableModule\(\)](#).

20.4.2.21 void EUSCI\_B\_SPI\_enableInterrupt ( uint32\_t *baseAddress*, uint8\_t *mask* )

Enables individual SPI interrupt sources.

Enables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor. Does not clear interrupt flags.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>mask</i>	is the bit mask of the interrupt sources to be enabled. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ <b>EUSCI_B_SPI_TRANSMIT_INTERRUPT</b></li> <li>■ <b>EUSCI_B_SPI_RECEIVE_INTERRUPT</b></li> </ul>

Modified bits of **UCAxIFG** register and bits of **UCAxIE** register.

**Returns**

None

Referenced by [SPI\\_enableInterrupt\(\)](#).

20.4.2.22 uint8\_t EUSCI\_B\_SPI\_getInterruptStatus ( uint32\_t *baseAddress*, uint8\_t *mask* )

Gets the current SPI interrupt status.

This returns the interrupt status for the SPI module based on which flag is passed.



**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>mask</i>	is the masked interrupt flag status to be returned. Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_TRANSMIT_INTERRUPT</li> <li>■ EUSCI_B_SPI_RECEIVE_INTERRUPT</li> </ul>

**Returns**

Logical OR of any of the following:

- EUSCI\_B\_SPI\_TRANSMIT\_INTERRUPT
  - EUSCI\_B\_SPI\_RECEIVE\_INTERRUPT
- indicating the status of the masked interrupts

Referenced by [SPI\\_getInterruptStatus\(\)](#).

#### 20.4.2.23 uint32\_t EUSCI\_B\_SPI\_getReceiveBufferAddressForDMA ( uint32\_t *baseAddress* )

Returns the address of the RX Buffer of the SPI for the DMA module.

Returns the address of the SPI RX Buffer. This can be used in conjunction with the DMA to store the received data directly to memory.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

**Returns**

the address of the RX Buffer

Referenced by [SPI\\_getReceiveBufferAddressForDMA\(\)](#).

#### 20.4.2.24 uint32\_t EUSCI\_B\_SPI\_getTransmitBufferAddressForDMA ( uint32\_t *baseAddress* )

Returns the address of the TX Buffer of the SPI for the DMA module.

Returns the address of the SPI TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

**Returns**

the address of the TX Buffer

Referenced by [SPI\\_getTransmitBufferAddressForDMA\(\)](#).

20.4.2.25 bool EUSCI\_B\_SPI\_isBusy ( uint32\_t *baseAddress* )

Indicates whether or not the SPI bus is busy.

This function returns an indication of whether or not the SPI bus is busy. This function checks the status of the bus via UCBBUSY bit

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

**Returns**

true if busy, false otherwise

Referenced by [SPI\\_isBusy\(\)](#).

20.4.2.26 void EUSCI\_B\_SPI\_masterChangeClock ( uint32\_t *baseAddress*, uint32\_t *clockSourceFrequency*, uint32\_t *desiredSpiClock* )

Initializes the SPI Master clock. At the end of this function call, SPI module is left enabled.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>clockSourceFrequency</i>	is the frequency of the selected clock source
<i>desiredSpiClock</i>	is the desired clock rate for SPI communication

Modified bits are **UCSWRST** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_changeMasterClock\(\)](#).

20.4.2.27 uint8\_t EUSCI\_B\_SPI\_receiveData ( uint32\_t *baseAddress* )

Receives a byte that has been sent to the SPI Module.

This function reads a byte of data from the SPI receive data Register.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
--------------------	--

**Returns**

Returns the byte received from by the SPI module, cast as an `uint8_t`.

Referenced by [SPI\\_receiveData\(\)](#).

20.4.2.28 `void EUSCI_B_SPI_select4PinFunctionality ( uint32_t baseAddress, uint8_t select4PinFunctionality )`

Selects 4Pin Functionality.

This function should be invoked only in 4-wire mode. Invoking this function has no effect in 3-wire mode.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>select4PinFunctionality</i>	selects 4 pin functionality Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_PREVENT_CONFLICTS_WITH_OTHER_MASTERS</li> <li>■ EUSCI_B_SPI_ENABLE_SIGNAL_FOR_4WIRE_SLAVE</li> </ul>

Modified bits are **UCSTEM** of **UCAxCTLW0** register.

**Returns**

None

Referenced by [SPI\\_selectFourPinFunctionality\(\)](#).

20.4.2.29 `bool EUSCI_B_SPI_slaveInit ( uint32_t baseAddress, uint16_t msbFirst, uint16_t clockPhase, uint16_t clockPolarity, uint16_t spiMode )`

Initializes the SPI Slave block.

Upon successful initialization of the SPI slave block, this function will have initialized the slave block, but the SPI Slave block still remains disabled and must be enabled with [EUSCI\\_B\\_SPI\\_enable\(\)](#)

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI Slave module.
<i>msbFirst</i>	controls the direction of the receive and transmit shift register. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_MSB_FIRST</li> <li>■ EUSCI_B_SPI_LSB_FIRST [Default]</li> </ul>

<i>clockPhase</i>	is clock phase select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default]</li> <li>■ EUSCI_B_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_B_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default]</li> </ul>
<i>spiMode</i>	is SPI mode select Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_B_SPI_3PIN</li> <li>■ EUSCI_B_SPI_4PIN_UCxSTE_ACTIVE_HIGH</li> <li>■ EUSCI_B_SPI_4PIN_UCxSTE_ACTIVE_LOW</li> </ul>

Modified bits are **EUSCI\_A\_CTLW0\_MSB**, **EUSCI\_A\_CTLW0\_MST**, **EUSCI\_A\_CTLW0\_SEVENBIT**, **EUSCI\_A\_CTLW0\_CKPL**, **EUSCI\_A\_CTLW0\_CKPH**, **UCMODE** and **UCSWRST** of **UCAxCTLW0** register.

**Returns**

STATUS\_SUCCESS

20.4.2.30 void EUSCI\_B\_SPI\_transmitData ( uint32\_t *baseAddress*, uint8\_t *transmitData* )

Transmits a byte from the SPI Module.

This function will place the supplied data into SPI trasmit data register to start transmission.

**Parameters**

<i>baseAddress</i>	is the base address of the EUSCI_B_SPI module.
<i>transmitData</i>	data to be transmitted from the SPI module

**Returns**

None

Referenced by [SPI\\_transmitData\(\)](#).

20.4.2.31 void SPI\_changeClockPhasePolarity ( uint32\_t *moduleInstance*, uint\_fast16\_t *clockPhase*, uint\_fast16\_t *clockPolarity* )

Changes the SPI clock phase and polarity. At the end of this function call, SPI module is left enabled.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
<i>clockPhase</i>	is clock phase select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default Value]</li> <li>■ EUSCI_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select. Valid values are: <ul style="list-style-type: none"> <li>■ EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default Value]</li> </ul>

Modified bits are **UCSWRST**, **UCCKPH**, **UCCKPL**, **UCSWRST** bits of **UCAxCTLW0**

**Returns**

None

References [EUSCI\\_A\\_SPI\\_changeClockPhasePolarity\(\)](#), and [EUSCI\\_B\\_SPI\\_changeClockPhasePolarity\(\)](#).

20.4.2.32 void SPI\_changeMasterClock ( uint32\_t *moduleInstance*, uint32\_t *clockSourceFrequency*, uint32\_t *desiredSpiClock* )

Initializes the SPI Master clock. At the end of this function call, SPI module is left enabled.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
<i>clockSourceFrequency</i>	is the frequency of the selected clock source
<i>desiredSpiClock</i>	is the desired clock rate for SPI communication.

Modified bits are **UCSWRST** bit of **UCAxCTLW0** register and **UCAxBRW** register

**Returns**

None

References [EUSCI\\_A\\_SPI\\_masterChangeClock\(\)](#), and [EUSCI\\_B\\_SPI\\_masterChangeClock\(\)](#).

#### 20.4.2.33 void SPI\_clearInterruptFlag ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Clears the selected SPI interrupt status flag.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
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<i>mask</i>	is the masked interrupt flag to be cleared.
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The mask parameter is the logical OR of any of the following:

- **EUSCI\_SPI\_RECEIVE\_INTERRUPT** -Receive interrupt
- **EUSCI\_SPI\_TRANSMIT\_INTERRUPT** - Transmit interrupt Modified registers are **UCAxIFG**.

#### Returns

None

References [EUSCI\\_A\\_SPI\\_clearInterruptFlag\(\)](#), and [EUSCI\\_B\\_SPI\\_clearInterruptFlag\(\)](#).

#### 20.4.2.34 void SPI\_disableInterrupt ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Disables individual SPI interrupt sources.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
<i>mask</i>	is the bit mask of the interrupt sources to be disabled.

Disables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_SPI\_RECEIVE\_INTERRUPT** Receive interrupt
- **EUSCI\_SPI\_TRANSMIT\_INTERRUPT** Transmit interrupt

Modified register is **UCAxIE**

#### Returns

None.

References [EUSCI\\_A\\_SPI\\_disableInterrupt\(\)](#), and [EUSCI\\_B\\_SPI\\_disableInterrupt\(\)](#).

#### 20.4.2.35 void SPI\_disableModule ( uint32\_t *moduleInstance* )

Disables the SPI block.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
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This will disable operation of the SPI block.

Modified bits are **UCSWRST** bit of **UCAxCTLW0** register.

**Returns**

None.

References [EUSCI\\_A\\_SPI\\_disable\(\)](#), and [EUSCI\\_B\\_SPI\\_disable\(\)](#).

#### 20.4.2.36 void SPI\_enableInterrupt ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Enables individual SPI interrupt sources.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
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<i>mask</i>	is the bit mask of the interrupt sources to be enabled.
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Enables the indicated SPI interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_SPI\_RECEIVE\_INTERRUPT** Receive interrupt
- **EUSCI\_SPI\_TRANSMIT\_INTERRUPT** Transmit interrupt

Modified registers are **UCAxIFG** and **UCAxIE**

#### Returns

None.

References [EUSCI\\_A\\_SPI\\_enableInterrupt\(\)](#), and [EUSCI\\_B\\_SPI\\_enableInterrupt\(\)](#).

### 20.4.2.37 void SPI\_enableModule ( uint32\_t *moduleInstance* )

Enables the SPI block.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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This will enable operation of the SPI block. Modified bits are **UCSWRST** bit of **UCAxCTLW0** register.

#### Returns

None.

References [EUSCI\\_A\\_SPI\\_enable\(\)](#), and [EUSCI\\_B\\_SPI\\_enable\(\)](#).

### 20.4.2.38 uint\_fast8\_t SPI\_getEnabledInterruptStatus ( uint32\_t *moduleInstance* )

Gets the current SPI interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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Modified registers are **UCAxIFG**.

## Returns

The current interrupt status as the mask of the set flags Mask parameter can be either any of the following selection:

- **EUSCI\_SPI\_RECEIVE\_INTERRUPT** -Receive interrupt
- **EUSCI\_SPI\_TRANSMIT\_INTERRUPT** - Transmit interrupt

References [SPI\\_getInterruptStatus\(\)](#).

#### 20.4.2.39 uint\_fast8\_t SPI\_getInterruptStatus ( uint32\_t moduleInstance, uint16\_t mask )

Gets the current SPI interrupt status.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
<i>mask</i>	Mask of interrupt to filter. This can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_RECEIVE_INTERRUPT</b> -Receive interrupt</li> <li>■ <b>EUSCI_SPI_TRANSMIT_INTERRUPT</b> - Transmit interrupt</li> </ul>

Modified registers are **UCAxIFG**.

**Returns**

The current interrupt status as the mask of the set flags Mask parameter can be either any of the following selection:

- **EUSCI\_SPI\_RECEIVE\_INTERRUPT** -Receive interrupt
- **EUSCI\_SPI\_TRANSMIT\_INTERRUPT** - Transmit interrupt

References [EUSCI\\_A\\_SPI\\_getInterruptStatus\(\)](#), and [EUSCI\\_B\\_SPI\\_getInterruptStatus\(\)](#).

Referenced by [SPI\\_getEnabledInterruptStatus\(\)](#).

#### 20.4.2.40 uint32\_t SPI\_getReceiveBufferAddressForDMA ( uint32\_t *moduleInstance* )

Returns the address of the RX Buffer of the SPI for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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Returns the address of the SPI RX Buffer. This can be used in conjunction with the DMA to store the received data directly to memory.

**Returns**

NONE

References [EUSCI\\_A\\_SPI\\_getReceiveBufferAddressForDMA\(\)](#), and [EUSCI\\_B\\_SPI\\_getReceiveBufferAddressForDMA\(\)](#).

#### 20.4.2.41 uint32\_t SPI\_getTransmitBufferAddressForDMA ( uint32\_t *moduleInstance* )

Returns the address of the TX Buffer of the SPI for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
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Returns the address of the SPI TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Returns**

NONE

References [EUSCI\\_A\\_SPI\\_getTransmitBufferAddressForDMA\(\)](#), and [EUSCI\\_B\\_SPI\\_getTransmitBufferAddressForDMA\(\)](#).

#### 20.4.2.42 bool SPI\_initMaster ( uint32\_t *moduleInstance*, const **eUSCI\_SPI\_MasterConfig** \* *config* )

Initializes the SPI Master block.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
<i>config</i>	Configuration structure for SPI master mode

## Configuration options for eUSCI\_SPI\_MasterConfig structure.

## Parameters

<i>selectClockSource</i>	selects clock source. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_SPI_CLOCKSOURCE_ACLK</li> <li>■ EUSCI_SPI_CLOCKSOURCE_SMCLK</li> </ul>
<i>clockSourceFrequency</i>	is the frequency of the selected clock source
<i>desiredSpiClock</i>	is the desired clock rate for SPI communication
<i>msbFirst</i>	controls the direction of the receive and transmit shift register. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_SPI_MSB_FIRST</li> <li>■ EUSCI_SPI_LSB_FIRST [Default Value]</li> </ul>
<i>clockPhase</i>	is clock phase select. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT [Default Value]</li> <li>■ EUSCI_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</li> </ul>
<i>clockPolarity</i>	is clock polarity select. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</li> <li>■ EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_LOW [Default Value]</li> </ul>

<i>spiMode</i>	<p>is SPI mode select. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_3PIN</b> [Default Value]</li> <li>■ <b>EUSCI_SPI_4PIN_UCxSTE_ACTIVE_HIGH</b></li> <li>■ <b>EUSCI_SPI_4PIN_UCxSTE_ACTIVE_LOW</b> Upon successful initialization of the SPI master block, this function will have set the bus speed for the master, but the SPI Master block still remains disabled and must be enabled with <a href="#">SPI_enableModule()</a></li> </ul>
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Modified bits are **UCCKPH**, **UCCKPL**, **UC7BIT**, **UCMSB**, **UCSELx**, **UCSWRST** bits of **UCAxCTLW0** register

**Returns**  
true

20.4.2.43 `bool SPI_initSlave ( uint32_t moduleInstance, const eUSCI_SPI_SlaveConfig * config )`

Initializes the SPI Slave block.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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<i>config</i>	Configuration structure for SPI slave mode
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### Configuration options for `eUSCI_SPI_SlaveConfig` structure.

#### Parameters

<i>msbFirst</i>	controls the direction of the receive and transmit shift register. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_MSB_FIRST</b></li> <li>■ <b>EUSCI_SPI_LSB_FIRST</b> [Default Value]</li> </ul>
<i>clockPhase</i>	is clock phase select. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_PHASE_DATA_CHANGED_ONFIRST_CAPTURED_ON_NEXT</b> [Default Value]</li> <li>■ <b>EUSCI_SPI_PHASE_DATA_CAPTURED_ONFIRST_CHANGED_ON_NEXT</b></li> </ul>
<i>clockPolarity</i>	is clock polarity select. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_HIGH</b></li> <li>■ <b>EUSCI_SPI_CLOCKPOLARITY_INACTIVITY_LOW</b> [Default Value]</li> </ul>
<i>spiMode</i>	is SPI mode select. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_SPI_3PIN</b> [Default Value]</li> <li>■ <b>EUSCI_SPI_4PIN_UCxSTE_ACTIVE_HIGH</b></li> <li>■ <b>EUSCI_SPI_4PIN_UCxSTE_ACTIVE_LOW</b> Upon successful initialization of the SPI slave block, this function will have initialized the slave block, but the SPI Slave block still remains disabled and must be enabled with <a href="#">SPI_enableModule()</a></li> </ul>

Modified bits are **UCMSB**, **UC7BIT**, **UCMST**, **UCCKPL**, **UCCKPH**, **UCMODE**, **UCSWRST** bits of **UCAxCTLW0**

**Returns**  
true

#### 20.4.2.44 `uint_fast8_t SPI_isBusy ( uint32_t moduleInstance )`

Indicates whether or not the SPI bus is busy.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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This function returns an indication of whether or not the SPI bus is busy. This function checks the status of the bus via UCBBUSY bit

**Returns**

EUSCI\_SPI\_BUSY if the SPI module transmitting or receiving is busy; otherwise, returns EUSCI\_SPI\_NOT\_BUSY.

References [EUSCI\\_A\\_SPI\\_isBusy\(\)](#), and [EUSCI\\_B\\_SPI\\_isBusy\(\)](#).

#### 20.4.2.45 uint8\_t SPI\_receiveData ( uint32\_t *moduleInstance* )

Receives a byte that has been sent to the SPI Module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b></li> </ul>
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This function reads a byte of data from the SPI receive data Register.

**Returns**

Returns the byte received from by the SPI module, cast as an uint8\_t.

References [EUSCI\\_A\\_SPI\\_receiveData\(\)](#), and [EUSCI\\_B\\_SPI\\_receiveData\(\)](#).



20.4.2.46 void SPI\_registerInterrupt ( uint32\_t *moduleInstance*, void(\*)(void) *intHandler* )

Registers an interrupt handler for the timer capture compare interrupt.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI (SPI) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> <li>■ <b>EUSCI_B0_BASE</b></li> <li>■ <b>EUSCI_B1_BASE</b></li> <li>■ <b>EUSCI_B2_BASE</b></li> <li>■ <b>EUSCI_B3_BASE</b> It is important to note that for eUSCI modules, only "B" modules such as EUSCI_B0 can be used. "A" modules such as EUSCI_A0 do not support the I2C mode.</li> </ul>
<i>intHandler</i>	is a pointer to the function to be called when the timer capture compare interrupt occurs.

This function registers the handler to be called when a timer interrupt occurs. This function enables the global interrupt in the interrupt controller; specific SPI interrupts must be enabled via [SPI\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [SPI\\_clearInterruptFlag\(\)](#).

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

20.4.2.47 void SPI\_selectFourPinFunctionality ( uint32\_t *moduleInstance*, uint\_fast8\_t *select4PinFunctionality* )

Selects 4Pin Functionality

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
<i>select4PinFunctionality</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_SPI_PREVENT_CONFLICTS_WITH_OTHER_MASTERS</li> <li>■ EUSCI_SPI_ENABLE_SIGNAL_FOR_4WIRE_SLAVE This function should be invoked only in 4-wire mode. Invoking this function has no effect in 3-wire mode.</li> </ul>

Modified bits are **UCSTEM** bit of **UCAxCTLW0** register

**Returns**

true

References [EUSCI\\_A\\_SPI\\_select4PinFunctionality\(\)](#), and [EUSCI\\_B\\_SPI\\_select4PinFunctionality\(\)](#).

20.4.2.48 void SPI\_transmitData ( uint32\_t *moduleInstance*, uint\_fast8\_t *transmitData* )

Transmits a byte from the SPI Module.

## Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
-----------------------	---

<i>transmitData</i>	data to be transmitted from the SPI module
---------------------	--

This function will place the supplied data into SPI transmit data register to start transmission

Modified register is **UCAxTXBUF**

**Returns**

None.

References [EUSCI\\_A\\_SPI\\_transmitData\(\)](#), and [EUSCI\\_B\\_SPI\\_transmitData\(\)](#).

#### 20.4.2.49 void SPI\_unregisterInterrupt ( uint32\_t *moduleInstance* )

Unregisters the interrupt handler for the timer

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A/B module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> <li>■ EUSCI_B0_BASE</li> <li>■ EUSCI_B1_BASE</li> <li>■ EUSCI_B2_BASE</li> <li>■ EUSCI_B3_BASE</li> </ul>
-----------------------	---

This function unregisters the handler to be called when timer interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 21 System Control Module (SysCtl)

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### 21.1 Module Operation

The SysCtl module is a conglomeration of miscellaneous system control modules that do not fit into any specific hardware peripheral.

Some of the functionalities of the SysCtl module include:

- Configure and enable/disable NMI sources
- Retrieve the SRAM/Flash size through software calls
- Disable/enable SRAM banks completely as well as disable retention during sleep
- Enable/disable GPIO glitch filters
- Change the type of reset that occurs on a WDT violation

### 21.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the SysCtl module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to retrieve the Flash and SRAM sizes using a software API. This is useful if the programmer is making a program that is meant to be run on multiple devices in the MSP432 family with different memory footprints.

```
int main(void)
{
    /* Variables we will store the sizes in. Declared volatile so the compiler
     * does not optimize out
     */
    volatile uint32_t sramSize, flashSize;

    /* Halting the Watchdog */
    MAP_WDT_A_holdTimer();

    sramSize = MAP_SysCtl_getSRAMSize();
    flashSize = MAP_SysCtl_getFlashSize();

    /* No operation. Set Breakpoint here */
    __no_operation();
}
```

## 21.3 Definitions

### Functions

- void [SysCtl\\_disableGlitchFilter](#) (void)
- void [SysCtl\\_disableNMISource](#) (uint\_fast8\_t flags)
- void [SysCtl\\_disablePeripheralAtCPUHalt](#) (uint\_fast16\_t devices)
- void [SysCtl\\_disableSRAMBank](#) (uint\_fast8\_t sramBank)
- void [SysCtl\\_disableSRAMBankRetention](#) (uint\_fast8\_t sramBank)
- void [SysCtl\\_enableGlitchFilter](#) (void)
- void [SysCtl\\_enableNMISource](#) (uint\_fast8\_t flags)
- void [SysCtl\\_enablePeripheralAtCPUHalt](#) (uint\_fast16\_t devices)
- void [SysCtl\\_enableSRAMBank](#) (uint\_fast8\_t sramBank)
- void [SysCtl\\_enableSRAMBankRetention](#) (uint\_fast8\_t sramBank)
- uint\_least32\_t [SysCtl\\_getFlashSize](#) (void)
- uint\_fast8\_t [SysCtl\\_getNMISourceStatus](#) (void)
- uint\_least32\_t [SysCtl\\_getSRAMSize](#) (void)
- uint\_fast16\_t [SysCtl\\_getTempCalibrationConstant](#) (uint32\_t refVoltage, uint32\_t temperature)
- void [SysCtl\\_getTLVInfo](#) (uint\_fast8\_t tag, uint\_fast8\_t instance, uint\_fast8\_t \*length, uint32\_t \*\*data\_address)
- void [SysCtl\\_rebootDevice](#) (void)
- void [SysCtl\\_setWDTPasswordViolationResetType](#) (uint\_fast8\_t resetType)
- void [SysCtl\\_setWDTTimeoutResetType](#) (uint\_fast8\_t resetType)

### 21.3.1 Detailed Description

The code for this module is contained in `driverlib/sysctl.c`, with `driverlib/sysctl.h` containing the API declarations for use by applications.

## 21.3.2 Function Documentation

### 21.3.2.1 void SysCtl\_disableGlitchFilter ( void )

Disables glitch suppression on the reset pin of the device. Refer to the device data sheet for specific information about glitch suppression

#### Returns

None.

### 21.3.2.2 void SysCtl\_disableNMISource ( uint\_fast8\_t *flags* )

Disables NMIs for the provided modules. When disabled, a NMI flag will not occur when a fault condition comes from the corresponding modules.

#### Parameters

<i>flags</i>	The NMI sources to disable Can be a bitwise OR of the following parameters: <ul style="list-style-type: none"> <li>■ <b>SYSCTL_NMIPIN_SRC,</b></li> <li>■ <b>SYSCTL_PCM_SRC,</b></li> <li>■ <b>SYSCTL_PSS_SRC,</b></li> <li>■ <b>SYSCTL_CS_SRC</b></li> </ul>
--------------	---

Referenced by [CS\\_startHFXTWithTimeout\(\)](#), and [CS\\_startLFXTWithTimeout\(\)](#).

### 21.3.2.3 void SysCtl\_disablePeripheralAtCPUHalt ( uint\_fast16\_t *devices* )

Makes it so that the provided peripherals will either halt execution after a CPU HALT. Parameters in this function can be combined to account for multiple peripherals. By default, all peripherals keep running after a CPU HALT.

#### Parameters

<i>devices</i>	The peripherals to disable after a CPU HALT
----------------	---

The *devices* parameter can be a bitwise OR of the following values: This can be a bitwise OR of the following values:

- **SYSCTL\_PERIPH\_DMA,**
- **SYSCTL\_PERIPH\_WDT,**
- **SYSCTL\_PERIPH\_ADC,**
- **SYSCTL\_PERIPH\_EUSCIB3,**
- **SYSCTL\_PERIPH\_EUSCIB2,**
- **SYSCTL\_PERIPH\_EUSCIB1**
- **SYSCTL\_PERIPH\_EUSCIB0,**
- **SYSCTL\_PERIPH\_EUSCIA3,**
- **SYSCTL\_PERIPH\_EUSCIA2**

- SYSCTL\_PERIPH\_EUSCIA1,
- SYSCTL\_PERIPH\_EUSCIA0,
- SYSCTL\_PERIPH\_TIMER32\_0\_MODULE,
- SYSCTL\_PERIPH\_TIMER16\_3,
- SYSCTL\_PERIPH\_TIMER16\_2,
- SYSCTL\_PERIPH\_TIMER16\_1,
- SYSCTL\_PERIPH\_TIMER16\_0

**Returns**

None.

21.3.2.4 void SysCtl\_disableSRAMBank ( uint\_fast8\_t *sramBank* )

Disables a set of banks in the SRAM. This can be used to optimize power consumption when every SRAM bank isn't needed. It is important to note that when a higher bank is disabled, all of the SRAM banks above that bank are also disabled. For example, if the user disables SYSCTL\_SRAM\_BANK5, the banks SYSCTL\_SRAM\_BANK6 through SYSCTL\_SRAM\_BANK7 will be disabled.

**Parameters**

<i>sramBank</i>	<p>The SRAM bank tier to disable. Must be only one of the following values:</p> <ul style="list-style-type: none"> <li>■ SYSCTL_SRAM_BANK1,</li> <li>■ SYSCTL_SRAM_BANK2,</li> <li>■ SYSCTL_SRAM_BANK3,</li> <li>■ SYSCTL_SRAM_BANK4,</li> <li>■ SYSCTL_SRAM_BANK5,</li> <li>■ SYSCTL_SRAM_BANK6,</li> <li>■ SYSCTL_SRAM_BANK7</li> </ul>
-----------------	---

**Note**

**SYSCTL\_SRAM\_BANK0** is reserved and always enabled.

**Returns**

None.

21.3.2.5 void SysCtl\_disableSRAMBankRetention ( uint\_fast8\_t *sramBank* )

Disables retention of the specified SRAM bank register when the device goes into LPM3 mode. When the system is placed in LPM3 mode, the SRAM banks specified with this function will not be placed into retention mode. By default, retention of every SRAM bank except SYSCTL\_SRAM\_BANK0 (reserved) is disabled. Retention of individual banks can be set without the restrictions of the enable/disable SRAM bank functions.



## Parameters

<i>sramBank</i>	<p>The SRAM banks to disable retention Can be a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>SYSCTL_SRAM_BANK1,</b></li> <li>■ <b>SYSCTL_SRAM_BANK2,</b></li> <li>■ <b>SYSCTL_SRAM_BANK3,</b></li> <li>■ <b>SYSCTL_SRAM_BANK4,</b></li> <li>■ <b>SYSCTL_SRAM_BANK5,</b></li> <li>■ <b>SYSCTL_SRAM_BANK6,</b></li> <li>■ <b>SYSCTL_SRAM_BANK7</b></li> </ul>
-----------------	--

**Note**

**SYSCTL\_SRAM\_BANK0** is reserved and retention is always enabled.

**Returns**

None.

## 21.3.2.6 void SysCtl\_enableGlitchFilter ( void )

Enables glitch suppression on the reset pin of the device. Refer to the device data sheet for specific information about glitch suppression

**Returns**

None.

## 21.3.2.7 void SysCtl\_enableNMISource ( uint\_fast8\_t flags )

Enables NMIs for the provided modules. When enabled, a NMI flag will occur when a fault condition comes from the corresponding modules.

## Parameters

<i>flags</i>	<p>The NMI sources to enable Can be a bitwise OR of the following parameters:</p> <ul style="list-style-type: none"> <li>■ <b>SYSCTL_NMIPIN_SRC,</b></li> <li>■ <b>SYSCTL_PCM_SRC,</b></li> <li>■ <b>SYSCTL_PSS_SRC,</b></li> <li>■ <b>SYSCTL_CS_SRC</b></li> </ul>
--------------	---

Referenced by [CS\\_startHFXTWithTimeout\(\)](#), and [CS\\_startLFXTWithTimeout\(\)](#).

## 21.3.2.8 void SysCtl\_enablePeripheralAtCPUHalt ( uint\_fast16\_t devices )

Makes it so that the provided peripherals will either halt execution after a CPU HALT. Parameters in this function can be combined to account for multiple peripherals. By default, all peripherals

keep running after a CPU HALT.

## Parameters

<i>devices</i>	<p>The peripherals to continue running after a CPU HALT. This can be a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>SYSCCTL_PERIPH_DMA,</b></li> <li>■ <b>SYSCCTL_PERIPH_WDT,</b></li> <li>■ <b>SYSCCTL_PERIPH_ADC,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIB3,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIB2,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIB1,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIB0,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIA3,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIA2,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIA1,</b></li> <li>■ <b>SYSCCTL_PERIPH_EUSCIA0,</b></li> <li>■ <b>SYSCCTL_PERIPH_TIMER32_0_MODULE,</b></li> <li>■ <b>SYSCCTL_PERIPH_TIMER16_3,</b></li> <li>■ <b>SYSCCTL_PERIPH_TIMER16_2,</b></li> <li>■ <b>SYSCCTL_PERIPH_TIMER16_1,</b></li> <li>■ <b>SYSCCTL_PERIPH_TIMER16_0</b></li> </ul>
----------------	---

## Returns

None.

21.3.2.9 void SysCtl\_enableSRAMBank ( uint\_fast8\_t *sramBank* )

Enables a set of banks in the SRAM. This can be used to optimize power consumption when every SRAM bank isn't needed. It is important to note that when a higher bank is enabled, all of the SRAM banks below that bank are also enabled. For example, if the user enables `SYSCCTL_SRAM_BANK7`, the banks `SYSCCTL_SRAM_BANK1` through `SYSCCTL_SRAM_BANK7` will be enabled (`SRAM_BANK0` is reserved and always enabled).

## Parameters

<i>sramBank</i>	<p>The SRAM bank tier to enable. Must be only one of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>SYSCCTL_SRAM_BANK1,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK2,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK3,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK4,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK5,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK6,</b></li> <li>■ <b>SYSCCTL_SRAM_BANK7</b></li> </ul>
-----------------	--

**Note**

**SYSCTL\_SRAM\_BANK0** is reserved and always enabled.

**Returns**

None.

### 21.3.2.10 void SysCtl\_enableSRAMBankRetention ( uint\_fast8\_t *sramBank* )

Enables retention of the specified SRAM bank register when the device goes into LPM3 mode. When the system is placed in LPM3 mode, the SRAM banks specified with this function will be placed into retention mode. By default, retention of every SRAM bank except **SYSCTL\_SRAM\_BANK0** (reserved) is disabled. Retention of individual banks can be set without the restrictions of the enable/disable functions.

**Parameters**

<i>sramBank</i>	<p>The SRAM banks to enable retention Can be a bitwise OR of the following values:</p> <ul style="list-style-type: none"> <li>■ <b>SYSCTL_SRAM_BANK1</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK2</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK3</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK4</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK5</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK6</b>,</li> <li>■ <b>SYSCTL_SRAM_BANK7</b></li> </ul>
-----------------	---

**Note**

**SYSCTL\_SRAM\_BANK0** is reserved and retention is always enabled.

**Returns**

None.

### 21.3.2.11 uint\_least32\_t SysCtl\_getFlashSize ( void )

Gets the size of the flash.

**Returns**

The total number of bytes of flash.

Referenced by [FlashCtl\\_getMemoryInfo\(\)](#), [FlashCtl\\_performMassErase\(\)](#), and [FlashCtl\\_verifyMemory\(\)](#).

### 21.3.2.12 uint\_fast8\_t SysCtl\_getNMISourceStatus ( void )

Returns the current sources of NMIs that are enabled

**Returns**

Bitwise OR of NMI flags that are enabled

Referenced by [CS\\_startHFXTWithTimeout\(\)](#), and [CS\\_startLFXTWithTimeout\(\)](#).

21.3.2.13 `uint_least32_t SysCtl_getSRAMSize ( void )`

Gets the size of the SRAM.

**Returns**

The total number of bytes of SRAM.

21.3.2.14 `uint_fast16_t SysCtl_getTempCalibrationConstant ( uint32_t refVoltage, uint32_t temperature )`

Retrieves the calibration constant of the temperature sensor to be used in temperature calculation.

**Parameters**

<i>refVoltage</i>	Reference voltage being used.
-------------------	-------------------------------

The *refVoltage* parameter must be only one of the following values:

- **SYSCTL\_1\_2V\_REF**
- **SYSCTL\_1\_45V\_REF**
- **SYSCTL\_2\_5V\_REF**

**Parameters**

<i>temperature</i>	is the calibration temperature that the user wants to be returned.
--------------------	--

The *temperature* parameter must be only one of the following values:

- **SYSCTL\_30\_DEGREES\_C**
- **SYSCTL\_85\_DEGREES\_C**

**Returns**

None.

21.3.2.15 `void SysCtl_getTLVInfo ( uint_fast8_t tag, uint_fast8_t instance, uint_fast8_t * length, uint32_t ** data_address )`

The TLV structure uses a tag or base address to identify segments of the table where information is stored. Some examples of TLV tags are Peripheral Descriptor, Interrupts, Info Block and Die Record. This function retrieves the value of a tag and the length of the tag.

## Parameters

<i>tag</i>	represents the tag for which the information needs to be retrieved. Valid values are: <ul style="list-style-type: none"> <li>■ TLV_TAG_RESERVED1</li> <li>■ TLV_TAG_RESERVED2</li> <li>■ TLV_TAG_CS</li> <li>■ TLV_TAG_FLASHCTL</li> <li>■ TLV_TAG_ADC14</li> <li>■ TLV_TAG_RESERVED6</li> <li>■ TLV_TAG_RESERVED7</li> <li>■ TLV_TAG_REF</li> <li>■ TLV_TAG_RESERVED9</li> <li>■ TLV_TAG_RESERVED10</li> <li>■ TLV_TAG_DEVINFO</li> <li>■ TLV_TAG_DIEREC</li> <li>■ TLV_TAG_RANDNUM</li> <li>■ TLV_TAG_RESERVED14</li> </ul>
<i>instance</i>	In some cases a specific tag may have more than one instance. For example there may be multiple instances of timer calibration data present under a single Timer Cal tag. This variable specifies the instance for which information is to be retrieved (0, 1, etc.). When only one instance exists; 0 is passed.
<i>length</i>	Acts as a return through indirect reference. The function retrieves the value of the TLV tag length. This value is pointed to by *length and can be used by the application level once the function is called. If the specified tag is not found then the pointer is null 0.
<i>data_address</i>	acts as a return through indirect reference. Once the function is called data_address points to the pointer that holds the value retrieved from the specified TLV tag. If the specified tag is not found then the pointer is null 0.

**Returns**

None

Referenced by [CS\\_getDCOFrequency\(\)](#), [CS\\_setDCOFrequency\(\)](#), [FlashCtl\\_eraseSector\(\)](#), and [FlashCtl\\_programMemory\(\)](#).

## 21.3.2.16 void SysCtl\_rebootDevice ( void )

Reboots the device and causes the device to re-initialize itself.

**Returns**

This function does not return.

## 21.3.2.17 void SysCtl\_setWDTPasswordViolationResetType ( uint\_fast8\_t resetType )

Sets the type of RESET that happens when a watchdog password violation occurs.

**Parameters**

<i>resetType</i>	The type of reset to set
------------------	--------------------------

The *resetType* parameter must be only one of the following values:

- **SYSCTL\_HARD\_RESET**,
- **SYSCTL\_SOFT\_RESET**

**Returns**

None.

Referenced by [WDT\\_A\\_setPasswordViolationReset\(\)](#).

### 21.3.2.18 void SysCtl\_setWDTTimeoutResetType ( uint\_fast8\_t *resetType* )

Sets the type of RESET that happens when a watchdog timeout occurs.

**Parameters**

<i>resetType</i>	The type of reset to set
------------------	--------------------------

The *resetType* parameter must be only one of the following values:

- **SYSCTL\_HARD\_RESET**,
- **SYSCTL\_SOFT\_RESET**

**Returns**

None.

Referenced by [WDT\\_A\\_setTimeoutReset\(\)](#).

## 22 System Tick (SysTick)

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### 22.1 Module Operation

SysTick is a simple timer that is part of the NVIC controller in the Cortex-M microprocessor. Its intended purpose is to provide a periodic interrupt for an RTOS, but it can be used for other simple timing purposes.

The SysTick interrupt handler does not need to clear the SysTick interrupt source as it is cleared automatically by the NVIC when the SysTick interrupt handler is called.

### 22.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the SysTick module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the SysTick module to interrupt periodically and blink an LED attached to P1.0.

```
int main(void)
{
    /* Halting the Watchdog */
    MAP_WDT_A_holdTimer();

    /* Configuring GPIO as an output */
    MAP_GPIO_setAsOutputPin(GPIO_PORT_P1, GPIO_PIN0);

    /* Configuring SysTick to trigger at 1500000 (MCLK is 3MHz so this will make
    * it toggle every 0.5s) */
    MAP_SysTick_enableModule();
    MAP_SysTick_setPeriod(1500000);
    MAP_Interrupt_enableSleepOnIsrExit();
    MAP_SysTick_enableInterrupt();

    /* Enabling MASTER interrupts */
    MAP_Interrupt_enableMaster();

    while (1)
    {
        MAP_PCM_gotoLPM0();
    }
}

void SysTick_Handler(void)
{
    MAP_GPIO_toggleOutputOnPin(GPIO_PORT_P1, GPIO_PIN0);
}
```



## 22.3 Definitions

### Functions

- void [SysTick\\_disableInterrupt](#) (void)
- void [SysTick\\_disableModule](#) (void)
- void [SysTick\\_enableInterrupt](#) (void)
- void [SysTick\\_enableModule](#) (void)
- uint32\_t [SysTick\\_getPeriod](#) (void)
- uint32\_t [SysTick\\_getValue](#) (void)
- void [SysTick\\_registerInterrupt](#) (void(\*intHandler)(void))
- void [SysTick\\_setPeriod](#) (uint32\_t period)
- void [SysTick\\_unregisterInterrupt](#) (void)

### 22.3.1 Detailed Description

The code for this module is contained in `driverlib/systick.c`, with `driverlib/systick.h` containing the API declarations for use by applications.

## 22.3.2 Function Documentation

### 22.3.2.1 void SysTick\_disableInterrupt ( void )

Disables the SysTick interrupt.

This function disables the SysTick interrupt, preventing it from being reflected to the processor.

**Returns**

None.

### 22.3.2.2 void SysTick\_disableModule ( void )

Disables the SysTick counter.

This function stops the SysTick counter. If an interrupt handler has been registered, it is not called until SysTick is restarted.

**Returns**

None.

### 22.3.2.3 void SysTick\_enableInterrupt ( void )

Enables the SysTick interrupt.

This function enables the SysTick interrupt, allowing it to be reflected to the processor.

**Note**

The SysTick interrupt handler is not required to clear the SysTick interrupt source because it is cleared automatically by the NVIC when the interrupt handler is called.

**Returns**

None.

### 22.3.2.4 void SysTick\_enableModule ( void )

Enables the SysTick counter.

This function starts the SysTick counter. If an interrupt handler has been registered, it is called when the SysTick counter rolls over.

**Note**

Calling this function causes the SysTick counter to (re)commence counting from its current value. The counter is not automatically reloaded with the period as specified in a previous call to [SysTick\\_setPeriod\(\)](#). If an immediate reload is required, the **NVIC\_ST\_CURRENT** register must be written to force the reload. Any write to this register clears the SysTick counter to 0 and causes a reload with the supplied period on the next clock.

**Returns**

None.

**22.3.2.5** `uint32_t SysTick_getPeriod ( void )`

Gets the period of the SysTick counter.

This function returns the rate at which the SysTick counter wraps, which equates to the number of processor clocks between interrupts.

**Returns**

Returns the period of the SysTick counter.

**22.3.2.6** `uint32_t SysTick_getValue ( void )`

Gets the current value of the SysTick counter.

This function returns the current value of the SysTick counter, which is a value between the period - 1 and zero, inclusive.

**Returns**

Returns the current value of the SysTick counter.

**22.3.2.7** `void SysTick_registerInterrupt ( void(*)(void) intHandler )`

Registers an interrupt handler for the SysTick interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the SysTick interrupt occurs.
-------------------	--

This function registers the handler to be called when a SysTick interrupt occurs.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_registerInterrupt\(\)](#).

**22.3.2.8** `void SysTick_setPeriod ( uint32_t period )`

Sets the period of the SysTick counter.

**Parameters**

<i>period</i>	is the number of clock ticks in each period of the SysTick counter and must be between 1 and 16, 777, 216, inclusive.
---------------	---

This function sets the rate at which the SysTick counter wraps, which equates to the number of processor clocks between interrupts.

**Note**

Calling this function does not cause the SysTick counter to reload immediately. If an immediate reload is required, the **NVIC\_ST\_CURRENT** register must be written. Any write to this register clears the SysTick counter to 0 and causes a reload with the *period* supplied here on the next clock after SysTick is enabled.

**Returns**

None.

### 22.3.2.9 void SysTick\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the SysTick interrupt.

This function unregisters the handler to be called when a SysTick interrupt occurs.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_unregisterInterrupt\(\)](#).

## 23 32-bit ARM Timer (Timer32)

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### 23.1 Module Operation

The Timer32 module in MSP432 is a simple 32-bit (or 16-bit depending on configuration) down counter which was implemented by ARM. While the user's guide for Timer32 treats the module as one unified timer, the DriverLib API separates the two timers into two separate modules. To choose between the module, the user either provides `TIMER32_0` or `TIMER32_1` to the timer in order to specify which timer is to be used.

### 23.2 Basic Operation Modes

**Free Run Mode** In free run mode, the timer will run from a value of `UINT16_MAX` or `UINT32_MAX` (depending on what resolution is selected).

**Periodic Mode** In periodic mode, the timer will run to a specified period by the user.

For both periodic and free run modes, the one shot boolean option in the [Timer32\\_startTimer\(\)](#) function. If specified, when the count reaches zero from the specified period the timer will stop and not automatically resume with the next iteration of the count.

## 23.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the Timer32 module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the Timer32 as a simple down counter with interrupts enabled:

```
int main(void)
{
    volatile uint32_t curValue;

    /* Holding the Watchdog */
    MAP_WDT_A_holdTimer();

    /* Initializing Timer32 in module in 32-bit free-run mode (with max value
     * of 0xFFFFFFFF
     */
    MAP_Timer32_initModule(TIMER32_BASE, TIMER32_PRESCALER_256, TIMER32_32BIT,
        TIMER32_FREE_RUN_MODE);

    /* Starting the timer */
    MAP_Timer32_startTimer(TIMER32_BASE, true);

    while(1)
    {
        /* Getting the current value of the Timer32 */
        curValue = MAP_Timer32_getValue(TIMER32_BASE);
    }
}
```

## 23.4 Definitions

### Functions

- void [Timer32\\_clearInterruptFlag](#) (uint32\_t timer)
- void [Timer32\\_disableInterrupt](#) (uint32\_t timer)
- void [Timer32\\_enableInterrupt](#) (uint32\_t timer)
- uint32\_t [Timer32\\_getInterruptStatus](#) (uint32\_t timer)
- uint32\_t [Timer32\\_getValue](#) (uint32\_t timer)
- void [Timer32\\_haltTimer](#) (uint32\_t timer)
- void [Timer32\\_initModule](#) (uint32\_t timer, uint32\_t preScaler, uint32\_t resolution, uint32\_t mode)
- void [Timer32\\_registerInterrupt](#) (uint32\_t timerInterrupt, void(\*intHandler)(void))
- void [Timer32\\_setCount](#) (uint32\_t timer, uint32\_t count)
- void [Timer32\\_setCountInBackground](#) (uint32\_t timer, uint32\_t count)
- void [Timer32\\_startTimer](#) (uint32\_t timer, bool oneShot)
- void [Timer32\\_unregisterInterrupt](#) (uint32\_t timerInterrupt)

### 23.4.1 Detailed Description

The code for this module is contained in `driverlib/timer32.c`, with `driverlib/timer32.h` containing the API declarations for use by applications.

## 23.4.2 Function Documentation

### 23.4.2.1 void Timer32\_clearInterruptFlag ( uint32\_t *timer* )

Clears Timer32 interrupt source.

#### Parameters

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

The Timer32 interrupt source is cleared, so that it no longer asserts.

#### Returns

None.

### 23.4.2.2 void Timer32\_disableInterrupt ( uint32\_t *timer* )

Disables a Timer32 interrupt source.

#### Parameters

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

Disables the indicated Timer32 interrupt source.

#### Returns

None.

### 23.4.2.3 void Timer32\_enableInterrupt ( uint32\_t *timer* )

Enables a Timer32 interrupt source.

#### Parameters

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

Enables the indicated Timer32 interrupt source.



**Returns**

None.

23.4.2.4 uint32\_t Timer32\_getInterruptStatus ( uint32\_t *timer* )

Gets the current Timer32 interrupt status.

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

This returns the interrupt status for the Timer32 module. A positive value will indicate that an interrupt is pending while a zero value will indicate that no interrupt is pending.

**Returns**

The current interrupt status

23.4.2.5 uint32\_t Timer32\_getValue ( uint32\_t *timer* )

Returns the current value of the timer.

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

**Returns**

The current count of the timer.

23.4.2.6 void Timer32\_haltTimer ( uint32\_t *timer* )

Halts the timer. Current count and setting values are preserved.

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
--------------	---

**Returns**

None

23.4.2.7 void Timer32\_initModule ( uint32\_t *timer*, uint32\_t *preScaler*, uint32\_t *resolution*, uint32\_t *mode* )

Initializes the Timer32 module

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
<i>preScaler</i>	is the prescaler (or divider) to apply to the clock source given to the Timer32 module. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER32_PRESCALER_1</b> [DEFAULT]</li> <li>■ <b>TIMER32_PRESCALER_16</b></li> <li>■ <b>TIMER32_PRESCALER_256</b></li> </ul>
<i>resolution</i>	is the bit resolution of the Timer32 module. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER32_16BIT</b> [DEFAULT]</li> <li>■ <b>TIMER32_32BIT</b></li> </ul>
<i>mode</i>	selects between free run and periodic mode. In free run mode, the value of the timer is reset to UINT16_MAX (for 16-bit mode) or UINT32_MAX (for 32-bit mode) when the timer reaches zero. In periodic mode, the timer is reset to the value set by the Timer32_setCount function. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER32_FREE_RUN_MODE</b> [DEFAULT]</li> <li>■ <b>TIMER32_PERIODIC_MODE</b></li> </ul>

**Returns**

None.

23.4.2.8 void Timer32\_registerInterrupt ( uint32\_t *timerInterrupt*, void(\*)*(void) intHandler* )

Registers an interrupt handler for Timer32 interrupts.

**Parameters**

<i>timerInterrupt</i>	is the specific interrupt to register. For the Timer32 module, there are a total of three different interrupts: one interrupt for each two Timer32 modules, and a "combined" interrupt which is a logical OR of each individual Timer32 interrupt. <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_INTERRUPT</b></li> <li>■ <b>TIMER32_1_INTERRUPT</b></li> <li>■ <b>TIMER32_COMBINED_INTERRUPT</b></li> </ul>
<i>intHandler</i>	is a pointer to the function to be called when the Timer32 interrupt occurs.

This function registers the handler to be called when an Timer32 interrupt occurs. This function enables the global interrupt in the interrupt controller; specific Timer32 interrupts must be enabled via [Timer32\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [Timer32\\_clearInterruptFlag\(\)](#).

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).23.4.2.9 void Timer32\_setCount ( uint32\_t *timer*, uint32\_t *count* )

Sets the count of the timer and resets the current value to the value passed. This value is set on the next rising edge of the clock provided to the timer module

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
<i>count</i>	Value of the timer to set. Note that if the timer is in 16-bit mode and a value is passed in that exceeds UINT16_MAX, the value will be truncated to UINT16_MAX.

Also note that if the timer is operating in periodic mode, the value passed into this function will represent the new period of the timer (the value which is reloaded into the timer each time it reaches a zero value).

**Returns**

None

#### 23.4.2.10 void Timer32\_setCountInBackground ( uint32\_t *timer*, uint32\_t *count* )

Sets the count of the timer without resetting the current value. When the current value of the timer reaches zero, the value passed into this function will be set as the new count value.

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
<i>count</i>	Value of the timer to set in the background. Note that if the timer is in 16-bit mode and a value is passed in that exceeds UINT16_MAX, the value will be truncated to UINT16_MAX.

Also note that if the timer is operating in periodic mode, the value passed into this function will represent the new period of the timer (the value which is reloaded into the timer each time it reaches a zero value).

**Returns**

None

23.4.2.11 void Timer32\_startTimer ( uint32\_t *timer*, bool *oneShot* )

Starts the timer. The Timer32\_initModule function should be called (in conjunction with Timer32\_setCount if periodic mode is desired) prior to

**Parameters**

<i>timer</i>	is the instance of the Timer32 module. Valid parameters must be one of the following values: <ul style="list-style-type: none"> <li>■ <b>TIMER32_0_BASE</b></li> <li>■ <b>TIMER32_1_BASE</b></li> </ul>
<i>oneShot</i>	sets whether the Timer32 module operates in one shot or continuous mode. In one shot mode, the timer will halt when a zero is reached and stay halted until either: <ul style="list-style-type: none"> <li>■ The user calls the Timer32PeriodSet function</li> <li>■ The Timer32_initModule is called to reinitialize the timer with one-shot mode disabled.</li> </ul>

A true value will cause the timer to operate in one shot mode while a false value will cause the timer to operate in continuous mode

**Returns**

None

23.4.2.12 void Timer32\_unregisterInterrupt ( uint32\_t *timerInterrupt* )

Unregisters the interrupt handler for the Timer32 interrupt.

**Parameters**

<i>timerInterrupt</i>	is the specific interrupt to register. For the Timer32 module, there are a total of three different interrupts: one interrupt for each two Timer32 modules, and a "combined" interrupt which is a logical OR of each individual Timer32 interrupt. <ul style="list-style-type: none"><li>■ <b>TIMER32_0_INTERRUPT</b></li><li>■ <b>TIMER32_1_INTERRUPT</b></li><li>■ <b>TIMER32_COMBINED_INTERRUPT</b></li></ul>
-----------------------	--

This function unregisters the handler to be called when a Timer32 interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 24 16-Bit Timer with Precision PWM (Timer\_A)

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### 24.1 Module Operation

TimerA is a 16-bit timer/counter with multiple capture/compare registers. TimerA can support multiple capture/compares, PWM outputs, and interval timing. TimerA also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

This peripheral API handles Timer A hardware peripheral.

TimerA features include:

- Asynchronous 16-bit timer/counter with four operating modes
- Selectable and configurable clock source
- Up to seven configurable capture/compare registers
- Configurable outputs with pulse width modulation (PWM) capability
- Asynchronous input and output latching
- Interrupt vector register for fast decoding of all Timer interrupts

### 24.2 Basic Operation Modes

TimerA can operate in 3 modes:

- Continuous Mode
- Up Mode
- Down Mode

TimerA Interrupts may be generated on counter overflow conditions and during capture compare events.

The TimerA may also be used to generate PWM outputs. PWM outputs can be generated by initializing the compare mode with `TimerA_initCompare()` and the necessary parameters. The PWM may be customized by selecting a desired timer mode (continuous/up/upDown), duty cycle, output mode, timer period etc. The library also provides a simpler way to generate PWM using `TimerA_generatePWM()` API. However the level of customization and the kinds of PWM generated are limited in this API. Depending on how complex the PWM is and what level of customization is required, the user can use `TimerA_generatePWM()` or a combination of `TimerA_initCompare` and timer start APIs.

The TimerA API provides a set of functions for dealing with the TimerA module. Functions are provided to configure and control the timer, along with functions to modify timer/counter values, and to manage interrupt handling for the timer.

Control is also provided over interrupt sources and events. Interrupts can be generated to indicate that an event has been captured.

## 24.3 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the TimerA module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to generate a PWM signal using the TimerA DriverLib module.

Below is the configuration parameter for the TimerA PWM config API:

```
/* Timer_A PWM Configuration Parameter */
Timer_A_PWMConfig pwmConfig =
{
    TIMER_A_CLOCKSOURCE_SMCLK,
    TIMER_A_CLOCKSOURCE_DIVIDER_1,
    32000,
    TIMER_A_CAPTURECOMPARE_REGISTER_1,
    TIMER_A_OUTPUTMODE_RESET_SET,
    3200
};
```

The next snippet of code is used to actually configure the PWM signal:

```
/* Setting MCLK to REFO at 128Khz for LF mode
 * Setting SMCLK to 64Khz */
MAP_CS_setReferenceOscillatorFrequency(CS_REFO_128KHZ);
MAP_CS_initClockSignal(CS_MCLK, CS_REFOCLK_SELECT, CS_CLOCK_DIVIDER_1);
MAP_CS_initClockSignal(CS_SMCLK, CS_REFOCLK_SELECT, CS_CLOCK_DIVIDER_2);
MAP_PCM_setPowerState(PCM_AM_LF_VCORE0);

/* Configuring GPIO2.4 as peripheral output for PWM and P6.7 for button
 * interrupt */
MAP_GPIO_setAsPeripheralModuleFunctionOutputPin(GPIO_PORT_P2, GPIO_PIN4,
    GPIO_PRIMARY_MODULE_FUNCTION);
MAP_GPIO_setAsInputPinWithPullUpResistor(GPIO_PORT_P1, GPIO_PIN1);
MAP_GPIO_clearInterruptFlag(GPIO_PORT_P1, GPIO_PIN1);
MAP_GPIO_enableInterrupt(GPIO_PORT_P1, GPIO_PIN1);

/* Configuring Timer_A to have a period of approximately 500ms and
 * an initial duty cycle of 10% of that (3200 ticks) */
MAP_Timer_A_generatePWM(TIMER_A0_BASE, &pwmConfig);
```



## 24.4 Definitions

### Data Structures

- struct [\\_Timer\\_A\\_CaptureModeConfig](#)
- struct [\\_Timer\\_A\\_CompareModeConfig](#)
- struct [\\_Timer\\_A\\_ContinuousModeConfig](#)
- struct [\\_Timer\\_A\\_PWMConfig](#)
- struct [\\_Timer\\_A\\_UpDownModeConfig](#)
- struct [\\_Timer\\_A\\_UpModeConfig](#)

### Functions

- void [Timer\\_A\\_clearCaptureCompareInterrupt](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- void [Timer\\_A\\_clearInterruptFlag](#) (uint32\_t timer)
- void [Timer\\_A\\_clearTimer](#) (uint32\_t timer)
- void [Timer\\_A\\_configureContinuousMode](#) (uint32\_t timer, const [Timer\\_A\\_ContinuousModeConfig](#) \*config)
- void [Timer\\_A\\_configureUpDownMode](#) (uint32\_t timer, const [Timer\\_A\\_UpDownModeConfig](#) \*config)
- void [Timer\\_A\\_configureUpMode](#) (uint32\_t timer, const [Timer\\_A\\_UpModeConfig](#) \*config)
- void [Timer\\_A\\_disableCaptureCompareInterrupt](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- void [Timer\\_A\\_disableInterrupt](#) (uint32\_t timer)
- void [Timer\\_A\\_enableCaptureCompareInterrupt](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- void [Timer\\_A\\_enableInterrupt](#) (uint32\_t timer)
- void [Timer\\_A\\_generatePWM](#) (uint32\_t timer, const [Timer\\_A\\_PWMConfig](#) \*config)
- uint\_fast16\_t [Timer\\_A\\_getCaptureCompareCount](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- uint32\_t [Timer\\_A\\_getCaptureCompareEnabledInterruptStatus](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- uint32\_t [Timer\\_A\\_getCaptureCompareInterruptStatus](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister, uint\_fast16\_t mask)
- uint16\_t [Timer\\_A\\_getCounterValue](#) (uint32\_t timer)
- uint32\_t [Timer\\_A\\_getEnabledInterruptStatus](#) (uint32\_t timer)
- uint32\_t [Timer\\_A\\_getInterruptStatus](#) (uint32\_t timer)
- uint\_fast8\_t [Timer\\_A\\_getOutputForOutputModeOutBitValue](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister)
- uint\_fast8\_t [Timer\\_A\\_getSynchronizedCaptureCompareInput](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister, uint\_fast16\_t synchronizedSetting)
- void [Timer\\_A\\_initCapture](#) (uint32\_t timer, const [Timer\\_A\\_CaptureModeConfig](#) \*config)
- void [Timer\\_A\\_initCompare](#) (uint32\_t timer, const [Timer\\_A\\_CompareModeConfig](#) \*config)
- void [Timer\\_A\\_registerInterrupt](#) (uint32\_t timer, uint\_fast8\_t interruptSelect, void(\*intHandler)(void))
- void [Timer\\_A\\_setCompareValue](#) (uint32\_t timer, uint\_fast16\_t compareRegister, uint\_fast16\_t compareValue)
- void [Timer\\_A\\_setOutputForOutputModeOutBitValue](#) (uint32\_t timer, uint\_fast16\_t captureCompareRegister, uint\_fast8\_t outputModeOutBitValue)
- void [Timer\\_A\\_startCounter](#) (uint32\_t timer, uint\_fast16\_t timerMode)
- void [Timer\\_A\\_stopTimer](#) (uint32\_t timer)
- void [Timer\\_A\\_unregisterInterrupt](#) (uint32\_t timer, uint\_fast8\_t interruptSelect)

## 24.4.1 Detailed Description

The code for this module is contained in `driverlib/timer_a.c`, with `driverlib/timer_a.h` containing the API declarations for use by applications.

## 24.4.2 Function Documentation

### 24.4.2.1 void Timer\_A\_clearCaptureCompareInterrupt ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Clears the capture-compare interrupt flag

#### Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>captureCompareRegister</i>	selects the Capture-compare register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to the datasheet to ensure the device has the capture compare register being used

#### Returns

None

### 24.4.2.2 void Timer\_A\_clearInterruptFlag ( uint32\_t *timer* )

Clears the Timer TAIFG interrupt flag

#### Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
--------------	---

**Returns**

None

24.4.2.3 void Timer\_A\_clearTimer ( uint32\_t *timer* )

Reset/Clear the timer clock divider, count direction, count

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
--------------	---

**Returns**

None

24.4.2.4 void Timer\_A\_configureContinuousMode ( uint32\_t *timer*, const **Timer\_A\_ContinuousModeConfig** \* *config* )

Configures Timer\_A in continuous mode.

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for Timer_A continuous mode

**Configuration options for Timer\_A\_ContinuousModeConfig structure.**

## Parameters

<i>clockSource</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_EXTERNAL_TXCLK</b> [Default value]</li> <li>■ <b>TIMER_A_CLOCKSOURCE_ACLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_INVERTED_EXTERNAL_TXCLK</b></li> </ul>
<i>timerInterruptEnable_TAIE</i>	is the divider for Clock source. Valid values are: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_1</b> [Default value]</li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_2</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_4</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_8</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_3</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_5</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_6</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_7</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_10</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_12</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_14</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_16</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_20</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_24</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_28</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_32</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_40</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_48</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_56</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_64</b></li> </ul>

<i>timerInterruptEnable_TAIE</i>	is to enable or disable Timer_A interrupt. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_TAIE_INTERRUPT_ENABLE</b></li> <li>■ <b>TIMER_A_TAIE_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>timerClear</i>	decides if Timer_A clock divider, count direction, count need to be reset. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_DO_CLEAR</b></li> <li>■ <b>TIMER_A_SKIP_CLEAR</b> [Default value]</li> </ul>

**Note**

This API does not start the timer. Timer needs to be started when required using the `Timer_A_startCounter` API.

**Returns**

None

24.4.2.5 `void Timer_A_configureUpDownMode ( uint32_t timer, const Timer_A_UpDownModeConfig * config )`

Configures Timer\_A in up down mode.

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for Timer_A UpDown mode

**Configuration options for Timer\_A\_UpDownModeConfig structure.****Parameters**

<i>clockSource</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_EXTERNAL_TXCLK</b> [Default value]</li> <li>■ <b>TIMER_A_CLOCKSOURCE_ACLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_INVERTED_EXTERNAL_TXCLK</b></li> </ul>
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<i>clockSourceDivider</i>	<p>is the divider for Clock source. Valid values are:</p> <ul style="list-style-type: none"><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_1</b> [Default value]</li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_2</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_4</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_8</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_3</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_5</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_6</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_7</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_10</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_12</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_14</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_16</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_20</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_24</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_28</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_32</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_40</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_48</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_56</b></li><li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_64</b></li></ul>
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<i>timerPeriod</i>	is the specified Timer_A period
<i>timerInterruptEnable_TAIE</i>	is to enable or disable Timer_A interrupt. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_TAIE_INTERRUPT_ENABLE</b></li> <li>■ <b>TIMER_A_TAIE_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>captureCompareInterruptEnable_CCR0_CCIE</i>	is to enable or disable Timer_A CCR0 captureCompare interrupt. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CCIE_CCR0_INTERRUPT_ENABLE</b> and</li> <li>■ <b>TIMER_A_CCIE_CCR0_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>timerClear</i>	decides if Timer_A clock divider, count direction, count need to be reset. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_DO_CLEAR</b></li> <li>■ <b>TIMER_A_SKIP_CLEAR</b> [Default value]</li> </ul>

This API does not start the timer. Timer needs to be started when required using the `Timer_A_startCounter` API.

#### Returns

None

#### 24.4.2.6 void Timer\_A\_configureUpMode ( uint32\_t timer, const Timer\_A\_UpModeConfig \* config )

Configures Timer\_A in up mode.

#### Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for Timer_A Up mode

**Configuration options for Timer\_A\_UpModeConfig structure.**



## Parameters

<i>clockSource</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_EXTERNAL_TXCLK</b> [Default value]</li> <li>■ <b>TIMER_A_CLOCKSOURCE_ACLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_INVERTED_EXTERNAL_TXCLK</b></li> </ul>
<i>clockSourceDivider</i>	is the divider for Clock source. Valid values are: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_1</b> [Default value]</li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_2</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_4</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_8</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_3</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_5</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_6</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_7</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_10</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_12</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_14</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_16</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_20</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_24</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_28</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_32</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_40</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_48</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_56</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_64</b></li> </ul>

<i>timerPeriod</i>	is the specified Timer_A period. This is the value that gets written into the CCR0. Limited to 16 bits[uint16_t]
<i>timerInterruptEnable_TAIE</i>	is to enable or disable Timer_A interrupt. Valid values are: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_TAIE_INTERRUPT_ENABLE</b> and</li> <li>■ <b>TIMER_A_TAIE_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>captureCompareInterruptEnable_CCR0_CCIE</i>	is to enable or disable Timer_A CCR0 captureCompare interrupt. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CCIE_CCR0_INTERRUPT_ENABLE</b> and</li> <li>■ <b>TIMER_A_CCIE_CCR0_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>timerClear</i>	decides if Timer_A clock divider, count direction, count need to be reset. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_DO_CLEAR</b></li> <li>■ <b>TIMER_A_SKIP_CLEAR</b> [Default value]</li> </ul>

**Note**

This API does not start the timer. Timer needs to be started when required using the `Timer_A_startCounter` API.

**Returns**

None

#### 24.4.2.7 void Timer\_A\_disableCaptureCompareInterrupt ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Disable capture compare interrupt

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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<i>captureCompareRegister</i>	is the selected capture compare register
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**Returns**

None

24.4.2.8 void Timer\_A\_disableInterrupt ( uint32\_t *timer* )

Disable timer interrupt

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

None

24.4.2.9 void Timer\_A\_enableCaptureCompareInterrupt ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Enable capture compare interrupt

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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<i>captureCompareRegister</i>	is the selected capture compare register
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**Returns**

None

24.4.2.10 void Timer\_A\_enableInterrupt ( uint32\_t *timer* )

Enable timer interrupt

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

None

24.4.2.11 void Timer\_A\_generatePWM ( uint32\_t *timer*, const **Timer\_A\_PWMConfig** \* *config* )

Generate a PWM with timer running in up mode

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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<i>config</i>	Configuration structure for Timer_A PWM mode
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**Configuration options for Timer\_A\_PWMConfig structure.****Parameters**

<i>clockSource</i>	<p>selects Clock source. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_EXTERNAL_TXCLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_ACLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_INVERTED_EXTERNAL_TXCLK</b></li> </ul>
<i>clockSourceDivider</i>	<p>is the divider for Clock source. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_1</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_2</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_4</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_8</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_3</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_5</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_6</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_7</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_10</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_12</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_14</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_16</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_20</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_24</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_28</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_32</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_40</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_48</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_56</b></li> <li>■ <b>TIMER_A_CLOCKSOURCE_DIVIDER_64</b></li> </ul>

<i>timerPeriod</i>	selects the desired timer period
<i>compareRegister</i>	selects the compare register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used
<i>compareOutputMode</i>	specifies the output mode. Valid values are: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_OUTPUTMODE_OUTBITVALUE,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_SET,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_RESET,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_SET_RESET</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_SET,</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET_SET</b></li> </ul>
<i>dutyCycle</i>	specifies the dutycycle for the generated waveform

**Returns**

None

#### 24.4.2.12 uint\_fast16\_t Timer\_A\_getCaptureCompareCount ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Get current capture compare count

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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<i>captureCompareRegister</i>	<p>selects the Capture register being used. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> <p>Refer to datasheet to ensure the device has the capture compare register being used</p>
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**Returns**

current count as uint16\_t

#### 24.4.2.13 uint32\_t Timer\_A\_getCaptureCompareEnabledInterruptStatus ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Return capture compare interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Parameters**

<i>timer</i>	<p>is the instance of the Timer_A module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>captureCompareRegister</i>	is the selected capture compare register

**Returns**

uint32\_t. The mask of the set flags. Valid values is an OR of

- **TIMER\_A\_CAPTURE\_OVERFLOW,**
- **TIMER\_A\_CAPTURECOMPARE\_INTERRUPT\_FLAG**

References [Timer\\_A\\_getCaptureCompareInterruptStatus\(\)](#).

#### 24.4.2.14 uint32\_t Timer\_A\_getCaptureCompareInterruptStatus ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister*, uint\_fast16\_t *mask* )

Return capture compare interrupt status

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>captureCompareRegister</i>	is the selected capture compare register
<i>mask</i>	is the mask for the interrupt status Mask value is the logical OR of any of the following: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURE_OVERFLOW</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_INTERRUPT_FLAG</b></li> </ul>

**Returns**

uint32\_t. The mask of the set flags. Valid values is an OR of

- **TIMER\_A\_CAPTURE\_OVERFLOW,**
- **TIMER\_A\_CAPTURECOMPARE\_INTERRUPT\_FLAG**

Referenced by [Timer\\_A\\_getCaptureCompareEnabledInterruptStatus\(\)](#).

#### 24.4.2.15 uint16\_t Timer\_A\_getCounterValue ( uint32\_t timer )

Returns the current value of the specified timer. Note that according to the Timer A user guide, reading the value of the counter is unreliable if the system clock is asynchronous from the timer clock. The API addresses this concern by reading the timer count register twice and then determining the integrity of the value. If the two values are within 10 timer counts of each other, the value is deemed safe and returned. If not, the process is repeated until a reliable timer value is determined.

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

The value of the specified timer

24.4.2.16 uint32\_t Timer\_A\_getEnabledInterruptStatus ( uint32\_t *timer* )

Get timer interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

uint32\_t. Return interrupt status. Valid values are

- **TIMER\_A\_INTERRUPT\_PENDING**
- **TIMER\_A\_INTERRUPT\_NOT\_PENDING**

References [Timer\\_A\\_getInterruptStatus\(\)](#).

24.4.2.17 uint32\_t Timer\_A\_getInterruptStatus ( uint32\_t *timer* )

Get timer interrupt status

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

uint32\_t. Return interrupt status. Valid values are

- **TIMER\_A\_INTERRUPT\_PENDING**
- **TIMER\_A\_INTERRUPT\_NOT\_PENDING**

Referenced by [Timer\\_A\\_getEnabledInterruptStatus\(\)](#).

24.4.2.18 uint\_fast8\_t Timer\_A\_getOutputForOutputModeOutBitValue ( uint32\_t *timer*, uint\_fast16\_t *captureCompareRegister* )

Get output bit for output mode

## Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>captureCompareRegister</i>	selects the Capture register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used

## Returns

**TIMER\_A\_OUTPUTMODE\_OUTBITVALUE\_HIGH** or  
 ■ **TIMER\_A\_OUTPUTMODE\_OUTBITVALUE\_LOW**

24.4.2.19 `uint_fast8_t Timer_A_getSynchronizedCaptureCompareInput ( uint32_t timer, uint_fast16_t captureCompareRegister, uint_fast16_t synchronizedSetting )`

Get synchronized capture compare input

## Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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<i>captureCompareRegister</i>	selects the Capture register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used
<i>synchronized-Setting</i>	is to select type of capture compare input. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_READ_CAPTURE_COMPARE_INPUT</b></li> <li>■ <b>TIMER_A_READ_SYNCHRONIZED_CAPTURECOMPAREINPUT</b></li> </ul>

**Returns**

**TIMER\_A\_CAPTURECOMPARE\_INPUT\_HIGH** or  
 ■ **TIMER\_A\_CAPTURECOMPARE\_INPUT\_LOW**

24.4.2.20 void Timer\_A\_initCapture ( uint32\_t *timer*, const **Timer\_A\_CaptureModeConfig** \* *config* )

Initializes Capture Mode

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for Timer_A capture mode

**Configuration options for Timer\_A\_CaptureModeConfig structure.**

## Parameters

<i>captureRegister</i>	<p>selects the Capture register being used. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> <p>Refer to datasheet to ensure the device has the capture compare register being used</p>
<i>captureMode</i>	<p>is the capture mode selected. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTUREMODE_NO_CAPTURE</b> [Default value]</li> <li>■ <b>TIMER_A_CAPTUREMODE_RISING_EDGE</b></li> <li>■ <b>TIMER_A_CAPTUREMODE_FALLING_EDGE</b></li> <li>■ <b>TIMER_A_CAPTUREMODE_RISING_AND_FALLING_EDGE</b></li> </ul>
<i>captureInputSelect</i>	<p>decides the Input Select</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURE_INPUTSELECT_CC1xA</b> [Default value]</li> <li>■ <b>TIMER_A_CAPTURE_INPUTSELECT_CC1xB</b></li> <li>■ <b>TIMER_A_CAPTURE_INPUTSELECT_GND</b></li> <li>■ <b>TIMER_A_CAPTURE_INPUTSELECT_Vcc</b></li> </ul>
<i>synchronize-CaptureSource</i>	<p>decides if capture source should be synchronized with timer clock Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURE_ASYNCHRONOUS</b> [Default value]</li> <li>■ <b>TIMER_A_CAPTURE_SYNCHRONOUS</b></li> </ul>
<i>captureInterruptEnable</i>	<p>is to enable or disable timer captureCompare interrupt. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_INTERRUPT_DISABLE</b> [Default value]</li> <li>■ <b>TIMER_A_CAPTURECOMPARE_INTERRUPT_ENABLE</b></li> </ul>
<i>captureOutputMode</i>	<p>specifies the output mode. Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>TIMER_A_OUTPUTMODE_OUTBITVALUE</b> [Default value],</li> <li>■ <b>TIMER_A_OUTPUTMODE_SET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_RESET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_SET_RESET</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_SET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET_SET</b></li> </ul>

**Returns**  
None

24.4.2.21 void Timer\_A\_initCompare ( uint32\_t *timer*, const **Timer\_A\_CompareModeConfig** \* *config* )

Initializes Compare Mode

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for Timer_A compare mode

**Configuration options for Timer\_A\_CompareModeConfig structure.**

**Parameters**

<i>compareRegister</i>	selects the Capture register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used
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<i>compareInterruptEnable</i>	is to enable or disable timer capture compare interrupt. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_INTERRUPT_ENABLE</b> and</li> <li>■ <b>TIMER_A_CAPTURECOMPARE_INTERRUPT_DISABLE</b> [Default value]</li> </ul>
<i>compareOutputMode</i>	specifies the output mode. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_OUTPUTMODE_OUTBITVALUE</b> [Default value],</li> <li>■ <b>TIMER_A_OUTPUTMODE_SET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_RESET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_SET_RESET</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_TOGGLE_SET</b>,</li> <li>■ <b>TIMER_A_OUTPUTMODE_RESET_SET</b></li> </ul>
<i>compareValue</i>	is the count to be compared with in compare mode

**Returns**

None

24.4.2.22 void Timer\_A\_registerInterrupt ( uint32\_t *timer*, uint\_fast8\_t *interruptSelect*, void(\*) (void) *intHandler* )

Registers an interrupt handler for the timer capture compare interrupt.

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
--------------	---

<i>interruptSelect</i>	Selects which timer interrupt handler to register. For the timer module, there are two separate interrupt handlers that can be registered: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CCR0_INTERRUPT</b> Corresponds to the interrupt for CCR0</li> <li>■ <b>TIMER_A_CCRX_AND_OVERFLOW_INTERRUPT</b> Corresponds to the interrupt for CCR1-6, as well as the overflow interrupt.</li> </ul>
<i>intHandler</i>	is a pointer to the function to be called when the timer capture compare interrupt occurs.

This function registers the handler to be called when a timer interrupt occurs. This function enables the global interrupt in the interrupt controller; specific Timer\_A interrupts must be enabled via [Timer\\_A\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [Timer\\_A\\_clearCaptureCompareInterrupt\(\)](#).

#### Returns

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

#### 24.4.2.23 void Timer\_A\_setCompareValue ( uint32\_t timer, uint\_fast16\_t compareRegister, uint\_fast16\_t compareValue )

Sets the value of the capture-compare register

#### Parameters

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>compareRegister</i>	selects the Capture register being used. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used



<i>compareValue</i>	is the count to be compared with in compare mode
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**Returns**

None

24.4.2.24 void Timer\_A\_setOutputForOutputModeOutBitValue ( uint32\_t *timer*,  
uint\_fast16\_t *captureCompareRegister*, uint\_fast8\_t *outputModeOutBitValue* )

Set output bit for output mode

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>captureCompareRegister</i>	selects the Capture register being used. are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_0</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_1</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_2</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_3</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_4</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_5</b></li> <li>■ <b>TIMER_A_CAPTURECOMPARE_REGISTER_6</b></li> </ul> Refer to datasheet to ensure the device has the capture compare register being used

<i>outputModeOut- BitValue</i>	the value to be set for out bit. Valid values are: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_OUTPUTMODE_OUTBITVALUE_HIGH</b></li> <li>■ <b>TIMER_A_OUTPUTMODE_OUTBITVALUE_LOW</b></li> </ul>
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**Returns**  
None

24.4.2.25 void Timer\_A\_startCounter ( uint32\_t *timer*, uint\_fast16\_t *timerMode* )

Starts Timer\_A counter

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>timerMode</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CONTINUOUS_MODE</b> [Default value]</li> <li>■ <b>TIMER_A_UPDOWN_MODE</b></li> <li>■ <b>TIMER_A_UP_MODE</b></li> </ul>

**Note**

This function assumes that the timer has been previously configured using Timer\_A\_configureContinuousMode, Timer\_A\_configureUpMode or Timer\_A\_configureUpDownMode.

**Returns**

None

24.4.2.26 void Timer\_A\_stopTimer ( uint32\_t *timer* )

Stops the timer

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
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**Returns**

None

24.4.2.27 void Timer\_A\_unregisterInterrupt ( uint32\_t *timer*, uint\_fast8\_t *interruptSelect* )

Unregisters the interrupt handler for the timer

**Parameters**

<i>timer</i>	is the instance of the Timer_A module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>TIMER_A0_BASE</b></li> <li>■ <b>TIMER_A1_BASE</b></li> <li>■ <b>TIMER_A2_BASE</b></li> <li>■ <b>TIMER_A3_BASE</b></li> </ul>
<i>interruptSelect</i>	Selects which timer interrupt handler to register. For the timer module, there are two separate interrupt handlers that can be registered: <ul style="list-style-type: none"> <li>■ <b>TIMER_A_CCR0_INTERRUPT</b> Corresponds to the interrupt for CCR0</li> <li>■ <b>TIMER_A_CCRX_AND_OVERFLOW_INTERRUPT</b> Corresponds to the interrupt for CCR1-6, as well as the overflow interrupt.</li> </ul>

This function unregisters the handler to be called when timer interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

# 25 Universal Asynchronous Receiver/Transmitter (UART)

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## 25.1 Module Operation

The MSPWare library for UART mode features include:

- Odd, even, or non-parity
- Independent transmit and receive shift registers
- Separate transmit and receive buffer registers
- LSB-first or MSB-first data transmit and receive
- Built-in idle-line and address-bit communication protocols for multiprocessor systems
- Status flags for error detection and suppression
- Status flags for address detection
- Independent interrupt capability for receive and transmit

The modes of operations supported by the UART and the library include

- UART mode
- Idle-line multiprocessor mode
- Address-bit multiprocessor mode
- UART mode with automatic baud-rate detection

In UART mode, the USCI transmits and receives characters at a bit rate asynchronous to another device. Timing for each character is based on the selected baud rate of the USCI. The transmit and receive functions use the same baud-rate frequency.

## 25.2 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the UART module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure and enable the UART module. In the case of this example, we assume the MCLK is operating off of the DCO and the DCO is tuned to 12MHz. This makes the configuration parameters so that the baud rate is 9600.

Below is an example of the UART configuration parameter:

```

/* UART Configuration Parameter. These are the configuration parameters to
 * make the eUSCI A UART module to operate with a 9600 baud rate. These
 * values were calculated using the online calculator that TI provides
 * at:
 *http://software-dl.ti.com/msp430/msp430_public_sw/mcu/msp430/MSP430BaudRateConverter/index.html
 */
const eUSCI_UART_Config uartConfig =
{
    EUSCI_A_UART_CLOCKSOURCE_SMCLK,           // SMCLK Clock Source
    78,                                       // BRDIV = 78
    2,                                       // UCxBRF = 2
    0,                                       // UCxBRS = 0
    EUSCI_A_UART_NO_PARITY,                 // No Parity
    EUSCI_A_UART_LSB_FIRST,                 // LSB First
    EUSCI_A_UART_ONE_STOP_BIT,              // One stop bit
    EUSCI_A_UART_MODE,                       // UART mode
    EUSCI_A_UART_OVERSAMPLING_BAUDRATE_GENERATION // Oversampling
};

```

This code snippet is the actual configuration of the UART module using the DriverLib APIs:

```

/* Configuring UART Module */
MAP_UART_initModule(EUSCI_A0_BASE, &uartConfig);

/* Enable UART module */
MAP_UART_enableModule(EUSCI_A0_BASE);

/* Enabling interrupts */
MAP_UART_enableInterrupt(EUSCI_A0_BASE, EUSCI_A_UART_RECEIVE_INTERRUPT);
MAP_Interrupt_enableInterrupt(INT_EUSCIA0);
MAP_Interrupt_enableSleepOnIsrExit();
MAP_Interrupt_enableMaster();

```

## 25.3 Definitions

### Data Structures

- struct `_eUSCI_eUSCI_UART_Config`

### Functions

- void `UART_clearInterruptFlag` (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void `UART_disableInterrupt` (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void `UART_disableModule` (uint32\_t moduleInstance)
- void `UART_enableInterrupt` (uint32\_t moduleInstance, uint\_fast8\_t mask)
- void `UART_enableModule` (uint32\_t moduleInstance)
- uint\_fast8\_t `UART_getEnabledInterruptStatus` (uint32\_t moduleInstance)
- uint\_fast8\_t `UART_getInterruptStatus` (uint32\_t moduleInstance, uint8\_t mask)
- uint32\_t `UART_getReceiveBufferAddressForDMA` (uint32\_t moduleInstance)
- uint32\_t `UART_getTransmitBufferAddressForDMA` (uint32\_t moduleInstance)
- bool `UART_initModule` (uint32\_t moduleInstance, const `eUSCI_UART_Config` \*config)
- uint\_fast8\_t `UART_queryStatusFlags` (uint32\_t moduleInstance, uint\_fast8\_t mask)
- uint8\_t `UART_receiveData` (uint32\_t moduleInstance)
- void `UART_registerInterrupt` (uint32\_t moduleInstance, void(\*intHandler)(void))
- void `UART_resetDormant` (uint32\_t moduleInstance)
- void `UART_selectDeglitchTime` (uint32\_t moduleInstance, uint32\_t deglitchTime)
- void `UART_setDormant` (uint32\_t moduleInstance)
- void `UART_transmitAddress` (uint32\_t moduleInstance, uint\_fast8\_t transmitAddress)
- void `UART_transmitBreak` (uint32\_t moduleInstance)
- void `UART_transmitData` (uint32\_t moduleInstance, uint\_fast8\_t transmitData)
- void `UART_unregisterInterrupt` (uint32\_t moduleInstance)

### 25.3.1 Detailed Description

The code for this module is contained in `uart/adc14.c`, with `driverlib/uart.h` containing the API declarations for use by applications.

## 25.3.2 Function Documentation

### 25.3.2.1 void UART\_clearInterruptFlag ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Clears UART interrupt sources.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>mask</i>	is a bit mask of the interrupt sources to be cleared.

The UART interrupt source is cleared, so that it no longer asserts. The highest interrupt flag is automatically cleared when an interrupt vector generator is used.

The mask parameter has the same definition as the mask parameter to EUSCI\_A\_UART\_enableInterrupt().

Modified register is **UCAxIFG**

#### Returns

None.

### 25.3.2.2 void UART\_disableInterrupt ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Disables individual UART interrupt sources.

#### Parameters

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	--



<i>mask</i>	is the bit mask of the interrupt sources to be disabled.
-------------	--

Disables the indicated UART interrupt sources. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_A\_UART\_RECEIVE\_INTERRUPT** -Receive interrupt
- **EUSCI\_A\_UART\_TRANSMIT\_INTERRUPT** - Transmit interrupt
- **EUSCI\_A\_UART\_RECEIVE\_ERRONEOUSCHAR\_INTERRUPT** - Receive erroneous-character interrupt enable
- **EUSCI\_A\_UART\_BREAKCHAR\_INTERRUPT** - Receive break character interrupt enable

Modified register is **UCAxIFG**, **UCAxIE** and **UCAxCTL1**

**Returns**

None.

25.3.2.3 void UART\_disableModule ( uint32\_t *moduleInstance* )

Disables the UART block.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	--

This will disable operation of the UART block.

Modified register is **UCAxCTL1**

**Returns**

None.

25.3.2.4 void UART\_enableInterrupt ( uint32\_t *moduleInstance*, uint\_fast8\_t *mask* )

Enables individual UART interrupt sources.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>mask</i>	is the bit mask of the interrupt sources to be enabled.

Enables the indicated UART interrupt sources. The interrupt flag is first and then the corresponding interrupt is enabled. Only the sources that are enabled can be reflected to the processor interrupt; disabled sources have no effect on the processor.

The mask parameter is the logical OR of any of the following:

- **EUSCI\_A\_UART\_RECEIVE\_INTERRUPT** -Receive interrupt
- **EUSCI\_A\_UART\_TRANSMIT\_INTERRUPT** - Transmit interrupt
- **EUSCI\_A\_UART\_RECEIVE\_ERRONEOUSCHAR\_INTERRUPT** - Receive erroneous-character interrupt enable
- **EUSCI\_A\_UART\_BREAKCHAR\_INTERRUPT** - Receive break character interrupt enable

Modified register is **UCAxIFG**, **UCAxIE** and **UCAxCTL1**

**Returns**

None.

25.3.2.5 void UART\_enableModule ( uint32\_t *moduleInstance* )

Enables the UART block.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	--

This will enable operation of the UART block.

Modified register is **UCAxCTL1**

**Returns**

None.

### 25.3.2.6 uint\_fast8\_t UART\_getEnabledInterruptStatus ( uint32\_t moduleInstance )

Gets the current UART interrupt status masked with the enabled interrupts. This function is useful to call in ISRs to get a list of pending interrupts that are actually enabled and could have caused the ISR.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	---

**Returns**

The current interrupt status as an ORed bit mask:

- EUSCI\_A\_UART\_RECEIVE\_INTERRUPT\_FLAG -Receive interrupt flag
- EUSCI\_A\_UART\_TRANSMIT\_INTERRUPT\_FLAG - Transmit interrupt flag

References [UART\\_getInterruptStatus\(\)](#).

### 25.3.2.7 uint\_fast8\_t UART\_getInterruptStatus ( uint32\_t moduleInstance, uint8\_t mask )

Gets the current UART interrupt status.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>mask</i>	<p>is the masked interrupt flag status to be returned. Mask value is the logical OR of any of the following:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A_UART_RECEIVE_INTERRUPT_FLAG</li> <li>■ EUSCI_A_UART_TRANSMIT_INTERRUPT_FLAG</li> <li>■ EUSCI_A_UART_STARTBIT_INTERRUPT_FLAG</li> <li>■ EUSCI_A_UART_TRANSMIT_COMPLETE_INTERRUPT_FLAG</li> </ul>

**Returns**

The current interrupt status as an ORed bit mask:

- **EUSCI\_A\_UART\_RECEIVE\_INTERRUPT\_FLAG** -Receive interrupt flag
- **EUSCI\_A\_UART\_TRANSMIT\_INTERRUPT\_FLAG** - Transmit interrupt flag

Referenced by [UART\\_getEnabledInterruptStatus\(\)](#).

25.3.2.8 uint32\_t UART\_getReceiveBufferAddressForDMA ( uint32\_t *moduleInstance* )

Returns the address of the RX Buffer of the UART for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	---

Returns the address of the UART RX Buffer. This can be used in conjunction with the DMA to store the received data directly to memory.

**Returns**

None

25.3.2.9 uint32\_t UART\_getTransmitBufferAddressForDMA ( uint32\_t *moduleInstance* )

Returns the address of the TX Buffer of the UART for the DMA module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	---

Returns the address of the UART TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Returns**

None

25.3.2.10 `bool UART_initModule ( uint32_t moduleInstance, const eUSCI_UART_Config * config )`

Initialization routine for the UART block. The values to be written into the UCxBRW and UCxMCTLW registers should be pre-computed and passed into the initialization function

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul>
<i>config</i>	Configuration structure for the UART module

**Configuration options for eUSCI\_UART\_Config structure.**

It is important to note that for eUSCI modules, only "A" modules such as EUSCI\_A0 can be used. "B" modules such as EUSCI\_B0 do not support the UART mode.

**Parameters**

<i>selectClock-Source</i>	selects Clock source. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_A_UART_CLOCKSOURCE_SMCLK</b></li> <li>■ <b>EUSCI_A_UART_CLOCKSOURCE_ACLK</b></li> </ul>
<i>clockPrescalar</i>	is the value to be written into UCBRx bits
<i>firstModReg</i>	is First modulation stage register setting. This value is a pre-calculated value which can be obtained from the Device User Guide. This value is written into UCBRFx bits of UCxMCTLW.
<i>secondModReg</i>	is Second modulation stage register setting. This value is a pre-calculated value which can be obtained from the Device User Guide. This value is written into UCBRx bits of UCxMCTLW.
<i>parity</i>	is the desired parity. Valid values are <ul style="list-style-type: none"> <li>■ <b>EUSCI_A_UART_NO_PARITY</b> [Default Value],</li> <li>■ <b>EUSCI_A_UART_ODD_PARITY</b>,</li> <li>■ <b>EUSCI_A_UART_EVEN_PARITY</b></li> </ul>

<i>msborLsbFirst</i>	controls direction of receive and transmit shift register. Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_A_UART_MSB_FIRST</li> <li>■ EUSCI_A_UART_LSB_FIRST [Default Value]</li> </ul>
<i>numberOfStop-Bits</i>	indicates one/two STOP bits Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_A_UART_ONE_STOP_BIT [Default Value]</li> <li>■ EUSCI_A_UART_TWO_STOP_BITS</li> </ul>
<i>uartMode</i>	selects the mode of operation Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_A_UART_MODE [Default Value],</li> <li>■ EUSCI_A_UART_IDLE_LINE_MULTI_PROCESSOR_MODE,</li> <li>■ EUSCI_A_UART_ADDRESS_BIT_MULTI_PROCESSOR_MODE,</li> <li>■ EUSCI_A_UART_AUTOMATIC_BAUDRATE_DETECTION_MODE</li> </ul>
<i>overSampling</i>	indicates low frequency or oversampling baud generation Valid values are <ul style="list-style-type: none"> <li>■ EUSCI_A_UART_OVERSAMPLING_BAUDRATE_GENERATION</li> <li>■ EUSCI_A_UART_LOW_FREQUENCY_BAUDRATE_GENERATION</li> </ul>

Upon successful initialization of the UART block, this function will have initialized the module, but the UART block still remains disabled and must be enabled with [UART\\_enableModule\(\)](#)

Refer to [this calculator](#) for help on calculating values for the parameters.

Modified bits are **UCPEN**, **UCPAR**, **UCMSB**, **UC7BIT**, **UCSPB**, **UCMODEx**, **UCSYNC** bits of **UCAxCTL0** and **UCSSELx**, **UCSWRST** bits of **UCAxCTL1**

**Returns**

true or STATUS\_FAIL of the initialization process

25.3.2.11 `uint_fast8_t UART_queryStatusFlags ( uint32_t moduleInstance, uint_fast8_t mask )`

Gets the current UART status flags.

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>mask</i>	is the masked interrupt flag status to be returned.

This returns the status for the UART module based on which flag is passed. mask parameter can

be either any of the following selection.

- EUSCI\_A\_UART\_LISTEN\_ENABLE
- EUSCI\_A\_UART\_FRAMING\_ERROR
- EUSCI\_A\_UART\_OVERRUN\_ERROR
- EUSCI\_A\_UART\_PARITY\_ERROR
- eUARTBREAK\_DETECT
- EUSCI\_A\_UART\_RECEIVE\_ERROR
- EUSCI\_A\_UART\_ADDRESS\_RECEIVED
- EUSCI\_A\_UART\_IDLELINE
- EUSCI\_A\_UART\_BUSY

Modified register is **UCAxSTAT**

**Returns**

the masked status flag

25.3.2.12 `uint8_t UART_receiveData ( uint32_t moduleInstance )`

Receives a byte that has been sent to the UART Module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ EUSCI_A0_BASE</li> <li>■ EUSCI_A1_BASE</li> <li>■ EUSCI_A2_BASE</li> <li>■ EUSCI_A3_BASE</li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	---

This function reads a byte of data from the UART receive data Register.

Modified register is **UCAxRXBUF**

**Returns**

Returns the byte received from by the UART module, cast as an `uint8_t`.

25.3.2.13 `void UART_registerInterrupt ( uint32_t moduleInstance, void(*)(void) intHandler )`

Registers an interrupt handler for UART interrupts.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode.</p>
<i>intHandler</i>	is a pointer to the function to be called when the timer capture compare interrupt occurs.

This function registers the handler to be called when an UART interrupt occurs. This function enables the global interrupt in the interrupt controller; specific UART interrupts must be enabled via [UART\\_enableInterrupt\(\)](#). It is the interrupt handler's responsibility to clear the interrupt source via [UART\\_clearInterruptFlag\(\)](#).

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).

**25.3.2.14 void UART\_resetDormant ( uint32\_t moduleInstance )**

Re-enables UART module from dormant mode

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
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Not dormant. All received characters set UCRXIFG.

Modified bits are **UCDORM** of **UCAxCTL1** register.

**Returns**

None.

**25.3.2.15 void UART\_selectDeglitchTime ( uint32\_t moduleInstance, uint32\_t deglitchTime )**

Sets the deglitch time



**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>deglitchTime</i>	<p>is the selected deglitch time Valid values are</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A_UART_DEGLITCH_TIME_2ns</b></li> <li>■ <b>EUSCI_A_UART_DEGLITCH_TIME_50ns</b></li> <li>■ <b>EUSCI_A_UART_DEGLITCH_TIME_100ns</b></li> <li>■ <b>EUSCI_A_UART_DEGLITCH_TIME_200ns</b></li> </ul>

Returns the address of the UART TX Buffer. This can be used in conjunction with the DMA to obtain transmitted data directly from memory.

**Returns**

None

25.3.2.16 void UART\_setDormant ( uint32\_t *moduleInstance* )

Sets the UART module in dormant mode

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
-----------------------	---

Puts USCI in sleep mode Only characters that are preceded by an idle-line or with address bit set UCRXIFG. In UART mode with automatic baud-rate detection, only the combination of a break and synch field sets UCRXIFG.

Modified register is **UCAxCTL1**

**Returns**

None.

25.3.2.17 void UART\_transmitAddress ( uint32\_t *moduleInstance*, uint\_fast8\_t *transmitAddress* )

Transmits the next byte to be transmitted marked as address depending on selected multiprocessor mode

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>transmitAddress</i>	is the next byte to be transmitted

Modified register is **UCAxCTL1, UCAxTXBUF**

**Returns**

None.

25.3.2.18 void UART\_transmitBreak ( uint32\_t *moduleInstance* )

Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud-rate detection, EUSCI\_A\_UART\_AUTOMATICBAUDRATE\_SYNC(0x55) must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise, DEFAULT\_SYNC(0x00) must be written into the transmit buffer. Also ensures module is ready for transmitting the next data

**Parameters**

<i>moduleInstance</i>	is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include: <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
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Modified register is **UCAxCTL1, UCAxTXBUF**

**Returns**

None.

25.3.2.19 void UART\_transmitData ( uint32\_t *moduleInstance*, uint\_fast8\_t *transmitData* )

Transmits a byte from the UART Module.

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode</p>
<i>transmitData</i>	data to be transmitted from the UART module

This function will place the supplied data into UART transmit data register to start transmission

Modified register is **UCAxTXBUF**

**Returns**

None.

25.3.2.20 void UART\_unregisterInterrupt ( uint32\_t *moduleInstance* )

Unregisters the interrupt handler for the UART module

**Parameters**

<i>moduleInstance</i>	<p>is the instance of the eUSCI A (UART) module. Valid parameters vary from part to part, but can include:</p> <ul style="list-style-type: none"> <li>■ <b>EUSCI_A0_BASE</b></li> <li>■ <b>EUSCI_A1_BASE</b></li> <li>■ <b>EUSCI_A2_BASE</b></li> <li>■ <b>EUSCI_A3_BASE</b></li> </ul> <p>It is important to note that for eUSCI modules, only "A" modules such as EUSCI_A0 can be used. "B" modules such as EUSCI_B0 do not support the UART mode.</p>
-----------------------	--

This function unregisters the handler to be called when timer interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

## 26 Watchdog Timer (WDT\_A)

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### 26.1 Module Operation

MSP432 includes a standard watchdog module that is identical to the WDT\_A module of MSP430. By using DriverLib, the user can configure all aspects of the watchdog peripheral including using the watchdog in interval mode as well as watchdog mode.

### 26.2 Watchdog Mode

Once the module is initiated in watchdog mode, the timer will reset part if the count expires. The reset can be set as either a soft or hard reset. This use case is useful when the programmer wants to make sure that the code execution isn't perpetually stuck/locked in an unrecoverable state.

To configure the WDT module in watchdog mode, the `WDT_initWatchdogTimer` function is used such as follows:

```
/* Configuring WDT to timeout after 512k iterations of SMCLK, at 128k,
 * this will roughly equal 4 seconds*/
MAP_SysCtl_setWDTTimeoutResetType(SYSCTL_SOFT_RESET);
MAP_WDT_A_initWatchdogTimer(WDT_A_CLOCKSOURCE_SMCLK,
                             WDT_A_CLOCKITERATIONS_512K);
```

This will set the watchdog timer to be sourced from SMCLK and have a duration of 512, 000 SMCLK cycles. This means that once started, if the watchdog timer goes 512, 000 iterations without being reset a reset will occur. To reset the counter (after using `WDT_startTimer` to start the timer), the user should use the `WDT_resetTimer` function.

### 26.3 Interval Mode

MSP432 Driverlib can also configure the WDT module to work in interval mode. This turns the WDT into an ordinary 16-bit down counter with interrupt support. This can be used if the user needs access to another low power counter, however has already used other resources. To configure the module in interval mode, use the `WDT_initIntervalTimer` function such as follows:

```
/* Configuring WDT in interval mode to trigger every 32K clock iterations.
 * This comes out to roughly every 3.5 seconds */
MAP_WDT_A_initIntervalTimer(WDT_A_CLOCKSOURCE_VLOCLK,
                             WDT_A_CLOCKITERATIONS_32K);
```

This will configure the WDT module to be sourced from SMCLK and have a period of 32,000 cycles. In this example, we have previously configured SMCLK to be 64KHz making this timer's period be approximately half a second. After using the WDT\_startTimer function to start the timer, the user can service interrupts from interval mode after enabling interrupts using the Interrupt\_enableInterrupt function.

## 26.4 Setting Reset Type

The type of reset that occurs on watchdog timeout/password violation can be configured through the SysCtl module using the SysCtl\_setWDTPasswordViolationResetType and SysCtl\_setWDTTimeoutResetType APIs. These APIs will allow the user to change whether a soft or hard reset occurs on a watchdog timeout and password violation. For the user, the convenience functions WDT\_setPasswordViolationReset and WDT\_setTimeoutReset exist in the WDT APIs.

## 26.5 Programming Example

The DriverLib package contains a variety of different code examples that demonstrate the usage of the WDT module. These code examples are accessible under the examples/ folder of the MSPWare release as well as through TI Resource Explorer if using Code Composer Studio. These code examples provide a comprehensive list of use cases as well as practical applications involving each module.

Below is a very brief code example showing how to configure the WDT module in interval mode:

```
/* Configuring WDT in interval mode to trigger every 32K clock iterations.
 * This comes out to roughly every 3.5 seconds */
MAP_WDT_A_initIntervalTimer(WDT_A_CLOCKSOURCE_VLOCLK,
                            WDT_A_CLOCKITERATIONS_32K);
```

## 26.6 Definitions

### Functions

- void [WDT\\_A\\_clearTimer](#) (void)
- void [WDT\\_A\\_holdTimer](#) (void)
- void [WDT\\_A\\_initIntervalTimer](#) (uint\_fast8\_t clockSelect, uint\_fast8\_t clockDivider)
- void [WDT\\_A\\_initWatchdogTimer](#) (uint\_fast8\_t clockSelect, uint\_fast8\_t clockDivider)
- void [WDT\\_A\\_registerInterrupt](#) (void(\*intHandler)(void))
- void [WDT\\_A\\_setPasswordViolationReset](#) (uint\_fast8\_t resetType)
- void [WDT\\_A\\_setTimeoutReset](#) (uint\_fast8\_t resetType)
- void [WDT\\_A\\_startTimer](#) (void)
- void [WDT\\_A\\_unregisterInterrupt](#) (void)

### 26.6.1 Detailed Description

The code for this module is contained in `driverlib/wdt.c`, with `driverlib/wdt.h` containing the API declarations for use by applications.



## 26.6.2 Function Documentation

### 26.6.2.1 void WDT\_A\_clearTimer ( void )

Clears the timer counter of the Watchdog Timer.

This function clears the watchdog timer count to 0x0000h. This function is used to "service the dog" when operating in watchdog mode.

**Returns**

None

### 26.6.2.2 void WDT\_A\_holdTimer ( void )

Holds the Watchdog Timer.

This function stops the watchdog timer from running. This way no interrupt or PUC is asserted.

**Returns**

None

Referenced by [PCM\\_gotoLPM4\(\)](#).

### 26.6.2.3 void WDT\_A\_initIntervalTimer ( uint\_fast8\_t *clockSelect*, uint\_fast8\_t *clockDivider* )

Sets the clock source for the Watchdog Timer in timer interval mode.

**Parameters**

<i>clockSelect</i>	is the clock source that the watchdog timer will use. Valid values are <ul style="list-style-type: none"> <li>■ <b>WDT_A_CLOCKSOURCE_SMCLK</b> [Default]</li> <li>■ <b>WDT_A_CLOCKSOURCE_ACLK</b></li> <li>■ <b>WDT_A_CLOCKSOURCE_VLOCLK</b></li> <li>■ <b>WDT_A_CLOCKSOURCE_BCLK</b></li> </ul>
<i>clockIterations</i>	is the number of clock iterations for a watchdog interval. Valid values are <ul style="list-style-type: none"> <li>■ <b>WDT_A_CLOCKITERATIONS_2G</b> [Default]</li> <li>■ <b>WDT_A_CLOCKITERATIONS_128M</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_8192K</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_512K</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_32K</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_8192</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_512</b></li> <li>■ <b>WDT_A_CLOCKITERATIONS_64</b></li> </ul>

This function sets the watchdog timer as timer interval mode, which will assert an interrupt without causing a PUC.

**Returns**

None

26.6.2.4 void WDT\_A\_initWatchdogTimer ( uint\_fast8\_t *clockSelect*, uint\_fast8\_t *clockDivider* )

Sets the clock source for the Watchdog Timer in watchdog mode.

**Parameters**

<i>clockSelect</i>	is the clock source that the watchdog timer will use. Valid values are <ul style="list-style-type: none"> <li>■ WDT_A_CLOCKSOURCE_SMCLK [Default]</li> <li>■ WDT_A_CLOCKSOURCE_ACLK</li> <li>■ WDT_A_CLOCKSOURCE_VLOCLK</li> <li>■ WDT_A_CLOCKSOURCE_BCLK</li> </ul>
<i>clockIterations</i>	is the number of clock iterations for a watchdog timeout. Valid values are <ul style="list-style-type: none"> <li>■ WDT_A_CLOCKITERATIONS_2G [Default]</li> <li>■ WDT_A_CLOCKITERATIONS_128M</li> <li>■ WDT_A_CLOCKITERATIONS_8192K</li> <li>■ WDT_A_CLOCKITERATIONS_512K</li> <li>■ WDT_A_CLOCKITERATIONS_32K</li> <li>■ WDT_A_CLOCKITERATIONS_8192</li> <li>■ WDT_A_CLOCKITERATIONS_512</li> <li>■ WDT_A_CLOCKITERATIONS_64</li> </ul>

This function sets the watchdog timer in watchdog mode, which will cause a PUC when the timer overflows. When in the mode, a PUC can be avoided with a call to WDT\_A\_resetTimer() before the timer runs out.

**Returns**

None

26.6.2.5 void WDT\_A\_registerInterrupt ( void(\*)(void) *intHandler* )

Registers an interrupt handler for the watchdog interrupt.

**Parameters**

<i>intHandler</i>	is a pointer to the function to be called when the watchdog interrupt occurs.
-------------------	---

**Returns**

None.

References [Interrupt\\_enableInterrupt\(\)](#), and [Interrupt\\_registerInterrupt\(\)](#).26.6.2.6 void WDT\_A\_setPasswordViolationReset ( uint\_fast8\_t *resetType* )

Sets the type of RESET that happens when a watchdog password violation occurs.

**Parameters**

<i>resetType</i>	The type of reset to set
------------------	--------------------------

The *resetType* parameter must be only one of the following values:

- WDT\_A\_HARD\_RESET
- WDT\_A\_SOFT\_RESET

**Returns**

None.

References [SysCtl\\_setWDTPasswordViolationResetType\(\)](#).26.6.2.7 void WDT\_A\_setTimeoutReset ( uint\_fast8\_t *resetType* )

Sets the type of RESET that happens when a watchdog timeout occurs.

**Parameters**

<i>resetType</i>	The type of reset to set
------------------	--------------------------

The *resetType* parameter must be only one of the following values:

- WDT\_A\_HARD\_RESET
- WDT\_A\_SOFT\_RESET

**Returns**

None.

References [SysCtl\\_setWDTTimeoutResetType\(\)](#).

## 26.6.2.8 void WDT\_A\_startTimer ( void )

Starts the Watchdog Timer.

This function starts the watchdog timer functionality to start counting.

**Returns**

None

### 26.6.2.9 void WDT\_A\_unregisterInterrupt ( void )

Unregisters the interrupt handler for the watchdog.

This function unregisters the handler to be called when a watchdog interrupt occurs. This function also masks off the interrupt in the interrupt controller so that the interrupt handler no longer is called.

**See Also**

[Interrupt\\_registerInterrupt\(\)](#) for important information about registering interrupt handlers.

**Returns**

None.

References [Interrupt\\_disableInterrupt\(\)](#), and [Interrupt\\_unregisterInterrupt\(\)](#).

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