CC2650 Size Benchmark

October 8, 2015

A benchmark application was created for CC26xx to allow a quick relative comparison of sizes between different kernel and driverlib releases. This application includes a representative set of SYS/BIOS kernel modules and API calls as used in a typical BLE application. This includes the Power module and its APIs. The application isn't intended to be functional - it includes several Power API calls for no purpose other than to have them linked into the application.

The total Flash and RAM sizes for recent releases are listed in tables below. In each case, the application is built to use SYS/BIOS in ROM, and uses the default tool optimizations of that release.

Note: The benchmark application was improved for the bios_6_42_03 release, with the following changes:

- **The application now uses the aggressive Standby power policy, versus a single explicit call to Power_sleep()**
- **Calls to Power_shutdown(), Power_getTransitionState(), and Power_getXoscStartupTime() are now included**
- **The SysCallback System provider is now used, to eliminate debugger I/O support**
- **System stack sizes are now equalized (previously the system stack for IAR was 2K, versus 1K for TI)**

The table immediately below shows the sizes for the new application and the new kernel and driverlib releases. The next table below that shows for comparison purposes the sizes using the new benchmark application, with the previous kernel and driverlib releases.

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bios_6_42_03_32 (Build date: October 5, 2015)
xdctools_3_31_01_33
cc26xxware_2_22_00_16101

	RCOSC Calibration	Flash	RAM
IAR	Disabled	13024	8331
	Enabled	14082	8387
TI	Disabled	15052	8375
	Enabled	16252	8431

Changes in this release known to affect size:
- Use the LF clock source to determine the startup delays for enabling the LF clock qualifiers (SDOCM00119402)
- Driverlib enhancements, including new functions for clock loss event control, and adding temperature compensation for VDDR sleep trim.

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bios_6_42_02_24 (Build date: August 4, 2015)
xdctools_3_31_01_33
cc26xxware_2_21_03_15980

	RCOSC Calibration	Flash	RAM
IAR	Disabled	12781	8331
	Enabled	13842	8387
TI	Disabled	14748	8375
	Enabled	15952	8431

Note: The following tables show earlier comparisons, using the earlier size benchmark application, with earlier kernel and driverlib releases.

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bios_6_42_02_24 (Build date: August 4, 2015)
xdctools_3_31_01_33
cc26xxware_2_21_03_15980

	RCOSC Calibration	Flash	RAM
IAR	Disabled	13287	8123
	Enabled	14352	8179
TI	Disabled	17254	7667
	Enabled	18458	7723

Changes in this release known to affect size:
- No longer use Clock_stop() from ROM; use new enhanced function that can trigger immediate reschedule of next tick (SDOCM00117544)
- Support VIMS RAM as GPRAM (SDOCM00117547)

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bios_6_42_01_15 (Build date: June 19, 2015)
xdctools_3_31_01_33
cc26xxware_2_21_02_15830

	RCOSC Calibration	Flash	RAM
IAR	Disabled	13267	8091
	Enabled	14341	8147
TI	Disabled	17170	7635
	Enabled	18374	7691

Changes in this release known to affect size:
- Reworked RCOSC calibration to reduce interrupt latency (SDOCM00115902)
- Optimizations for cc26xx and cc13xx should favor size (SDOCM00116205)

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bios_6_42_00_07 (Build date: April 30, 2015)
xdctools_3_31_01_33
cc26xxware_2_21_01_15600

	RCOSC Calibration	Flash	RAM
IAR	Disabled	13520	8035
	Enabled	14418	8091
TI	Disabled	18098	7583
	Enabled	19474	7635

Changes in this release known to affect size:
- Removed PG1, PG2.0, and PG2.1 workarounds
- Removed backdoor recovery mechanism
- Eliminate all RSOSC calibration code when the feature is disabled

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bios_6_41_02_41 (Build date: February 9, 2015)
xdctools_3_30_06_67
cc26xxware_2_20_06_14829

	RCOSC Calibration	Flash	RAM
IAR	Disabled	14173	8063
	Enabled	15201	8087
TI	Disabled	18310	7611
	Enabled	19386	7635