

# **DSP/BIOS™ LINK**

## **OMAP2530 EVM**

### **LNK 187 USR**

**Version 1.65.00.03**

**JUL 12, 2010**

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## A. PLATFORM GUIDE



### 1 Purpose

DSP/BIOS™ LINK is foundation software for the inter-processor communication across the GPP-DSP boundary. It provides a generic API that abstracts the characteristics of the physical link connecting GPP and DSP from the applications. It eliminates the need for customers to develop such link from scratch and allows them to focus more on application development.

This document provides the users necessary information about usage of DSP/BIOS™ LINK on the OMAP 2530 platform.

This document corresponds to the engineering release Version 1.65.00.03 dated JUL 12, 2010.

### 2 TextConventions

	This bullet indicates important information. Please read such text carefully.
	This bullet indicates additional information.
[ arg1   arg2 ]	In context of the commands, contents enclosed in square brackets are the optional arguments to the command. Different values of these arguments are separated by " ".

### 3 Terms&Abbreviations

CCS	Code Composer Studio
IPC	Inter Processor Communication
GPP	General Purpose e.g. ARM
DSP	Digital Signal Processor e.g. TMS320C5510
CGTools	Code Gen Tools, e.g. Compiler, Linker, Archiver

### 4 References

1.	User Guide	DSP/BIOS™ LINK user guide
2.	InstallGuide_<OS>_O MAP2530.doc	Installation guide for relevant OS if present.
3.	Porting Guide	Porting guide for relevant OS if present.

### 5 ConfiguringCCS

#### 5.1 OMAP2530

To use CCS for debugging the DSP side application, you will need to configure CCS to use both ARM and DSP with the OMAP2530.

- ❑ *CCS can attach to only ARM in the beginning. It can attach to the DSP only after the ARM-side application releases it from reset through a call to `PROC_Start ()`.*

## 6 Platformspecificinformation

### 6.1 Workingontargetplatform

#### 6.1.1 ConfiguringKernelParameters

DSP/BIOS™ LINK requires a few specific arguments to be passed to the Linux kernel during boot up. 2MB of memory is used by DSP/BIOS™ LINK for communication between GPP and DSP, and for DSP external memory. This must be reserved by specifying 2MB less as available for the Linux kernel for its usage.

#### 6.1.2 ConfiguringDynamicentries

Following are the assumptions for Dynamic entries:-

- The hardware provides a shared memory area, to which both the GPP and the DSP have access.
- The following page sizes are supported:
  - Super section: 16M bytes
  - Section : 1M bytes
  - Large page : 64K bytes
  - Small page : 4K bytes

Following are the constraints:-

Any memory overlap cases will treat as error case.

For optimization of TLB entries please make sure

- Requested entries should be continuous.
- Requested entries should be aligned with 16M or 1M or 64K or 4K.

#### API Usage:-

If DSP access an area whose mapping is not present in the TLB, then DSP's MMU generates an interrupt of PAGE fault type. This interrupt is generated on ARM (HOST). This happens only in case when table walking logic is disabled. Otherwise, if it is enabled, MMU checks with tables present in the memory.

To map some area into the DSP's address space, user can call `PROC_control` API with respective commands from GPI side. Below shows a usage scenario of mapping an area into DSP's address space.

#### Add the MMU entry:

```
MemMapInfo * mapInfo ;

mapInfo.dspAddr = DSP_ADDR1 ;
mapInfo.size    = 0x80000 ;

status = PROC_control (ID_PROCESSOR,
                      PROC_CTRL_CMD_MMU_ADD_ENTRY,
                      &mapInfo) ;
```

Here `PROC_CTRL_CMD_MMU_ADD_ENTRY` is an enumerated type, directing GPP side logic to add user given entries to the DSP's TLB. Now, User may want to write some

information on the area, to be given to DSP. For this user has to map the area into GPP user/kernel address space. For this below example is useful:

```
MemMapInfo * mapInfo ;

mapInfo.dspAddr = DSP_ADDR1 ;
mapInfo.size     = 0x80000 ;

status = PROC_control (ID_PROCESSOR,
                      PROC_CTRL_CMD_MAP_DSPMEM,
                      &mapInfo);
```

Once the user has done with his/her protocol, he/she may want to unmap the area from GPP and DSP address space as well. Below code how to achieve this:

**Delete the MMU entry:**

```
MemUnmapInfo * mapInfo ;

mapInfo.dspAddr = DSP_ADDR1 ;
mapInfo.size     = 0x80000 ;

status = PROC_control (ID_PROCESSOR,
                      PROC_CTRL_CMD_UNMAP_DSPMEM,
                      &mapInfo);
status = PROC_control (ID_PROCESSOR,
                      PROC_CTRL_CMD_MMU_DEL_ENTRY,
                      &mapInfo);
```

- ☐ Given size should be same to add and delete the dynamic entry.
- ☐ Can not remove a static entry dynamically.
- ☐ Given memory area to create a dynamic entry should be physically contiguous.

## 6.2 DSPMemoryManagementUnit(MMU)Configuration

The DSP on the OMAP2530 has a MMU for accessing L3 interconnect address space (addresses above 0x11000000). DSP/BIOS™ Link automatically configures and enables the MMU. The translation from virtual to physical is a straight thru (i.e. physical address == virtual address). With the MMU enabled, many invalid memory accesses (e.g. garbage pointer) can be detected. Also, the GPP memory is protected from DSP corruption.

### 6.2.1 Configuration

The memory regions that are added to the MMU configuration are determined by the `LINKCFG_MemEntry` array supplied by the application. All entries in this array are added into the DSP's MMU configuration. If the DSP accesses memory via the L3 interconnect and that memory is not in the configuration in the MMU, a MMU fault occurs and the GPP is notified. Refer the `LINKCFG_memTable_00` array in `${DSPLINK}/config/all/CFG_OMAP_2530.c` for the default configuration.

DSP/BIOS™ Link configures the MMU by locking entries into the Translation Look-aside Buffers (TLBs). There are 32 TLB entries, but only 31 can be locked. Each TLB entry can be used to map a 4KB, 64KB, 1MB or 16MB contiguous memory region. DSP/BIOS™ Link does not currently generate a separate translation table.



During initialization, DSP/BIOS™ Link scans the `LINKCFG_MemEntry` array and adds TLB entries. If the `LINKCFG_MemEntry` array has entries that have adjacent memory region, DSP/BIOS™ Link treats the adjacent regions as one larger region. Note this is possible because the translation is 1 to 1 (e.g. virtual address 0x83E00000 -> physical address 0x83E00000). Combining regions reduces the number of TLB entries used.

Since each TLB entry can only manage a 4KB, 64KB, 1MB, or 16MB memory region, the entries in the `LINKCFG_MemEntry` array must be a multiple of 4KB or entries with adjacent memory must add up to a multiple of 4KB. For example, the following is allowed because the two regions defined by the two entries are contiguous and the total size is 1MB (0xFFF80 + 0x80) which is a multiple of 4KB.

```
#define RSTENTRYID          0u
#define RESETCTRLADDR      0x83E00000u
#define RESETCTRLSIZE      0x80u

#define CODEENTRYID        1u
#define CODEMEMORYADDR     (RESETCTRLADDR + RESETCTRLSIZE)
#define CODEMEMORYSIZE     0xFFF80u
{
    RSTENTRYID,           /* ENTRY      : Entry number */
    "RESETCTRL",          /* NAME       : Name of the memory region */
    RESETCTRLADDR,        /* ADDRPHYS   : Physical address */
    RESETCTRLADDR,        /* ADDRDSPVIRT : DSP virtual address */
    (Uint32) -1u,         /* ADDRGPVIRT : GPP virtual address */
    RESETCTRLSIZE,        /* SIZE       : Size of the memory region */
    TRUE,                 /* SHARED     : Shared access memory? */
    FALSE,                /* SYNCD      : Synchornized? */
},
{
    CODEENTRYID,          /* ENTRY      : Entry number */
    "DDR2",               /* NAME       : Name of the memory region */
    CODEMEMORYADDR,        /* ADDRPHYS   : Physical address */
    CODEMEMORYADDR,        /* ADDRDSPVIRT : DSP virtual address */
    (Uint32) -1u,         /* ADDRGPVIRT : GPP virtual address */
    CODEMEMORYSIZE,        /* SIZE       : Size of the memory region */
    TRUE,                 /* SHARED     : Shared access memory? */
    FALSE,                /* SYNCD      : Synchornized? */
},
},
```

While the following is not allowed because the `RESETCTRL` entry's size is not a multiple of 4KB and its address is not adjacent to a region that would make its size a multiple of 4KB. This would result in a runtime configuration error (see section 6.2.2 for more details).

```
#define RSTENTRYID          0u
#define RESETCTRLADDR      0x83E00000u
#define RESETCTRLSIZE      0x80u

#define CODEENTRYID        1u
#define CODEMEMORYADDR     (RESETCTRLADDR + RESETCTRLSIZE + 0x20u)
#define CODEMEMORYSIZE     0xFFF80u
{
    RSTENTRYID,           /* ENTRY      : Entry number */
    "RESETCTRL",          /* NAME       : Name of the memory region */
    RESETCTRLADDR,        /* ADDRPHYS   : Physical address */
    RESETCTRLADDR,        /* ADDRDSPVIRT : DSP virtual address */
    (Uint32) -1u,         /* ADDRGPVIRT : GPP virtual address */
    RESETCTRLSIZE,        /* SIZE       : Size of the memory region */
    TRUE,                 /* SHARED     : Shared access memory? */
    FALSE,                /* SYNCD      : Synchornized? */
},
{
    CODEENTRYID,          /* ENTRY      : Entry number */
    "DDR2",               /* NAME       : Name of the memory region */
    CODEMEMORYADDR,        /* ADDRPHYS   : Physical address */
    CODEMEMORYADDR,        /* ADDRDSPVIRT : DSP virtual address */
    (Uint32) -1u,         /* ADDRGPVIRT : GPP virtual address */
    CODEMEMORYSIZE,        /* SIZE       : Size of the memory region */
    TRUE,                 /* SHARED     : Shared access memory? */
    FALSE,                /* SYNCD      : Synchornized? */
},
},
```

```

        RESETCTRLSIZE, /* SIZE           : Size of the memory region */
        TRUE,          /* SHARED        : Shared access memory? */
        FALSE,         /* SYNC          : Synchronizing? */
    },
    {
        CODEENTRYID,    /* ENTRY         : Entry number */
        "DDR2",         /* NAME          : Name of the memory region */
        CODEMEMORYADDR, /* ADDRPHYS      : Physical address */
        CODEMEMORYADDR, /* ADDRDSPVIRT   : DSP virtual address */
        (UInt32) -1u,   /* ADDRGGPVIRT   : GPP virtual address */
        CODEMEMORYSIZE, /* SIZE          : Size of the memory region */
        TRUE,          /* SHARED        : Shared access memory? */
        FALSE,         /* SYNC          : Synchronizing? */
    },
},

```

There are configurations that can use up all 31 of the TLB entries. For example, specifying a region of size 0xFF000 (1MB - 4KB), would result in 30 TLB entries (15 64KB entries and 15 4KB entries). While a 1MB region would result in one 1MB TLB entry. If more than 31 TLB entries are needed, a runtime configuration error is reported (see section 6.2.2 for more details). The memory region configuration must be changed to allow at most 31 TLB entries.

## 6.2.2 ConfigurationErrors

Two types of configuration errors may arise in regards to the MMU.

1. `LINKCFG_MemEntry` configuration requires too many TLB entries
2. A `LINKCFG_MemEntry` entry's size is not a multiple of 4KB (or if the entry's memory is adjacent to another entry's memory, the combined size is not a multiple of 4KB).

Both would result in a runtime configuration error (`DSP_ECONFIG`). Additional information is displayed to `stdio` also (e.g. "Configuration error: Exceeded maximum number [31] of Translation Look-aside Buffers.>").

## 6.3 DSP/BIOS™CLKManagerConfiguration

DSP/BIOS™ on the OMAP2530 uses Timer 5 by default. DSP/BIOS™ Link on the GPP must help in the management of this timer. Currently this management on the GPP is hard-coded to `GPTimer5` (done in `${DSPLINK}/gpp/src/ldrv/HAL/OMAP/2530/hal_prcm.c`), thus the DSP/BIOS™ CLK Manager Timer Selection must use Timer 5. Below is an example of the required DSP/BIOS™ CLK Manager configuration (which again is the default).

```

bios.CLK.TIMERSELECT = "Timer 5";

```