

TVP5158 RAM Code Release Notes

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1. Introduction

The TVP5158 has embedded video decoding firmware revision v02.00 in the device on-chip ROM. The TVP5158 device has a limited embedded RAM space which allows patch firmware code download possible. The patch can be used in improving decoder performance or fixing known decoder firmware bugs.

This document discusses the hardware and firmware issues related to the TVP5158 and fixes made by the patch v02.03.00. The discussions also include performance improvement made by the patch, the differences between the patch and the TVP5158 data manual.

2. Device & Firmware Affected

The information provided below is related only to the following device and firmware. Additional devices and firmware releases will have their own release notes.

Table 1. Device & Firmware Affected

Device	TVP5158
Firmware	v02.03.02
Patch Size	11,120 bytes
Data Manual	SLES243F.pdf

3. Device Related Issues

- The following are the known firmware issues in the TVP5158 ROM v2.00 device. Additional issues will be added to the list as they are discovered.
- Improved AGC response time
- Fixed pixel-interleaved mode.
- Added CTI gain and coring control - I²C address: 15h
- Fixed active video cropping issue - bit 6 of I²C address B1h
- Fixed Macrovision detection problem.
- Added OFM bypass enable for non-interleaved mode - bit 7 of I2C address B1h
- Changed manual HBLK control in 16-bit mode - I²C address B8h-B9h
- Fixed the output clock frequency control - bit 6 of I²C address B2h
- Modified automatic hblank duration algorithm
- Added host interrupt when input change to weak signal or signal present.
- Introduce vblank_stop1_offset_ram (address BEh) and vblank_stop2_offset_ram (address BFh)
 - vblank_stop1_offset_ram: 0Fh (default)
 - bit 0..3: NTSC vblank stop1 offset range -8..7
 - bit 4..7: PAL vblank stop1 offset range -8..7
 - vblank_stop2_offset_ram: 0Fh (default)
 - bit 0..3: NTSC vblank stop2 offset range -8..7
 - bit 4..7: PAL vblank stop2 offset range -8..7

Recommended settings for the DM6446 are F0h and 0Fh for vblank_stop1_offset_ram and vblank_stop2_offset_ram, respectively.
- Fix the INTR problem when 2nd intr set, the 1st get clear.
- Add intr open drain or intr driven bit 6 of I²C reg ADh.
- Enabled coarse clamp droop current control (I2C address BBh) to work in weak signal mode.

- Added new fine clamp mode that can be enabled by writing 0x02 to I²C register 0x98.
- Provide stable syncs when the video source is disconnected.
 - Bits 1:0 of I²C register 60h must always be set to 00b.
- Implemented new embedded V-bit control algorithm.
 - Supports two modes of operation selectable via bit 3 of I²C register 60h.
 - Original V-bit control mode (default): Maintains a fixed vertical blanking interval as the total number of lines per frame varies.
 - New V-bit control mode: Maintains a fixed number of active lines per frame as the total number of lines per frame varies. In this mode, the minimum F1_to_Active interval is programmable via I²C address D5h (default = 8 lines).
 - Fixed embedded sync offset control (I²C register: AEh).
 - Changed default for I²C register 88h from 00h to 03h. With this setting, the F/V-bit are always decoded from the line count.
 - Changed default for I²C register 8Bh from 64h to 60h.
 - Added V-PLL free run mode (Bit 7 of I²C register 60h).
- Implemented new adaptive BOP/EOP algorithm for the line-interleaved mode.
- Added support for the following video output formats (see Revision F of data manual).
 - 6-Ch Half-D1 at 81/108MHz
 - 6-Ch Half-D1 + 1-Ch D1 at 108MHz
 - 3-Ch D1 at 81/108MHz
- Added support for the following audio sample rates (see Revision F of data manual).
 - 12kHz, 24kHz
 - 11.025kHz, 22.05kHz
- Disabled internal pull-down resistors when video outputs are enabled.
- Fixed cross-hatch noise issue during loss of color lock.
- Resolved horizontal alignment issue in the line cropping mode (bit 6 of I²C register B1h set to 1) after writing to I²C register 5Dh.
- I²C registers BEh and BFh are no longer re-initialized to 0Fh when the video input switches from NTSC to PAL or vice versa. The power-up default setting for both registers is still 0Fh.
- Modified initialization of the new embedded V-bit control algorithm to properly support NTSC 4.43, PAL-M and PAL60 in the following two scenarios.
 - New V-bit control mode is enabled (bit 3 of I²C register 60h set to 1)
 - CIF output format in the line-interleaved mode is selected (refer to I²C register B0h)

4. Related Documentation

The following is the currently available related documentation.

Table 2. Related Documentation

Description	File	Purpose
Patch download app note	SLEA096a.pdf	Application note

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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