

TVP5157 RAM Code Release Notes

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1. Introduction

The TVP5157 has embedded video decoding firmware revision v02.00 in the device on-chip ROM. The TVP5157 device has a limited embedded RAM space which allows patch firmware code download possible. The patch can be used in improving decoder performance or fixing known decoder firmware bugs.

This document discusses the hardware and firmware issues related to the TVP5157 and fixes made by the patch v02.80.14. The discussions also include performance improvement made by the patch, the differences between the patch and the TVP5157 data manual.

2. Device & Firmware Affected

The information provided below is related only to the following device and firmware. Additional devices and firmware releases will have their own release notes.

Table 1. Device & Firmware Affected

Device	TVP5157
Firmware	v02.80.15
Patch Size	10,900 bytes
Data Manual	SLES243F.pdf

3. Device Related Issues

- The following are the known firmware issues in the TVP5157 ROM v2.00 device. Additional issues will be added to the list as they are discovered.
- Improved AGC response time
- Fixed 2-Ch pixel-interleaved mode.
- Added CTI gain and coring control - I²C address: 15h
- Fixed active video cropping issue - bit 6 of I²C address B1h
- Fixed Macrovision detection problem.
- Added OFM bypass enable for non-interleaved mode - bit 7 of I2C address B1h
- Added host interrupt when input changes to weak signal or signal present.
- Fix the INTR problem when 2nd intr set, the 1st get clear.
- Add intr open drain or intr driven bit 6 of I²C reg ADh.
- Enabled coarse clamp droop current control (I2C address BBh) to work in weak signal mode.
- Added new fine clamp mode that can be enabled by writing 0x02 to I²C register 0x98.
- Provide stable syncs when the video source is disconnected.
 - Bits 1:0 of I²C register 60h must always be set to 00b.
- Added support for the following audio sample rates (see Revision F of data manual).
 - 12kHz, 24kHz
 - 11.025kHz, 22.05kHz
- Fixed cross-hatch noise issue during loss of color lock.

- Implemented new embedded V-bit control algorithm.
 - Supports two modes of operation selectable via bit 3 of I²C register 60h.
 - Original V-bit control mode (default): Maintains a fixed vertical blanking interval as the total number of lines per frame varies.
 - New V-bit control mode: Maintains a fixed number of active lines per frame as the total number of lines per frame varies. In this mode, the minimum F1_to_Active interval is programmable via I²C address D5h (default = 8 lines).
 - Fixed embedded sync offset control (I²C register: AEh).
 - Changed default for I²C register 88h from 00h to 03h. With this setting, the F/V-bit are always decoded from the line count.
 - Changed default for I²C register 8Bh from 64h to 60h.
 - Added V-PLL free run mode (Bit 7 of I²C register 60h).
- Modified initialization of the new embedded V-bit control algorithm to properly support NTSC 4.43, PAL-M and PAL60 when the new V-bit control mode is enabled (bit 3 of I²C register 60h set to 1).

4. Related Documentation

The following is the currently available related documentation.

Table 2. Related Documentation

Description	File	Purpose
Patch download app note	SLEA096a.pdf	Application note

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