

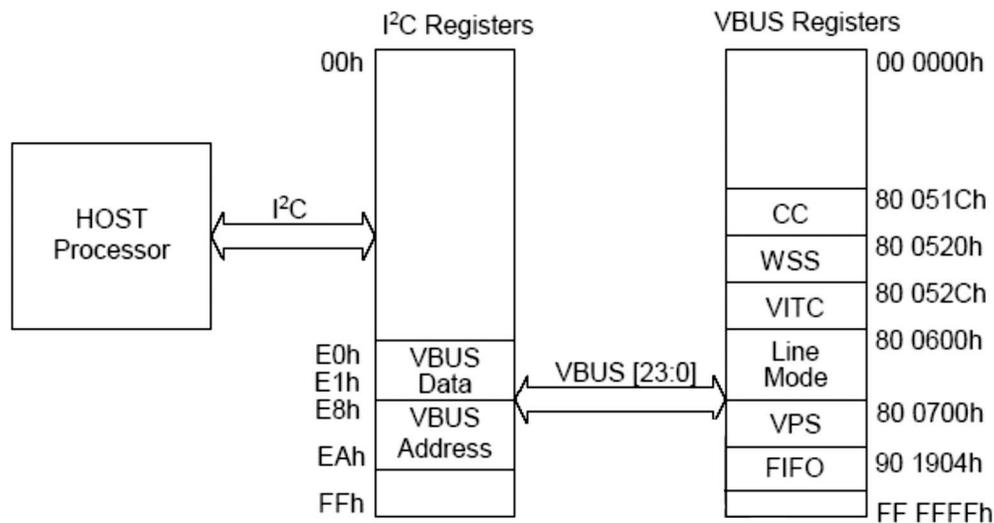
TVP5158 Patch Code Download Guidelines

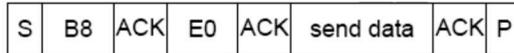
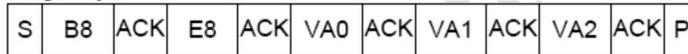
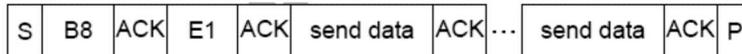
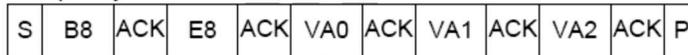
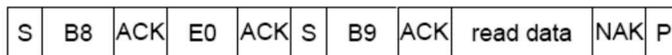
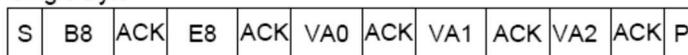
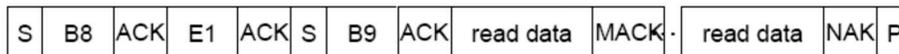
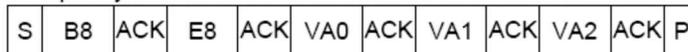
1 Overview

This application report explains how to load RAM code into the TVP5158 video decoder. The TVP5158 video decoder by default executes firmware from internal ROM on power up. Special functions or optimizations are available by utilizing the internal RAM of the TVP5158. The following describes the processed required to access and load code into the TVP5158 RAM.

2 Understanding the VBUS

It is important to understand that loading RAM code is not a feature provided by the standard I²C register map. This procedure requires I²C writes to the physical hardware of the TVP5158 CPU. These internal registers of the TVP5158 video decoder are known as VBUS registers. The following figures show a typical VBUS register access.



VBUS Write
Single Byte

Multiple Bytes

VBUS Read
Single Byte

Multiple Bytes


The examples above use default the I²C address, 0xB8. The acronyms used in the example are:

ACK – Acknowledge generated by the slave

MACK – Acknowledge generated by the master

NAK – No Acknowledge generated by the master

3 The Process

There are six steps required in order to properly load RAM code into the TVP5158.

1. Set the I²C to write to four decoders

0xFE, 0x0F

2. Place the CPU into Reset

By writing a 1 to bit 0 of the first byte in the 0xB00060 VBUS address, the internal processor is placed into a reset state. This is necessary to load RAM code. To do this, the VBUS address must first be set. Set VBUS address to 0xB00060 by making the following I²C writes.

0xE8, 0x60

0xE9, 0x00

0xEA, 0xB0

Where:

0xE8, 0xE9, 0xEA indicates the bytes of the address being setup (byte1, etc.).

0x60, 0x00, 0xB0 indicates the bytes of the physical VBUS address.

Once these writes have been performed, the current VBUS address is set to 0xB00060. Use the nonincrementing data register, 0xE0, to set the Reset bit by setting bit 0 to 1.

0xE0, 0x01

3. Set the I2C to write to four decoders

0xFE, 0x0F

4. Set the VBUS to the beginning of Program RAM

Now that the internal processor is in a reset state, the following I²C writes set the VBUS to the beginning of Program RAM. This is the location in which the RAM code will be stored during the loading process. Set the VBUS address to the beginning of Program RAM, 0x400000.

0xE8, 0x00

0xE9, 0x00

0xEA, 0x40

5. Load the RAM Code

With the VBUS now set to the beginning of Program RAM, start loading the provided RAM code *.bin file using the following writes. Because the firmware code data is loaded at once, the incrementing VBUS data register, 0xE1 must be used, where:

0xE1, (RAM Code Data)

Using the above technique, all of the bytes of the firmware should be written using a single I²C transaction. See below for details.

ST B8 E1 D0 D1 ... DN-1 SP

Where:

ST = I²C start condition

B8 = TVP5158 device I²C address for writes (could also be BA depending on the GLCO/I2CA pin at the end of RESET)

E1 = I²C sub-address of the incrementing VBUS data register

D0 D1 ... DN-1D = Data from the binary firmware file. N is the number of bytes in the firmware file.

SP = I²C stop condition

6. Set the RAM Loaded Bit

For the default ROM code to understand RAM load has been used, the RAM Loaded bit must be used. This is used by the internal CPU to execute out of RAM instead of ROM. To set the RAM Loaded bit, set VBUS address to 0xB00060.

0xE8, 0x60

0xE9, 0x00

0xEA, 0xB0

Write 0x03 to the nonincrementing VBUS data register, 0xE0, sets the RAM Loaded bit and keeps the CPU RESET bit set.

0xE0, 0x03

7. Release the CPU Reset

To restart the CPU and release it from its reset state, a write of 0x02 to the same VBUS address as above (0xB00060) is necessary.

0xE8, 0x60

0xE9, 0x00

0xEA, 0xB0

0xE0, 0x02

8. The patch code should now be running.

The revision number can be verified by reading the ROM version, RAM version MSB, and RAM version LSB from I²C registers 0x04, 0x05, and 0x06, respectively.

For example:

Patch Release = v02.01.22

ROM Version = 0x02

RAM Version MSB = 0x01

RAM Version LSB = 0x22

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