

Ittiam G711 Decoder

G711 Decoder

The ITU G.711 converts digitized, linear PCM input signals (16 bit PCM) sampled at a 8 kHz sampling rate into 64 kbps alaw/ulaw encoded bit stream using the priciples of non-linear quantization.

Features

- Decoder decompresses 64 Kbps bit stream into linear PCM samples.
- Bit Compliant with ITU-T G.711 specifications
- Optimized for ARM9E
- C callable interface for the decoder
- Re-entrant multi channel implementation
- Implementation Compatible with TI XDAIS rules
- Fully interruptible Code

Decoder Validation

The G711 decoder implementation is fully complaint to G711 Test specification as defined by ITU-T. The decoder has also been tested for robustness with erroneous bit-streams and quality validation has been done by means of listening tests.

Resource requirements on ARM9E Processor

Function	MCPS	Pgm	Tables	Static	Scratch
	Peak	ROM (Bytes)		RAM (kb)	
Decode	0.02	910	512	Nil	Nil

Note

The Data Memory mentioned in the above Table does not include Input/ Output buffers.

The MCPS have been calculated by profiling the G711Decoder functions with the generated test-vectors for a 10ms frame size (80 samples)

All memory numbers are in bytes. Program Memory includes the XDAIS interface overhead

MCPS measurement on 0 wait- state memory access

Details of ARM9E Resources required

CPU Loading

CPU	Simulator	Hardware
Description	Ave MCPS	Ave MCPS
A law	0.02	0.31
U law	0.02	0.31

Memory Usage

Program	Tables	Static	Scratch	Stack
910	512	Nil	Nil	<128

Note:

- Memory numbers are in bytes
- Performance numbers on Simulator generated with ARM RVDS Tools version 2.1 *with 0-wait state memory access and without Cache*
- Hardware performance generated on a ARM9E processor with 16kB of I-Cache and 8kB of D-Cache
- Hardware performance generated under Linux 2.6 , using the ARM-GCC 3.4.3 Compiler
- MCPS numbers on the hardware will vary with the I-Cache and D-Cache size and with the memory configuration/place

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